DATA SHEET

PCF8535
65 × 133 pixel matrix driver

Product specification
Supersedes data of 1999 Aug 24
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Philips
Semiconductors

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CONTENTS

65 × 133 pixel matrix driver PCF8535

1 FEATURES

- Single-chip LCD controller/driver
- 65 row, 133 column outputs
- Display data RAM 65 × 133 bits
- 133 icons (last row is used for icons)
- Fast mode I^2C-bus interface (400 kbits/s)
- Software selectable multiplex rates: 1 : 17, 1 : 26, 1 : 34, 1 : 49 and 1 : 65
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
  - Generation of V_{LCD}.
- CMOS compatible inputs
- Software selectable bias configuration
- Logic supply voltage range V_{DD1} to V_{SS1} from 4.5 to 5.5 V
- Supply voltage range for high voltage part V_{DD2} and V_{DD3} to V_{SS2} from 4.5 to 5.5 V
- Display supply voltage range V_{LCD} to V_{SS} from 8 to 16 V (Mux rate 1 : 65)
- Low power consumption, suitable for battery operated systems
- Internal Power-on reset and/or external reset
- Temperature read back available
- Manufactured in N-well silicon gate CMOS process.

2 APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Instrumentation.

3 GENERAL DESCRIPTION

The PCF8535 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 17, 1 : 26, 1 : 34, 1 : 49 and 1 : 65. Furthermore, it can drive up to 133 icons. All necessary functions for the display are provided in a single-chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and low power consumption. The PCF8535 is compatible with most microcontrollers and communicates via an industry standard two-line bidirectional I^2C-bus serial interface. All inputs are CMOS compatible.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8535U/2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

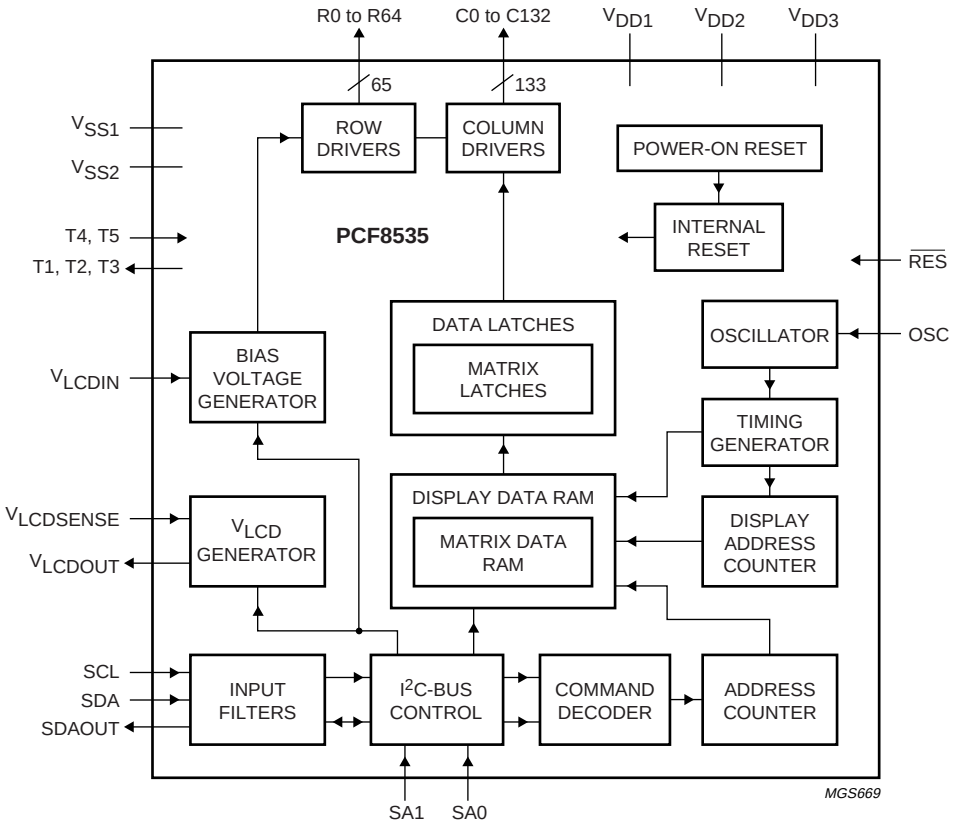


Fig.1 Block diagram.

5.1 Block diagram functions

5.1.1 OSCILLATOR

The on-chip oscillator provides the display clock for the system; it requires no external components. Alternatively, an external display clock may be provided via the OSC input. The OSC input must be connected to V_{DD1} or V_{SS1} when not in use. During power-down additional current saving can be made if the external clock is disabled.

5.1.2 POWER-ON RESET

The on-chip Power-on reset initializes the chip after power-on or power failure.

5.1.3 I²C-BUS CONTROLLER

The I²C-bus controller detects the I²C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel). The PCF8535 acts as an I²C-bus slave and therefore cannot initiate bus communication.

5.1.4 INPUT FILTERS

Input filters are provided to enhance noise immunity in electrically adverse environments. RC low-pass filters are provided on the SDA, SCL and $\overline{RES}$ lines.

5.1.5 DISPLAY DATA RAM

The PCF8535 contains a 65 × 133 bit static RAM which stores the display data. The RAM is divided into 9 banks of 133 bytes. The last bank is used for icon data and is only one bit deep. During RAM access, data is transferred to the RAM via the I²C-bus interface. There is a direct correspondence between the X address and the column output number.

5.1.6 TIMING GENERATOR

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

5.1.7 ADDRESS COUNTER

The address counter sends addresses to the Display Data RAM (DDRAM) for writing.

5.1.8 DISPLAY ADDRESS COUNTER

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The display status (all dots on or off, normal or inverse video) is set via the I²C-bus.

6 PINNING

SYMBOL	PAD	DESCRIPTION
dummy	1	–
bump/align 1	2	–
R0 to R15	3 to 18	LCD row driver outputs
C0 to C132	19 to 151	LCD column driver outputs
R47 to R33	152 to 166	LCD row driver outputs
bump/align 2	167	–
dummy	168	–
R48 to R64	169 to 185	LCD row driver outputs; R64 is icon row
bump/align 3	186	–
dummy	187 to 189	–
OSC	190	oscillator
V_{LCDIN}	191 to 196	LCD supply voltage
V_{LCDOUT}	197 to 203	voltage multiplier output
$V_{LCDSENSE}$	204	voltage multiplier regulation input (V_{LCD})
dummy	205 and 206	–
$\overline{RES}$	207	external reset input (active LOW)
T3	208	test output 3
T2	209	test output 2
T1	210	test output 1
V_{DD2}	211 to 218	supply voltage 2
V_{DD3}	219 to 222	supply voltage 3
V_{DD1}	223 to 228	supply voltage 1
dummy	229	–
SDA	230 and 231	I^2C-bus serial data input
SDAOUT	232	I^2C-bus serial data output
SA1	233	I^2C-bus slave address input 1
SA0	234	I^2C-bus slave address input 0
V_{SS2}	235 to 242	ground 2
V_{SS1}	243 to 250	ground 1
T5	251	test input 5
T4	252	test input 4
dummy	253	–
SCL	254 and 255	I^2C-bus serial clock input
bump/align 4	256	–
R32 to R16	257 to 273	LCD row driver outputs

6.1 Pin functions

6.1.1 R0 TO R64

These pads output the display row signals.

6.1.2 C0 TO C132

These pads output the display column signals.

6.1.3 V_{SS1} AND V_{SS2}

V_{SS1} and V_{SS2} must be connected together.

6.1.4 V_{DD1} TO V_{DD3}

V_{DD1} is the logic supply. V_{DD2} and V_{DD3} are for the voltage multiplier. For split power supplies V_{DD2} and V_{DD3} must be connected together. If only one supply voltage is available, all three supplies must be connected together.

6.1.5 V_{LCDOUT}

If, in the application, an external V_{LCD} is used, V_{LCDOUT} must be left open-circuit; otherwise (if the internal voltage multiplier is enabled) the chip may be damaged. V_{LCDOUT} should not be driven when V_{DD1} is below its minimum allowed value otherwise a low impedance path between V_{LCDOUT} and V_{SS1} will exist.

6.1.6 V_{LCDIN}

This is the V_{LCD} supply for when an external V_{LCD} is used. If the internal V_{LCD} generator is used, then V_{LCDOUT} and V_{LCDIN} must be connected together. V_{LCDIN} should not be driven when V_{DD1} is below its minimum allowed value, otherwise a low impedance path between V_{LCDIN} and V_{SS1} will exist.

6.1.7 $V_{LCDSENSE}$

This is the input to the internal voltage multiplier regulator. It must be connected to V_{LCDOUT} when the internal voltage generator is used otherwise it may be left open-circuit. $V_{LCDSENSE}$ should not be driven when V_{DD1} is below its minimum allowed value, otherwise a low impedance path between $V_{LCDSENCE}$ and V_{SS1} will exist.

6.1.8 SDA

I^2C-bus serial data input.

6.1.9 SDAOUT

SDAOUT is the serial data acknowledge for the I^2C-bus. By connecting SDAOUT to SDA externally, the SDA line becomes fully I^2C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the PCF8535 will not be able to create a valid LOW level. By splitting the SDA input from the SDAOUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required or where read back is required, it is necessary to minimize the track resistance from the SDAOUT pad to the system SDA line to guarantee a valid LOW level.

6.1.10 SCL

I^2C-bus serial clock input.

6.1.11 SA0 AND SA1

Least significant bits of the I^2C-bus slave address.

Table 1 Slave address

The slave address is a concatenation of the following bits 0, 1, 1, 1, 1, SA1, SA0 and R/W.

SA1 AND SA0	MODE	SLAVE ADDRESS
0 and 0	write	78H
	read	79H
0 and 1	write	7AH
	read	7BH
1 and 0	write	7CH
	read	7DH
1 and 1	write	7EH
	read	7FH

6.1.12 OSC

If the on-chip oscillator is used this input must be connected to V_{DD1} or V_{SS1}.

6.1.13 $\overline{RES}$

When the external reset input is LOW the chip will be reset (see Section 7.1). If an external reset is not required, this pad must be tied to V_{DD1}. Timing for the $\overline{RES}$ pad is given in Chapter 12.

6.1.14 T1, T2, T3, T4 AND T5

In applications T4 and T5 must be connected to V_{SS}. T1, T2 and T3 are to be left open-circuit.

7 FUNCTIONAL DESCRIPTION

The PCF8535 is a low power LCD driver designed to interface with microprocessors or microcontrollers and a wide variety of LCDs.

The host microprocessor or microcontroller and the PCF8535 are both connected to the I^2C-bus. The SDA and SCL lines must be connected to the positive power supply via pull-up resistors. The internal oscillator requires no external components. The appropriate intermediate biasing voltages for the multiplexed LCD waveforms are generated on-chip. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and suitable capacitors for decoupling V_{LCD} and V_{DD}.

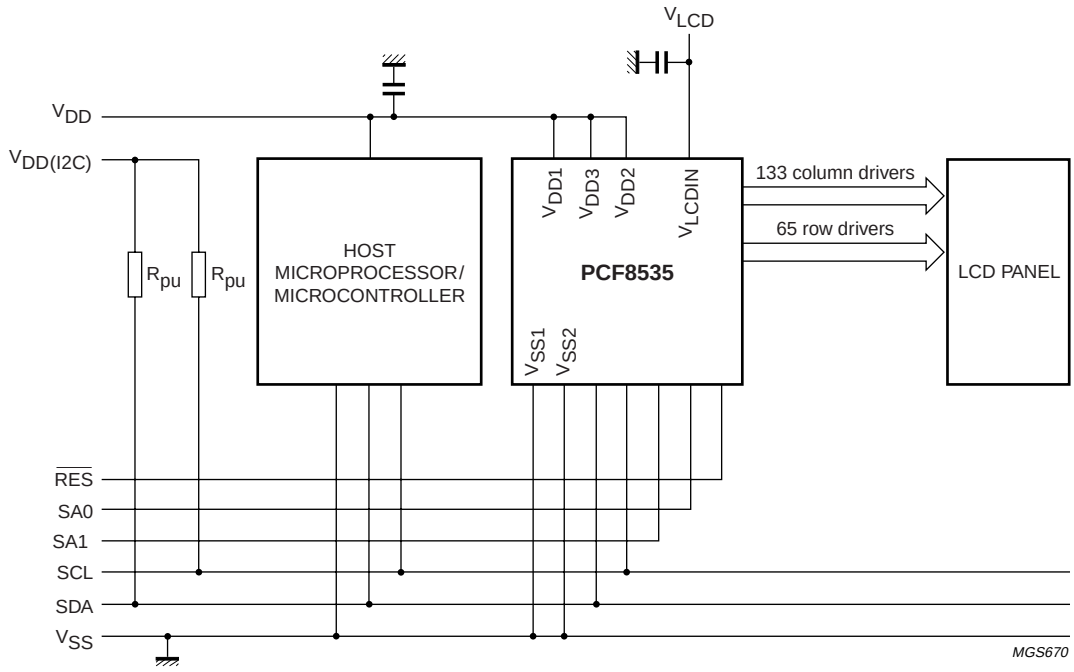


Fig.2 Typical system configuration.

7.1 Reset

The PCF8535 has two Reset modes: internal Power-on reset or external reset. Reset initiated from either the $\overline{RES}$ pad or the internal Power-on reset block will initialize the chip to the following starting condition:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0); no mirror X or Y (MX = 0 and MY = 0)
- Display blank (D = 0 and E = 0)
- Address counter X[6:0] = 0, Y[2:0] = 0 and XM_0 = 0
- Bias system BS[2:0] = 0
- Multiplex rate M[2:0] = 0 (Mux rate 1 : 17)
- Temperature control mode TC[2:0] = 0
- HV-gen control, HVE = 0 (HV generator is switched off), PRS = 0 and S[1:0] = 00
- V_{LCDOUT} is equal to 0 V
- RAM data is unchanged (Remark: RAM data is undefined after power-up)
- All row and column outputs are set to V_{SS} (display off)
- TRS and BRS are set to zero
- Direct mode is disabled (DM = 0)
- Internal oscillator is selected, but not running (EC = 0)
- Bias current set to low current mode (IB = 0).

7.2 Power-down

During power-down all static currents are switched off (no internal oscillator, no timing and no LCD segment drive system) and all LCD outputs are internally connected to V_{SS}. The I^2C-bus function remains active.

7.3 LCD supply voltage selector

The practical value for V_{OP} is determined by equating $V_{off(rms)}$ with the defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast.

7.4 Oscillator

The internal logic operation and the multi-level drive signals of the PCF8535 are clocked by the built-in RC oscillator. No external components are required.

7.5 Timing

The timing of the PCF8535 organizes the internal data flow of the device. The timing also generates the LCD frame frequency which is derived from the clock frequency generated by the internal clock generator.

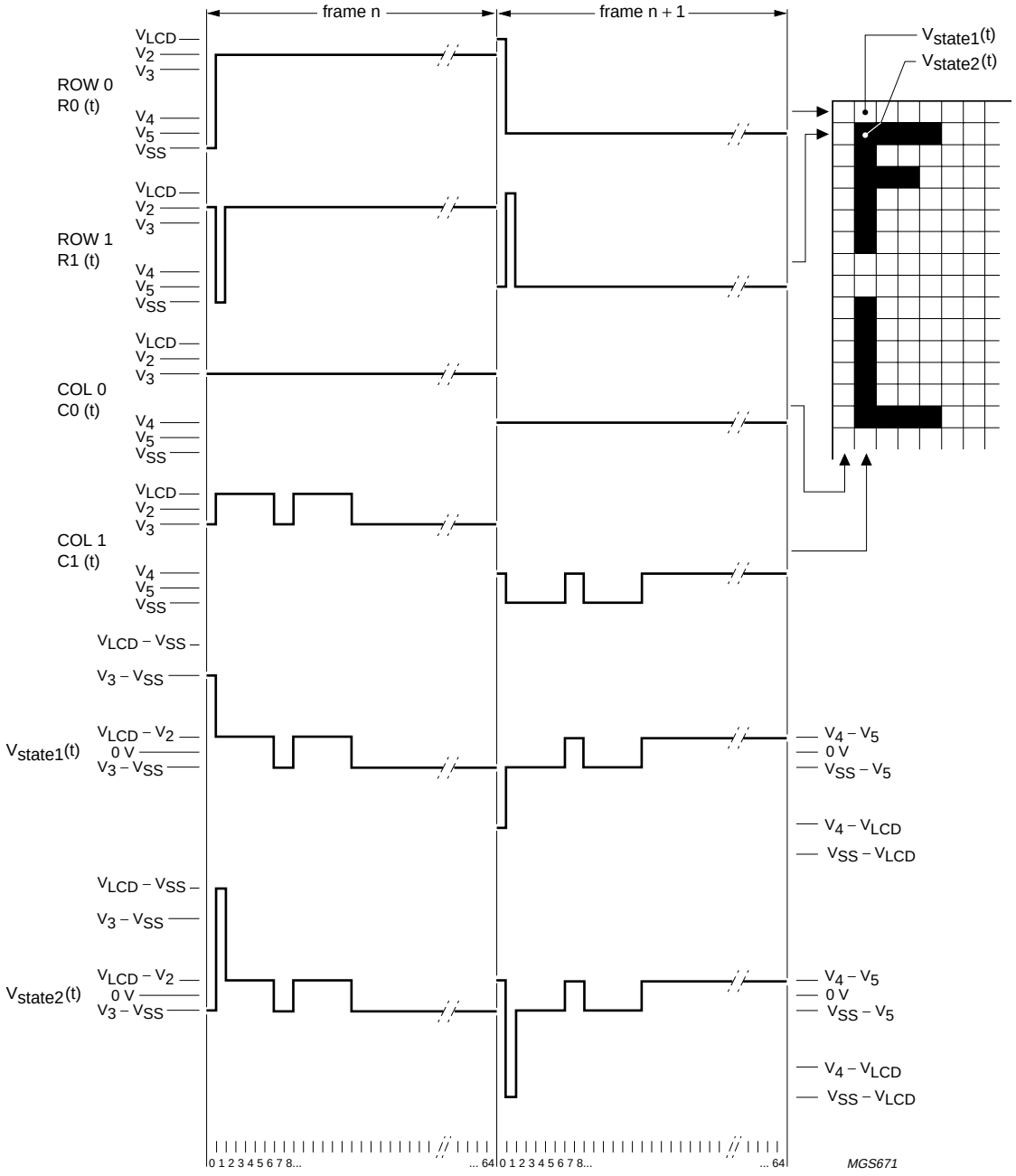
7.6 Column driver outputs

The LCD drive section includes 133 column outputs (C0 to C132) which should be connected directly to the LCD. The column output signals are generated in accordance with the multiplexed row signals and with the data in the display latch. When less than 133 columns are required the unused column outputs should be left open-circuit.

7.7 Row driver outputs

The LCD drive section includes 65 row outputs (R0 to R64) which should be connected directly to the LCD. The row output signals are generated in accordance with the selected LCD drive mode. If lower multiplex rates or less than 65 rows are required, the unused outputs should be left open-circuit.

7.8 Drive waveforms



$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R1(t)$.

Fig.3 Typical LCD driver waveforms.

7.9 Set multiplex rate

The PCF8535 can be used to drive displays of varying sizes. The selected multiplex rate controls which rows are used. In all cases, the last row is always driven and is intended for icons. If Top Row Swap (TRS) is at logic 1, then the icon row will be output on pad R48. M[2:0] selects the multiplex rate (see Table 2).

Table 2 Multiplex rates

M2	M1	M0	MULTIPLEX RATE	ACTIVE ROWS
0	0	0	1 : 17	R0 to R15 and R64
0	0	1	1 : 26	R0 to R24 and R64
0	1	0	1 : 34	R0 to R32 and R64
0	1	1	1 : 49	R0 to R47 and R64
1	0	0	1 : 65	R0 to R64
1	0	1	do not use	–
:	:	:	:	:
1	1	1	do not use	–

7.10 Bias system

7.10.1 Set bias system

The bias voltage levels are set in the ratio of R – R – nR – R – R. Different multiplex rates require different factors n. This is programmed by BS[2:0]. For optimum bias values, n can be calculated from:

$$n = \sqrt{\text{Mux rate}} - 3$$

Changing the bias system from the optimum values will have a consequence on the contrast and viewing angle. One reason to come away from the optimum would be to reduce the required V_{OP}. A compromise between contrast and V_{OP} must be found for any particular application.

Table 3 Programming the required bias system

BS2	BS1	BS0	n	BIAS MODE	TYPICAL MUX RATES
0	0	0	7	$^1/_{11}$	1 : 100
0	0	1	6	$^1/_{10}$	1 : 80
0	1	0	5	$^1/_9$	1 : 65
0	1	1	4	$^1/_8$	1 : 49
1	0	0	3	$^1/_7$	1 : 34
1	0	1	2	$^1/_6$	1 : 26
1	1	0	1	$^1/_5$	1 : 17
1	1	1	0	$^1/_4$	1 : 9

Table 4 Example of LCD bias voltage for $^1/_7$ bias mode (n = 3)

SYMBOL	BIAS VOLTAGE
V1	V_{LCD}
V2	$^6/_7 \times V_{LCD}$
V3	$^5/_7 \times V_{LCD}$
V4	$^2/_7 \times V_{LCD}$
V5	$^1/_7 \times V_{LCD}$
V6	V_{SS}

7.11 Temperature measurement

7.11.1 Temperature read back

The PCF8535 has an in-built temperature sensor. For power saving, the sensor should only be enabled when a measurement is required. It will not operate in the Power-down mode. The temperature read back requires a clock to operate. Normally the internal clock is used but, if the device is operating from an external clock, then this clock must be present for the measurement to work. V_{DD2} and V_{DD3} must also be applied. A measurement is initialized by setting the SM bit. Once started the SM bit will be automatically cleared. An internal oscillator will be initialized and allowed to warm-up for approximately 2 frame periods. After this the measurement starts and lasts for a maximum of 2 frame periods.

Temperature data is returned via a status register. During the measurement the register will contain zero. Once the measurement is completed the register will be updated with the current temperature (non zero value). Because the I^2C-bus interface is asynchronous to the temperature measurement, read back prior to the end of the measurement is not guaranteed. If this mode is required the register should be read twice to validate the data.

The ideal temperature read-out can be calculated as follows:

$$TR_{ideal} = 128 + (T - 27) \times \frac{1}{c} \quad (1)$$

where T is the on-chip temperature in °C and c is the conversion constant: c = 1.17 °C/lsb.

It should be noted that the temperature read-out is only valid when TC0 is selected. If another TC is used, the read-out function will generate a non-linear result.

To improve the accuracy of the temperature measurement a calibration is recommended during the assembly of the final product.

For calibrating the temperature read-out a measurement must be taken at a defined temperature. The offset between the ideal read-out and the actual result has to be stored into a non-volatile register (e.g. EEPROM):

$$\text{Offset} = TR_{ideal} - TR_{meas} \quad (2)$$

where TR_{meas} is the actual temperature read-out of the PCF8535.

The calibrated temperature read-out can be calculated for each measurement as follows:

$$TR_{cal} = TR_{meas} + \text{Offset} \quad (3)$$

The accuracy after the calibration is ±6.7% (plus ±1 lsb) of the difference between the current temperature and the calibration temperature. For this reason a calibration at or near the most sensitive temperature for the display is recommended. E.g. for a calibration at 25 °C with the current temperature at –20 °C, the absolute error may be calculated as:

Absolute error = 0.067 × [25 – (–20)]
= ±3 °C + ±1 lsb = ±4.17 °C.

7.12 Temperature compensation

7.12.1 TEMPERATURE COEFFICIENTS

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage, Voltage must be increased at lower temperatures to maintain optimum contrast. Fig.4 shows V_{LCD} as a function of temperature for a typical high multiplex rate liquid.

In the PCF8535 the temperature coefficient of V_{LCD} can be selected from 8 values by setting bits TC[2:0] (see Table 5).

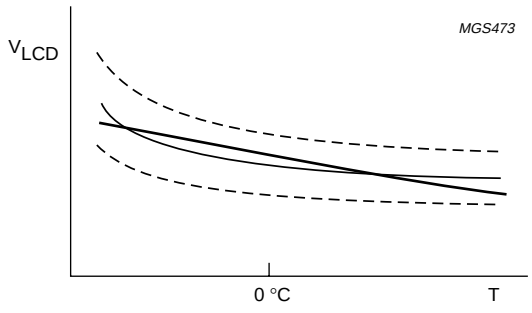


Fig.4 V_{LCD} as function of liquid crystal temperature (typical values).

Table 5 Selectable temperature coefficients

TC2	TC1	TC0	TC VALUE	UNIT
0	0	0	0	1/°C
0	0	1	-0.44×10^{-3}	1/°C
0	1	0	-1.10×10^{-3}	1/°C
0	1	1	-1.45×10^{-3}	1/°C
1	0	0	-1.91×10^{-3}	1/°C
1	0	1	-2.15×10^{-3}	1/°C
1	1	0	-2.32×10^{-3}	1/°C
1	1	1	-2.74×10^{-3}	1/°C

7.13 V_{OP}

7.13.1 SET V_{OP} VALUE

The voltage at the reference temperature (T_{cut}) can be calculated as:

$$V_{LCD(Tcut)} = a + b \times V_{OP} \quad (4)$$

The operating voltage, V_{OP}, can be set by software. The generated voltage is dependent on the temperature, programmed Temperature Coefficient (TC) and the programmed voltage at the reference temperature (T_{cut}):

$$V_{LCD} = (a + b \times V_{OP}) \times \{1 + [(T - T_{cut}) \times TC]\} \quad (5)$$

The values for T_{cut}, a and b are given in Table 6. The maximum voltage that can be generated is dependent on the voltage V_{DD2} and the display load current. Two overlapping V_{OP} ranges are selectable via the command page “HV-gen control” (see Fig.5).

The LOW range offers programming from 4.5 to 10.215 V, with the HIGH range from 10.215 to 15.93 V at T_{cut}. Care must be taken, when using temperature coefficients, that the programmed voltage does not exceed the maximum allowed V_{LCD}, see Chapter 10.

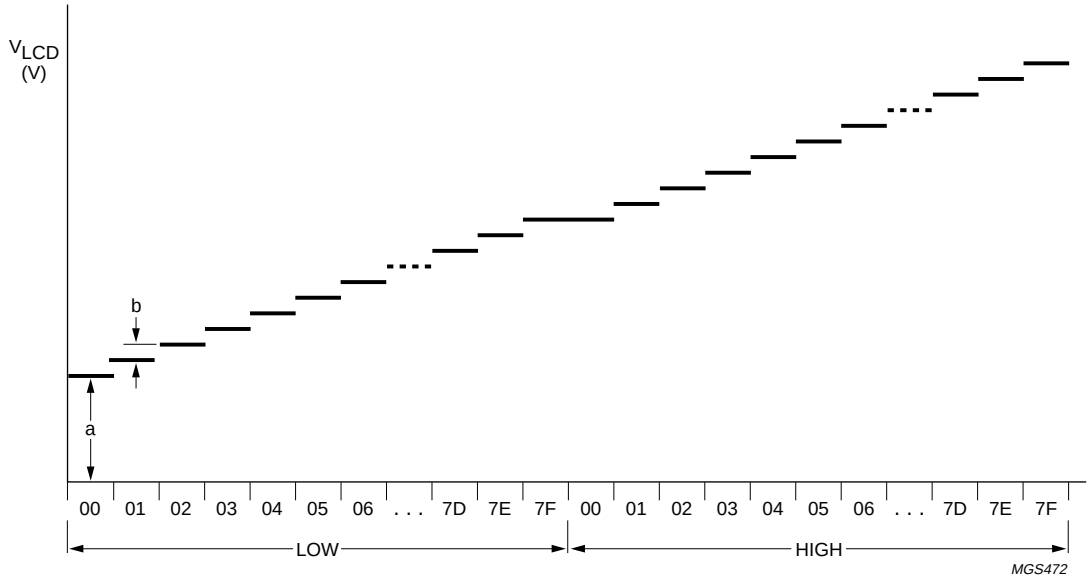
For a particular liquid, the optimum V_{LCD} can be calculated for a given multiplex rate. For a Mux rate of 1 : 65, the optimum operating voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{65}}\right)}} \times V_{th} = 6.85 \times V_{th} \quad (6)$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Table 6 Values for parameters of V_{OP} programming

SYMBOL	BITS	VALUE	UNIT
a	PRS = 0	4.5	V
	PRS = 1	10.215	V
b		0.045	V
T_{cut}		27	°C



V_{OP}[6:0] programming (00H to 7FH, programming range LOW and HIGH).

Fig.5 V_{OP} programming of PCF8535.

7.14 Voltage multiplier control

7.14.1 S[1:0]

The PCF8535 incorporates a software configurable voltage multiplier. After reset ($\overline{RES}$) the voltage multiplier is set to $2 \times V_{DD2}$. Other voltage multiplier factors are set via the HV-gen command page. Before switching on the charge pump, the charge pump has to be pre-charged using the following sequence.

A starting state of HVE = 0, DOF = 0, PD = 1 and DM = 0 is assumed. A small delay between the steps is indicated. The recommended wait period is 20 µs per 100 nF of the capacitance on V_{LCD}.

1. Set DM = 1 and PD = 0
2. Delay
3. Set the multiplication factor to 2 by setting S[1:0] = 00
4. Set the required V_{OP} and PRS.
5. Set HVE = 1 to switch-on the charge pump with a multiplication factor of 2
6. Delay
7. Increase the number of stages, one at a time, with a delay between each until the required level is achieved.

Table 7 HV generator multiplication factor

S1	S0	MULTIPLICATION FACTOR
0	0	$2 \times V_{DD2}$
0	1	$3 \times V_{DD2}$
1	0	$4 \times V_{DD2}$
1	1	$5 \times V_{DD2}$

7.15 Addressing

Addressing of the RAM can be split into two parts: input addressing and output addressing. Input addressing is concerned with writing data into the RAM. Output addressing is almost entirely automatic and taken care of by the device, however, it is possible to affect the output mode.

7.15.1 INPUT ADDRESSING

Data is downloaded byte wise into the RAM matrix of the PCF8535 as indicated in Figs 6 to 10.

The display RAM has a matrix of 65 × 133 bits. The columns are addressed by a combination of the X address pointer and the X-RAM page pointer, whilst the rows addressed in groups of 8 by the Y address pointer. The X address pointer has a range of 0 to 127 (7FH). Its range can be extended by the X-RAM page pointer XM_0. The Y address pointer has a range of 0 to 8 (08H). The PCF8535 is limited to 133 columns by 65 rows, addressing the RAM outside of this area is not allowed.

Table 8 Effect of X-RAM page pointer

X ADDRESS POINTER	X-RAM PAGE POINTER XM_0	ADDRESSED COLUMN MX = 0	ADDRESSED COLUMN MX = 1
0	0	C0	C132
1	0	C1	C131
2	0	C2	C130
:	:	:	:
125	0	C125	C7
126	0	C126	C6
127	0	C127	C5
0	1	C128	C4
1	1	C129	C3
:	:	:	:
4	1	C132	C0

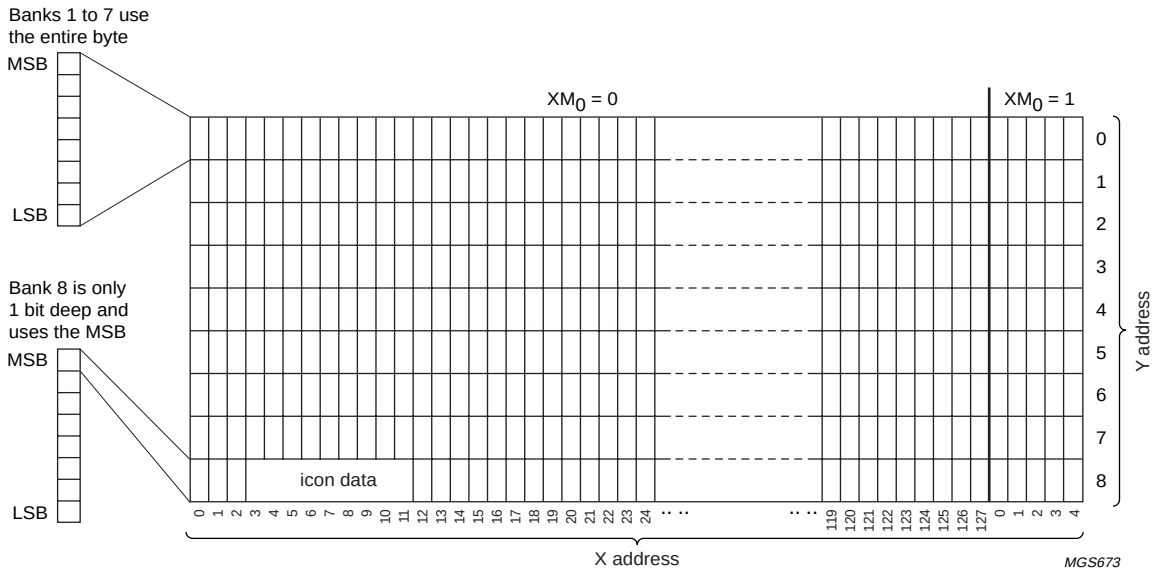


Fig.6 RAM format, input addressing.

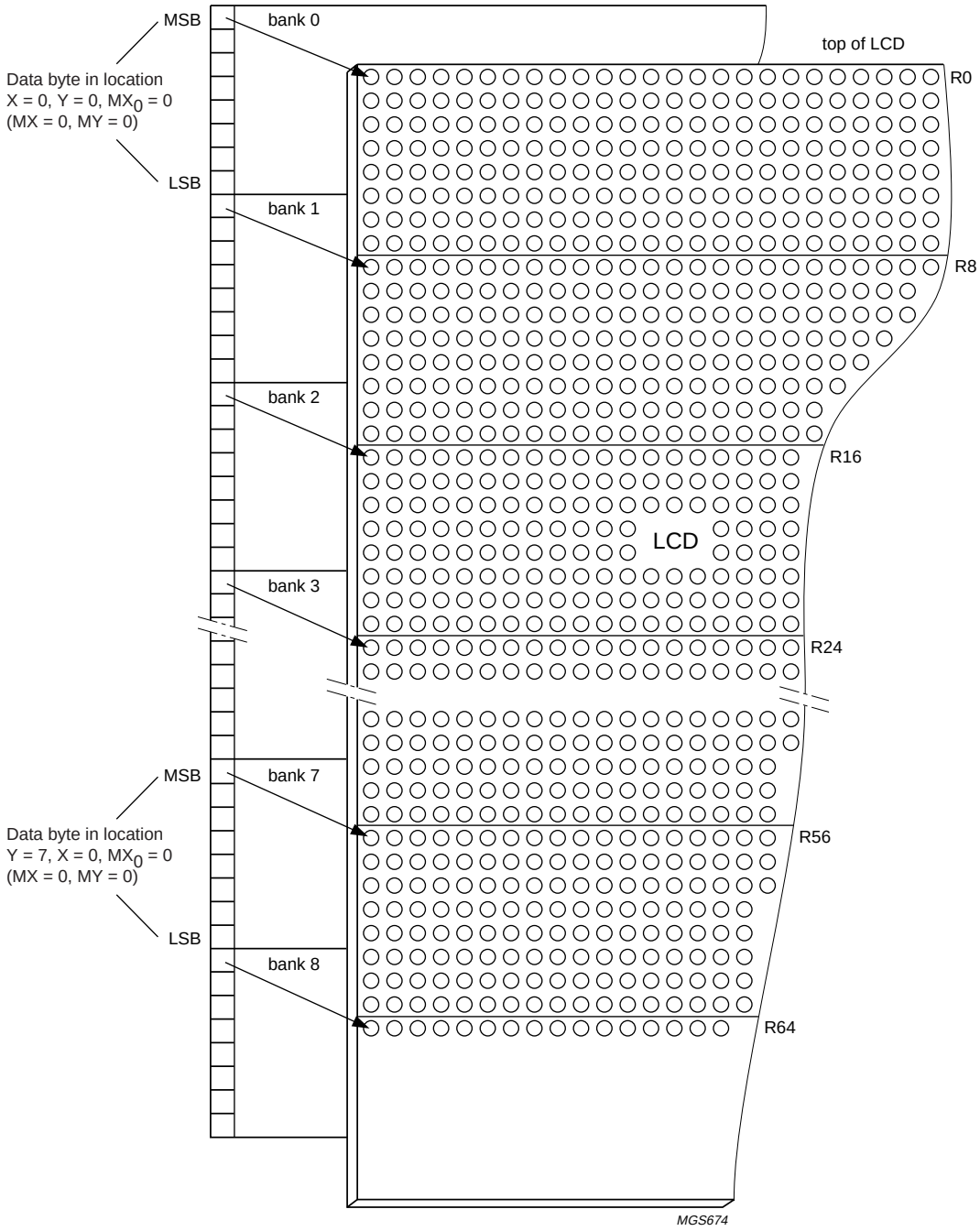


Fig.7 DDRAM to display mapping.

Two automated addressing modes are available: vertical addressing (V = 1) and horizontal addressing (V = 0). These modes change the way in which the auto-incrementing of the address pointers is handled and are independent of multiplex rate. The auto-incrementing works in a way so as to aid filling of the entire RAM. It is not a prerequisite of operation that the entire RAM is filled: in lower multiplex rates not all of the RAM will be needed. For these multiplex rates, use of horizontal addressing mode (V = 0) is recommended.

Addressing the icon row is a special case as these RAM locations are not automatically accessed. These locations must be explicitly addressed by setting the Y address pointer to 8.

The Y address pointer does not auto-increment when the X address over or underflows, it stays set to 8. Writing icon data is independent of the vertical and horizontal addressing mode, but is effected by the mirror X bit as described in Sections 7.15.1.2 and 7.15.1.3.

The addressing modes may be further modified by the mirror X bit MX. This bit causes the data to be written into the RAM from right to left instead of the normal left to right. This effectively flips the display about the Y axis. The MX bit affects the mode of writing into the RAM; changing the MX bit after RAM data is written will not flip the display.

7.15.1.1 Vertical addressing non-mirrored

In the vertical addressing mode data is written top to bottom and left to right. Here, the Y counter will auto-increment from 0 to 7 and then wrap around to 0 (see Fig.8). On each wrap-over, the X counter will increment to address the next column. When the X counter wraps over from 127 to 0, the XM_0 bit will be set. The last address accessible is Y = 7, X = 4 and XM_0 = 1; after this access the counter will wrap around to Y = 0, X = 0 and XM_0 = 0.

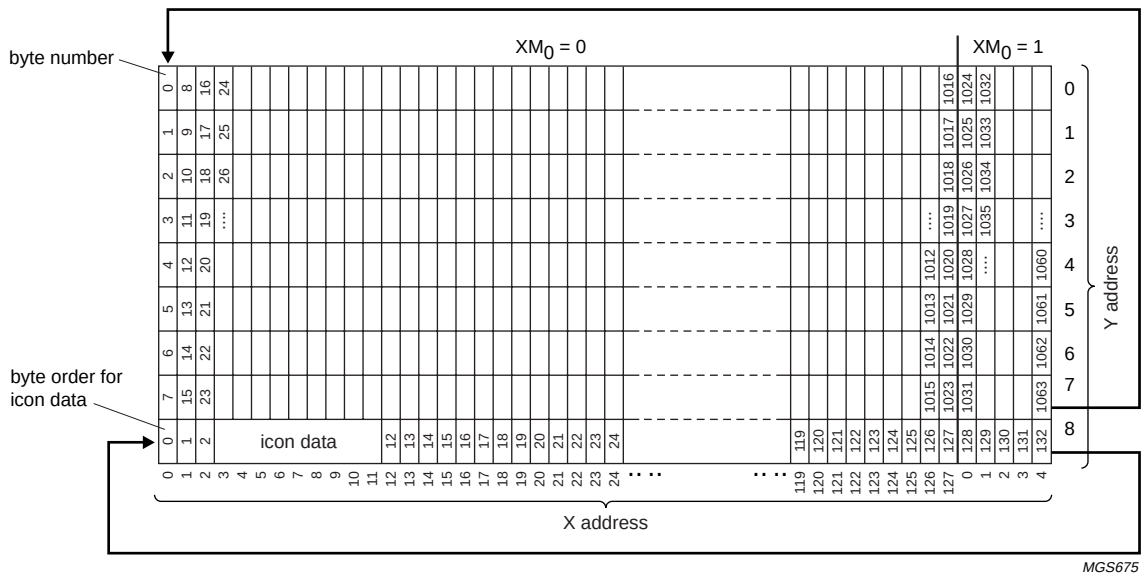


Fig.8 Sequence of writing data bytes into the RAM with normal vertical addressing (V = 1 and MX = 0).

7.15.1.2 Vertical addressing mirrored

It is also possible to write data from right to left, instead of from the normal left to right, still going top to bottom. In the mirrored vertical addressing mode the Y counter will auto-increment from 0 to 7 and then wrap around to 0 (see Fig.9). On each wrap-over, the X counter will decrement to address the preceding column. The XM_0 bit will be automatically toggled each time the X address counter wraps over from 0. The last address accessible is Y = 7, X = 4 and XM_0 = 1; after this access the counter will wrap around to Y = 0, X = 0 and XM_0 = 0.

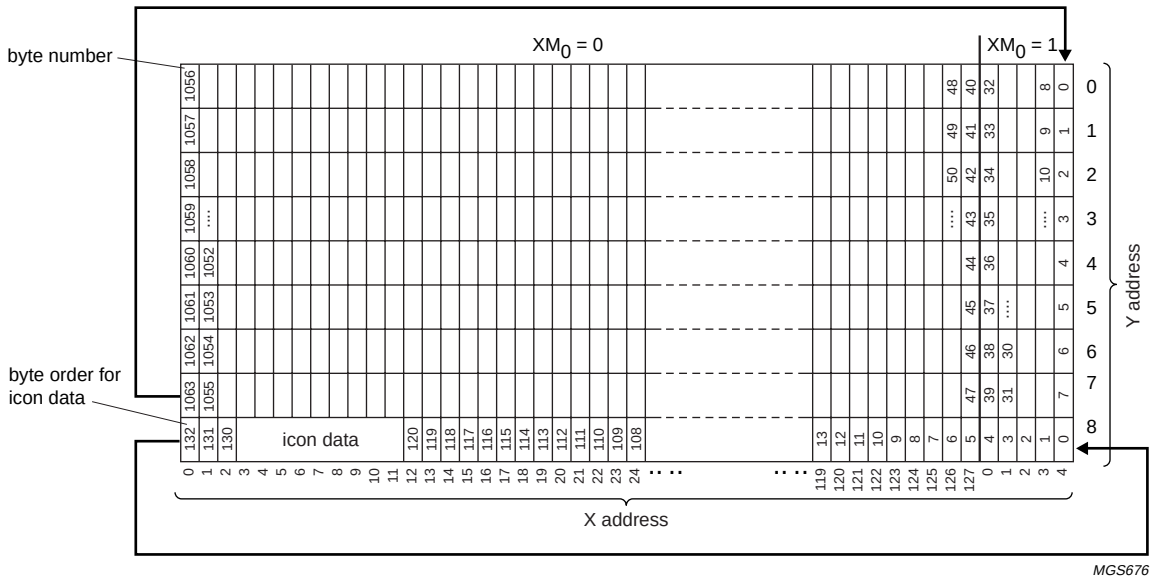


Fig.9 Sequence of writing data bytes into the RAM with mirrored vertical addressing (V = 1 and MX = 1).

7.15.1.3 Horizontal addressing non-mirrored

In horizontal addressing bit data is written from left to right and top to bottom. Here, the X counter will auto-increment from 0 to 127, set the XM_0, then count 0 to 4 before wrapping around to 0 and clearing the XM_0 bit (see Fig.10). On each wrap-over, the Y counter will increment. The last address accessible is Y = 7, X = 4 and XM_0 = 1; after this access the counter will wrap around to Y = 0, X = 0 and XM_0 = 0.

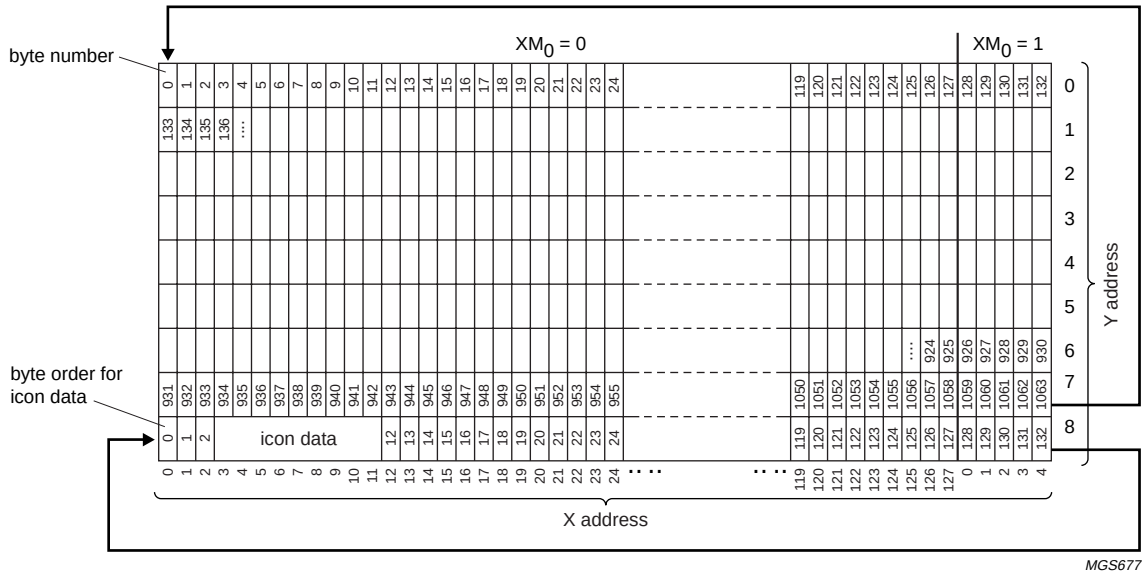


Fig.10 Sequence of writing data bytes into the RAM with normal horizontal addressing (V = 0 and MX = 0).

7.15.1.4 Horizontal addressing mirrored

It is also possible to write data from right to left, instead of from the normal left to right, still going top to bottom. In the mirrored horizontal addressing mode the X counter will auto-decrement from 4 to 0, clear the XM_0, then count 127 to 0 before wrapping around to 4 and setting the XM_0 bit (see Fig.11). On each wrap-over, the Y counter will increment. The last address accessible is Y = 7, X = 4 and XM_0 = 0; after this access the counter will wrap around to Y = 0, X = 0 and XM_0 = 0.

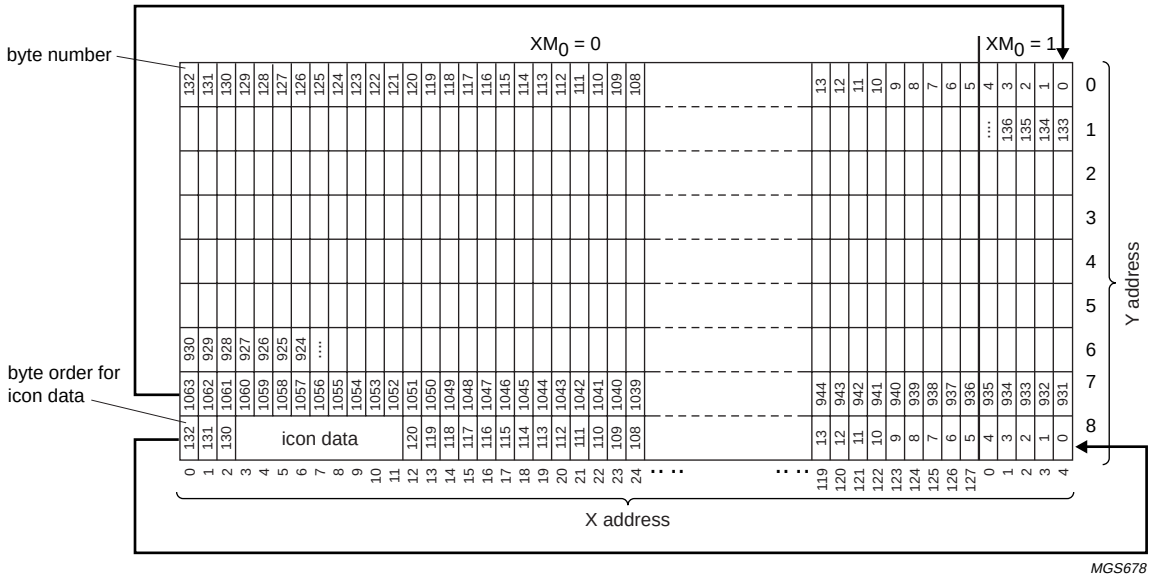


Fig.11 Sequence of writing data bytes into the RAM with mirrored horizontal addressing (V = 0 and MX = 1).

7.15.1.5 Use of MX and MY bits

The MX bit is used to flip the display left to right; as shown in Fig.12. This utility allows the display to be viewed from behind instead of on top, allowing for flexibility in the assembly of equipment and saving complicated data manipulation within the controller.

The MY bits flips the display top to bottom. A combination of MY and MX allows the display to be rotated 180 deg; as shown in Fig.13. This utility is useful for viewing the display from the opposite edge.

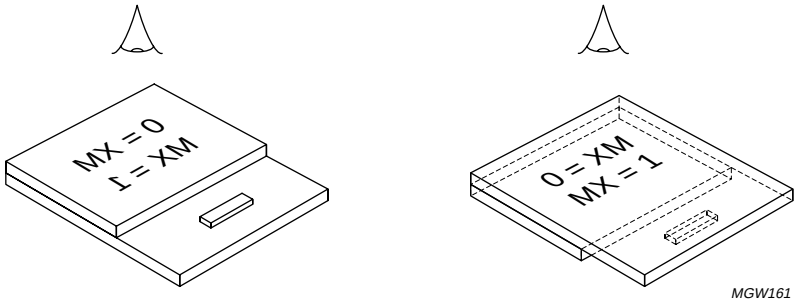


Fig.12 Use of MX bit.

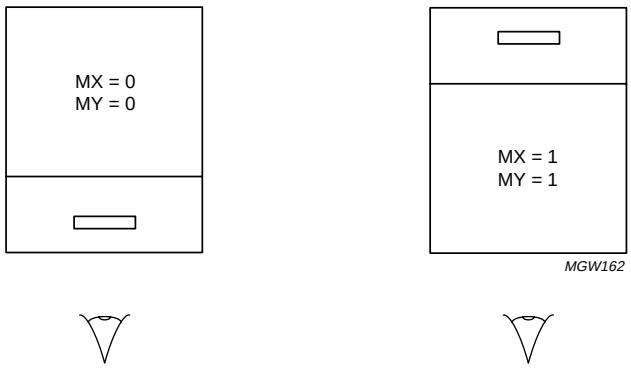


Fig.13 Use of MX and MY bits.

7.15.2 OUTPUT ADDRESSING

The output addressing of the RAM is done automatically in accordance with the currently selected multiplex rate. Normally the user would not need to make any alterations to the addressing. There are, however, circumstances pertaining to various connectivity of the device on a glass that would benefit from some built-in functionality. Three modes exist that enable the user to modify the output addressing:

1. Mirror the Y axis (bit MY). This mode effectively flips the display around the X axis, resulting in an upside down display. The effect is observable immediately the bit is modified. This is useful if the device is to be mounted above the display area instead of below.
2. Bottom Row Swap (BRS). This mode swaps the order of the rows on the bottom(1) edge of the chip. This is useful to aid routing to the display when it is not possible to pass tracks under the device; a typical example would be in tape carrier package. This mode is often used in conjunction with TRS.
3. Top Row Swap (TRS). As with BRS, but swaps the order of rows on the top(1) edge of the chip.

7.15.2.1 Mirror Y

As described above, the Y axis is mirrored in the X axis.

(1) The top edge is defined as the edge containing the user interface pads. The bottom edge is the opposing edge.

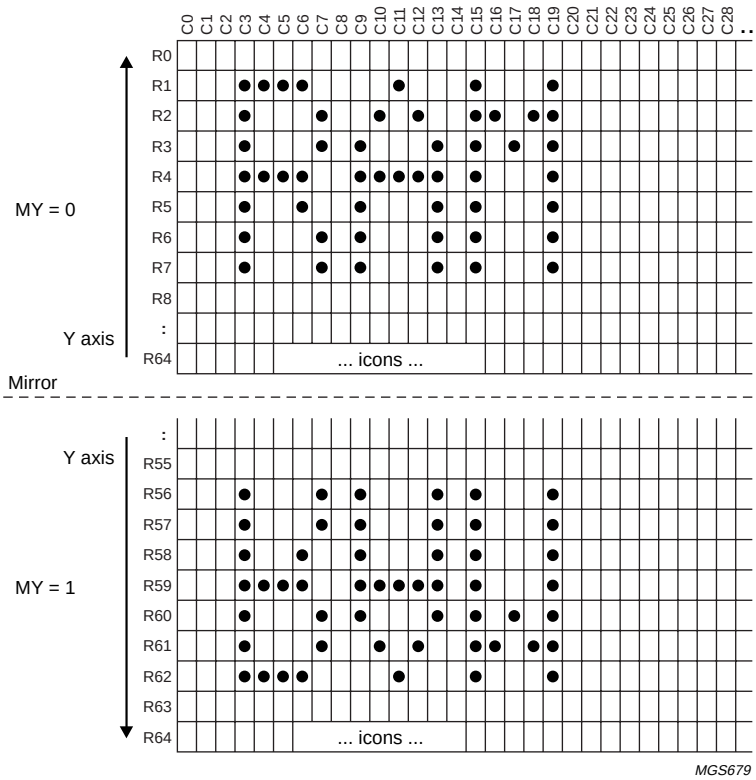


Fig.14 Mirror Y behaviour (Mux rate 1 : 65).

7.15.2.2 Bottom Row Swap

Here the order of the row pads is modified. Each block of rows is swapped around its local Y axis.

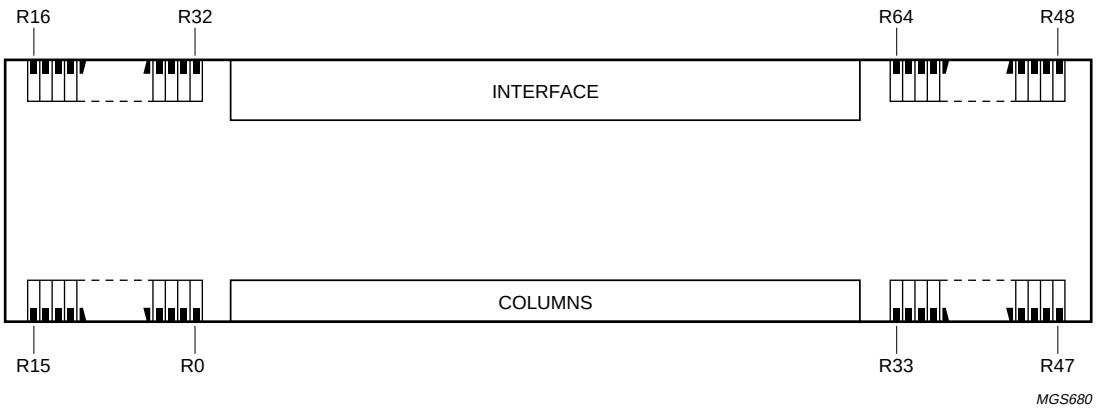


Fig.15 Bottom row swap.

7.15.2.3 Top Row Swap

Here the order of the row pads is modified. Each block of rows is swapped around its local Y axis.

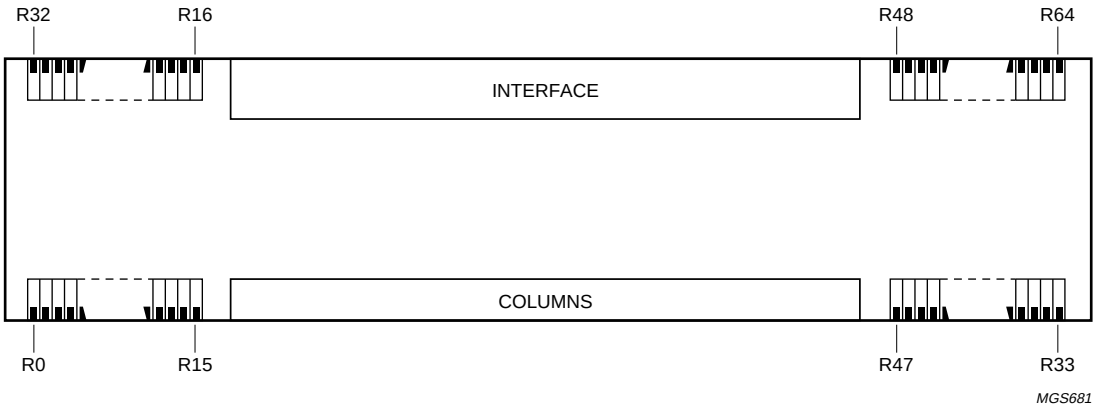


Fig.16 Top row swap.

7.15.2.4 Output row order

The order in which the rows are activated is a function of bits MY, TRS, BRS and the selected multiplex rate. Tables 9 to 12 give the order in which the rows are activated. In all cases, the RAM is accessed in a linear fashion, starting at zero, counting to the last row and then jumping to the end for the icon data. When MY = 1, the RAM is still accessed in a linear fashion but starting from the last row, counting down to zero and then jumping to the icon data.

Table 9 Row order for BRS = 0 and TRS = 0

MULTIPLEX RATE	ROW ACTIVATION	RAM ACCESS (MY = 0)	RAM ACCESS (MY = 1)
1 : 17	R0 to R15 and R64	0 to 15 and 64	15 to 0 and 64
1 : 26	R0 to R24 and R64	0 to 24 and 64	24 to 0 and 64
1 : 34	R0 to R32 and R64	0 to 32 and 64	32 to 0 and 64
1 : 49	R0 to R47 and R64	0 to 47 and 64	47 to 0 and 64
1 : 65	R0 to R64	0 and 64	63 to 0 and 64

Table 10 Row order for BRS = 1 and TRS = 0

MULTIPLEX RATE	ROW ACTIVATION	RAM ACCESS (MY = 0)	RAM ACCESS (MY = 1)
1 : 17	R15 to R0 and R64	0 to 15 and 64	15 to 0 and 64
1 : 26	R15 to R0, R16 to R24 and R64	0 to 24 and 64	24 to 0 and 64
1 : 34	R0 to R32 and R64	0 to 32 and 64	32 to 0 and 64
1 : 49	R15 to R0, R16 to R32, R47 to R33 and R64	0 to 47 and 64	47 to 0 and 64
1 : 65	R15 to R0, R16 to R32, R47 to R33 and R48 to R64	0 and 64	63 to 0 and 64

Table 11 Row order for BRS = 0 and TRS = 1

MULTIPLEX RATE	ROW ACTIVATION	RAM ACCESS (MY = 0)	RAM ACCESS (MY = 1)
1 : 17	R0 to R15 and R48	0 to 15 and 64	15 to 0 and 64
1 : 26	R0 to R15, R32 to R24 and R48	0 to 24 and 64	24 to 0 and 64
1 : 34	R0 to R15, R32 to R16 and R48	0 to 32 and 64	32 to 0 and 64
1 : 49	R0 to R15, R32 to R16, R33 to R47 and R48	0 to 47 and 64	47 to 0 and 64
1 : 65	R0 to R15, R32 to R16, R33 to R47 and R64 to R48	0 and 64	63 to 0 and 64

Table 12 Row order for BRS = 1 and TRS = 1

MULTIPLEX RATE	ROW ACTIVATION	RAM ACCESS (MY = 0)	RAM ACCESS (MY = 1)
1 : 17	R15 to R0 and R48	0 to 15 and 64	15 to 0 and 64
1 : 26	R15 to R0, R32 to R24 and R48	0 to 24 and 64	24 to 0 and 64
1 : 34	R15 to R0, R32 to R16 and R48	0 to 32 and 64	32 to 0 and 64
1 : 49	R15 to R0, R32 to R16, R47 to R33 and R48	0 to 47 and 64	47 to 0 and 64
1 : 65	R15 to R0, R32 to R16, R47 to R33 and R64 to R48	0 and 64	63 to 0 and 64

7.15.2.5 Interconnect possibilities using TRS and BRS

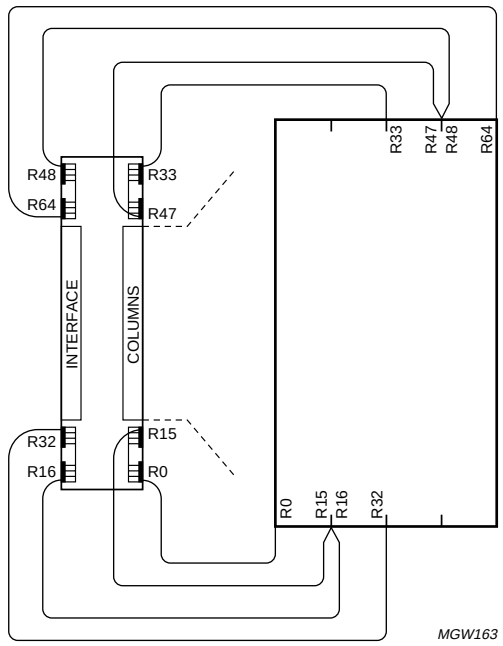


Fig.17 BRS = 0; TRS = 0

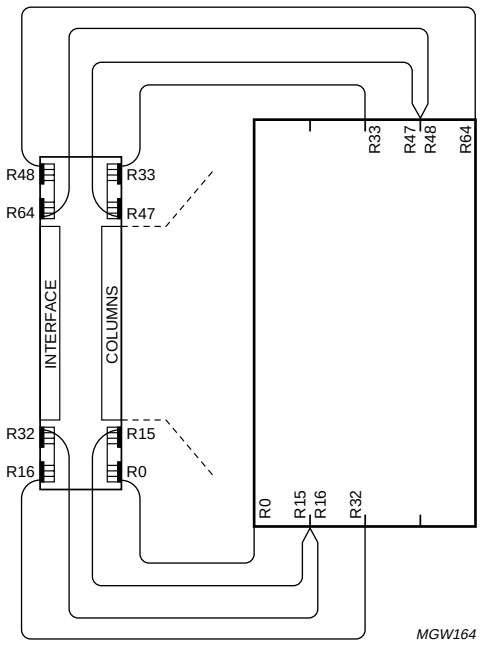


Fig.18 BRS = 0; TRS = 1

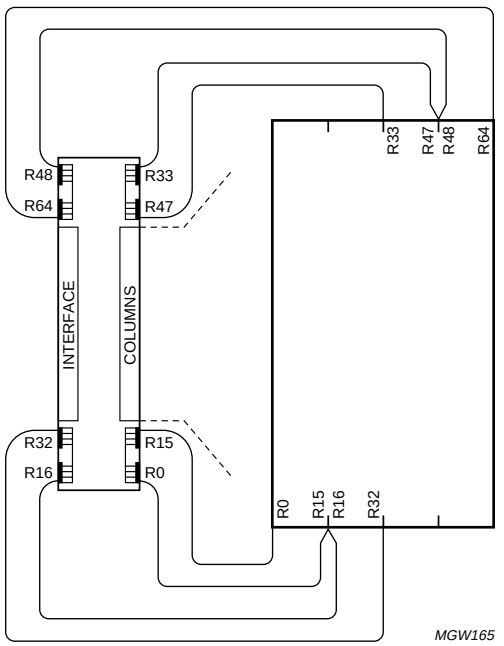


Fig.19 BRS = 1; TRS = 0

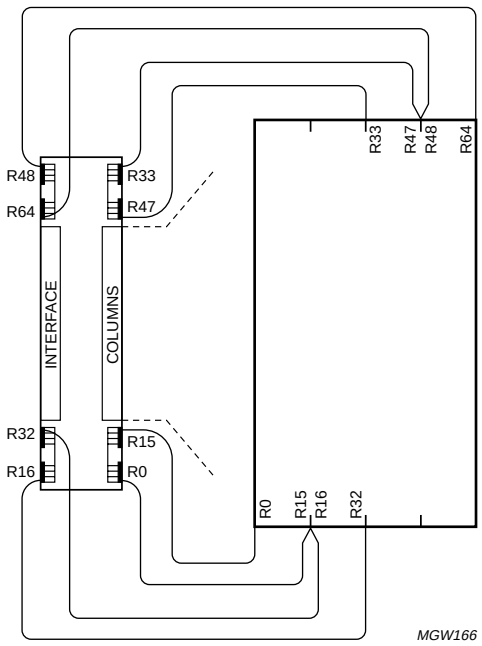


Fig.20 BRS = 1; TRS = 1

7.16 Instruction set

Data accesses to the PCF8535 can be broken down into two areas, those that define the operating mode of the device and those that fill the display RAM; the distinction being the D/$\overline{C}$ bit. When bit D/$\overline{C}$ = 0, the device will respond to instructions as defined in Table 16. When bit D/$\overline{C}$ = 1, the device will store data into the RAM. Data may be written to the device that is independent to the presence of the display clock.

There are 4 instruction types:

1. Define PCF8535 functions such as display configuration, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, type 3 instructions are the most frequently used. To lessen the MPU program load, automatic incrementing by one of the internal RAM address pointers after each data write is implemented.

The instruction set is broken down into several pages, each command page being individually addressed via the H[2:0] bits.

7.16.1 RAM READ/WRITE COMMAND PAGE

This page is special in that it is accessible independently of the H bits. This page is mainly used as a stepping stone to other pages. Sending the 'Default H[2:0]' command will cause an immediate step to the 'Function and RAM command page' which will allow the H[2:0] bits to be set.

7.16.2 FUNCTION AND RAM COMMAND PAGE

7.16.2.1 Command page

Setting H[2:0] will move the user immediately to the required command page. Pages not listed should not be accessed as the behaviour is not defined.

7.16.2.2 Function set

PD

When PD = 1, the LCD driver is in Power-down mode:

- All LCD outputs at V_{SS}
- Oscillator off
- V_{LCDIN} may be disconnected
- I^2C-bus interface accesses are possible
- RAM contents are not cleared; RAM data can be written
- Register settings remain unchanged.

V

When V = 0, horizontal addressing is selected. When V = 1, vertical addressing is selected. The behaviour is described in Section 7.15.

7.16.2.3 RAM page

The XM_0 bit extends the RAM into a second page. The bit may be considered to be the Most Significant Bit (MSB) of an 8-bit X address. The behaviour is described in Section 7.15.

7.16.2.4 Set Y address of RAM

The Y address is used as a pointer to the RAM for RAM writing. The range is 0 to 8. Each bank corresponds to a set of 8 rows; the only exception being bank 8, which contains the icon data and is only 1-bit deep (see Table 13).

Table 13 Y address pointer

Y[3]	Y[2]	Y[1]	Y[0]	BANK	ROWS
0	0	0	0	bank 0	R0 to R7
0	0	0	1	bank 1	R8 to R15
0	0	1	0	bank 2	R16 to R23
0	0	1	1	bank 3	R24 to R31
0	1	0	0	bank 4	R32 to R39
0	1	0	1	bank 5	R40 to R47
0	1	1	0	bank 6	R48 to R55
0	1	1	1	bank 7	R56 to R63
1	0	0	0	bank 8 (icons)	R64

7.16.2.5 Set X address of RAM

The X address is used as a pointer to the RAM for RAM writing. The range of X is 0 to 127 and may be extended by the XM_0 bit. The combined value of XM_0 and X address directly corresponds to the display column number when MX = 0 and corresponds to the inverse display column number when MX = 1 (see Table 14).

Table 14 X address pointer

XM_0, X[6:0]	ADDRESSED COLUMN	
	MX = 0	MX = 1
0	C0	C132
1	C1	C131
2	C2	C130
3	C3	C129
:	:	:
129	C129	C3
130	C130	C2
131	C131	C1
132	C132	C0

7.16.3 DISPLAY SETTING COMMAND PAGE

7.16.3.1 Display control

The D and E bits set the display mode as given in Table 15.

Table 15 Display control

D	E	MODE
0	0	display blank
1	0	normal mode
0	1	all display segments on
1	1	inverse video

7.16.3.2 External display control

Mirror X and mirror Y have the effect of flipping the display left to right or top to bottom respectively. MX works by changing the order data that is written into the RAM. As such, the effects of toggling MX will only be seen after data is written into the RAM. MY works by reversing the order that column data is accessed relative to the row outputs. The effect of toggling MY will be seen immediately. The behaviour of both of these bits is further described in Section 7.15.

7.16.3.3 Bias system

BS[2:0] sets the bias system (see Section 7.10).

7.16.3.4 Display size

Physically large displays require stronger drivers. Bit IB enables the user to select a stronger driving mode and should be used if suitable display quality can not be achieved with the default setting.

7.16.3.5 Multiplex rate

M[2:0] sets the multiplex rate (see Section 7.9).

7.16.4 HV-GEN COMMAND PAGE

7.16.4.1 HV-gen control

PRS

Bit PRS selects the programmable charge pump range select. This bit defines whether the programmed voltage for V_{OP} is in the LOW or the HIGH range. The behaviour of this bit is further described in Section 7.13.

HVE

Bit HVE enables the high voltage generator. When set to logic 0, the charge pump is disabled. When set to logic 1, the charge pump is enabled.

7.16.4.2 HV-gen stages

S[1:0] set the multiplication factor of the charge pump ranging from times 2 to times 5. The behaviour of these bits is further described in Section 7.14.

7.16.4.3 Temperature coefficients

TC[2:0] set the required temperature coefficient. The behaviour of these bits is further described in Section 7.12.

7.16.4.4 Temperature measurement control

The SM bit is used to initiate a temperature measurement. The SM bit is automatically cleared at the end of the measurement. The behaviour of this bit is further described in Section 7.11.

7.16.4.5 V_{LCD} control

V_{OP}[6:0] sets the required operating voltage for the display.

7.16.5 SPECIAL FEATURE COMMAND PAGE

7.16.5.1 State control

DM

Direct mode allows V_{LCDOUT} to be sourced directly from V_{DD2}. This may be useful in systems where V_{DD} is to be used for V_{LCD}.

DOF

Display off will turn off all internal analog circuitry that is not required for temperature measurement.
As a consequence the display will be turned off. This mode is only required if temperature measurements are required whilst in Power-down mode.

7.16.5.2 Oscillator setting

The internal oscillator may be disabled and the source clock for the display is derived from the OSC pad. It is important to remember that LCDs are damaged by DC voltages and that the clock, whether derived internally or externally, should never be disabled whilst the display is active. The internal oscillator is switched off during power-down mode.

Using an external clock and disabling it during power-down mode will further reduce the standby current. If it is not possible to disable it externally, then it is worth noting that by selecting the internal clock, which is disabled during power-down mode, the same effect may be achieved.

7.16.5.3 COG/TCP

The chip may be mounted on either a glass, foil or tape carrier package. For these applications, different organizations of the row pads are required to negate the necessity of routing tracks under the device. The TRS and BRS allow for this swapping. The behaviour of both of these bits is further described in Section 7.15.

7.16.6 INSTRUCTION SET

Table 16 Instruction set

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$(1)	I²C-BUS COMMAND BYTE								I²C-BUS COMMANDS
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
H[2:0] = XXX; RAM read/write command page											
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	write data to display RAM
Read status	0	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	return result of temperature measurement
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Default H[2:0]	0	0	0	0	0	0	0	0	0	1	jump to H[2:0] = 111
H[2:0] = 111; function and RAM command page											
Command page	0	0	0	0	0	0	1	H_2	H_1	H_0	select command page
Function set	0	0	0	0	0	1	0	PD	V	0	power-down control, data entry mode
RAM page	0	0	0	0	1	0	0	XM_0	0	0	set RAM page for X address
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	set Y address of RAM $0 \leq Y \leq 8$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	set X address of RAM $0 \leq X \leq 127$
H[2:0] = 110; display setting command page											
Display control	0	0	0	0	0	0	0	1	D	E	set display mode
External display control	0	0	0	0	0	0	1	MX	MY	0	mirror X, mirror Y
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	set bias system

INSTRUCTION	D/$\overline{C}$	R/$\overline{W}$(1)	I²C-BUS COMMAND BYTE								I²C-BUS COMMANDS
			DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display size	0	0	0	0	1	0	0	IB	0	0	set current for bias system
Multiplex rate	0	0	1	0	0	0	0	M_2	M_1	M_0	set multiplex rate
H[2:0] = 101; HV-gen command page											
HV-gen control	0	0	0	0	0	0	0	1	PRS	HVE	select V_{LCD} programming range, enable/disable HV-gen
HV-gen stages	0	0	0	0	0	0	1	0	S_1	S_0	select HV-gen voltage multiplication factor
Temperature coefficients	0	0	0	0	0	1	0	TC2	TC1	TC0	set temperature coefficient
Temperature measurement control	0	0	0	0	1	0	0	0	0	SM	start temperature measurement
V_{LCD} control	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	set V_{LCD} register $0 \leq V_{LCD} \leq 127$
H[2:0] = 011; special feature command page											
State control	0	0	0	0	0	0	0	1	DOF	DM	display off, direct mode
Oscillator setting	0	0	0	0	0	0	1	0	EC	0	enable/disable the internal oscillator
COG/TCP	0	0	0	1	0	TRS	BRS	0	0	0	top row swap, bottom row swap

Note

1. R/$\overline{W}$ is set in the slave address.

Table 17 Description of the symbols used in Table 16

BIT	0	1
PD	chip is active	chip is in power-down mode
V	horizontal addressing	vertical addressing
HVE	voltage multiplier disabled	voltage multiplier enabled
PRS	V_{LCD} programming range LOW	V_{LCD} programming range HIGH
SM	no measurement	start measurement
MX	no X mirror	mirror X
MY	no Y mirror	mirror Y
TRS	top row swap inactive	top row swap active
BRS	bottom row swap inactive	bottom row swap active
EC	internal oscillator enabled; OSC pad ignored	internal oscillator disabled; OSC pad enabled for input
DM[1]	direct mode disabled	direct mode enabled
DOF[1]	display off mode disabled	display off mode enabled
IB	low current mode for smaller displays	high current mode for larger displays

Note

1. Conditional on other bits.

Table 18 Priority behaviour of bits PD, DOF, HVE and DM; note 1

PD	DOF	HVE	DM	MODE
1	X	X	X	chip is in power-down mode as defined under PD
0	1	X	X	all analog blocks except those required for temperature measurement are off
0	0	1	X	chip is active and using the internal V_{LCD} generator
0	0	0	1	chip is active and using V_{DD} as V_{LCD}
0	0	0	0	chip is active and using an external supply voltage attached to V_{LCDIN}

Note

1. X = don’t care state.

7.17 I²C-bus interface

7.17.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

7.17.1.1 Bit transfer

One data bit is transferred during each clock pulse.
The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.
Bit transfer is illustrated in Fig.21.

7.17.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S).
A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.22.

7.17.1.3 System configuration

The system configuration is illustrated in Fig.23:

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

7.17.1.4 Acknowledge

Each byte of 8 bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C-bus is illustrated in Fig.24.

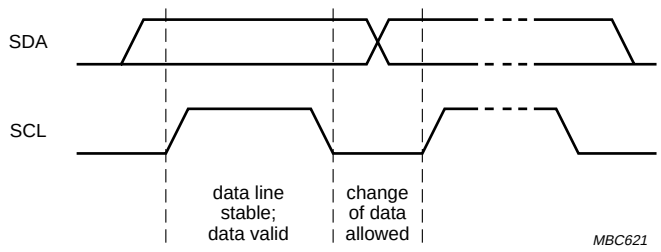


Fig.21 Bit transfer.

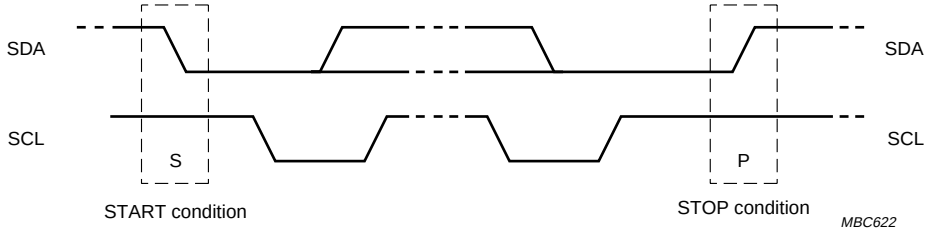


Fig.22 Definition of START and STOP conditions.

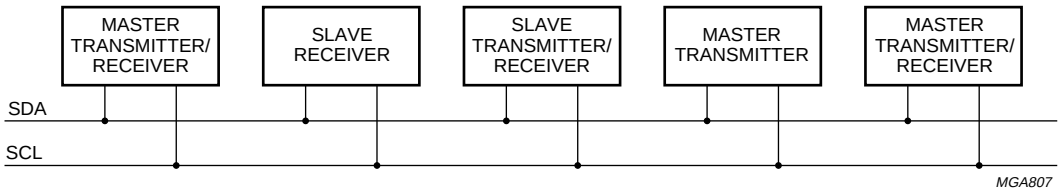


Fig.23 System configuration.

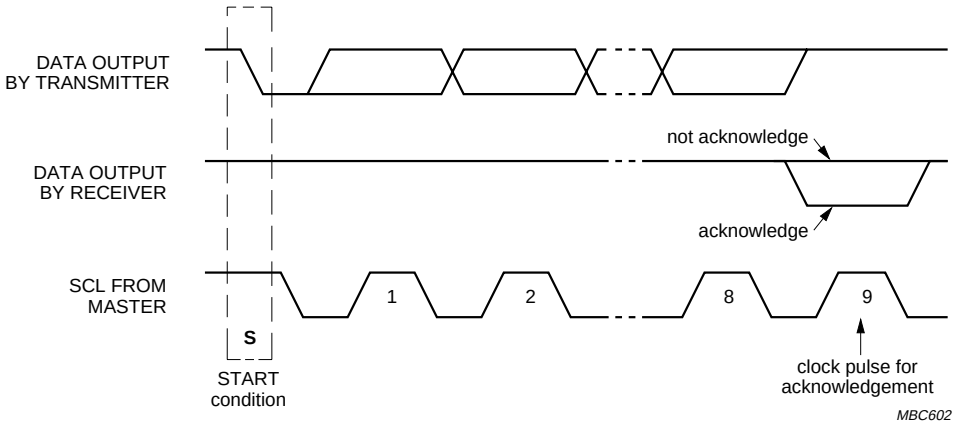


Fig.24 Acknowledgement on the I^2C-bus.

7.17.2 I²C-BUS PROTOCOL

The PCF8535 is a slave receiver/transmitter. If data is to be read from the device the SDAOUT pad must be connected, otherwise SDAOUT is unused.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed. Four slave addresses, 0111100, 0111101, 0111110 and 0111111 are reserved for the PCF8535. The Least Significant Bits (LSBs) of the slave address is set by connecting SA1 and SA0 to either logic 0 (V_{SS}) or logic 1 (V_{DD}).

A sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

After the acknowledgement cycle of a write, a control byte follows which defines the destination for the forthcoming data byte and the mode for subsequent bytes. For a read, the PCF8535 will immediately start to output the requested data until a NOT acknowledge is transmitted by the master. The sequence should be terminated by a STOP in the event that no further access is required for the time being, or by a RE-START should further access be required.

For ease of operation a continuation bit Co has been included. This bit allows the user to set-up the chip configuration and transmit RAM data in one access. A data selection bit, D/$\overline{C}$, defines the destination for data. These bits are contained in the control byte. DB5 to DB0 should be set to logic 0. These bits are reserved for future expansion.

An example of a write access is given in Fig.25. Here, multiple instruction data is sent, followed by multiple display bytes.

An example of a read access is given in Fig.26.

Table 19 Co and D/$\overline{C}$ definitions

BIT	VALUE	R/$\overline{W}$	ACTION
Co	0	n.a.	last control byte to be sent and only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or RE-START condition
	1	n.a.	another control byte will follow the data byte unless a STOP or RE-START condition is received
D/$\overline{C}$	0	0	data byte will be decoded and used to set up the device
		1	data byte will return the contents of the currently selected status register
	1	0	data byte will be stored in the display RAM
		1	no provision for RAM read back is provided

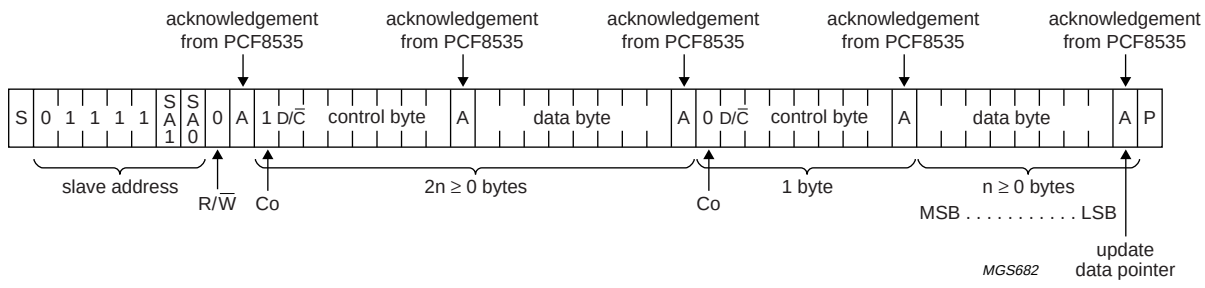


Fig.25 Master transmits to slave receiver; write mode.

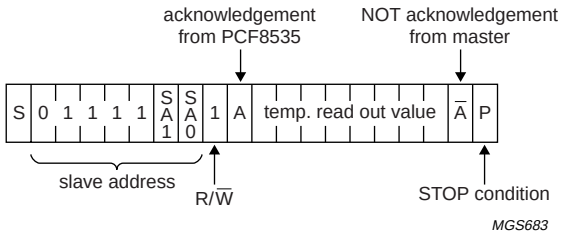


Fig.26 Master reads a slaves' status register.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); notes 1, 2 and 3.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7.0	V
I_{DD}	supply current	–50	+50	mA
V_{LCD}	LCD supply voltage	–0.5	+17.0	V
I_{LCD}	LCD supply current	–50	+50	mA
I_{SS}	negative supply current	–50	+50	mA
V_I	input voltage (any input)	–0.5	V_{DD} + 0.5	V
V_O	output voltage (any output)	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation per package	–	300	mW
P/out	power dissipation per output	–	30	mW
T_{amb}	ambient temperature	–40	+85	°C
T_{stg}	storage temperature	–65	+150	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

Notes

1. Stresses above these values listed may cause permanent damage to the device.
2. Parameters are valid over the operating temperature range unless otherwise specified. All voltages are referenced to V_{SS} unless otherwise specified.
3. V_{SS} = 0 V.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

10 DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 16.0 V; T_{amb} = –40 to +85 °C; all voltages referenced to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{LCDIN}	LCD supply voltage	all Mux modes	4.5	–	16.0	V
I_{LCDIN}	I_{LCD}; LCD supply current	power-down; note 1	–	0	10	µA
		display active; Mux 1:65, bias 1/9; V_{LCDIN} = 12 V; notes 1 and 2	–	63	125	µA
		display active; Mux 1:17, bias 1/5; V_{LCDIN} = 5 V; notes 1 and 2	–	44	88	µA
V_{LCDOUT}	generated LCD supply voltage	LCD voltage generator enabled	–	–	16.0	V
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	I_{DD}; V_{DD} supply current	power-down; note 1	–	2	10	µA
		display active; V_{LCDIN} = 12 V; Mux 1:65, bias 1/9; notes 1 and 2	–	30	60	µA
		display active; V_{LCDOUT} = 12 V; times 3 multiplier; Mux 1:65; bias 1/9; notes 1 and 2	–	315	630	µA
		display active; V_{LCDIN} = 5 V; Mux 1:17; bias 1/5; notes 1 and 2	–	22	45	µA
		display active; direct mode; Mux 1:17, bias 1/5; notes 1 and 2	–	95	190	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL}	LOW-level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3.0	–	–	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
Column and row outputs						
$R_{o(col)}$	column output resistance C0 to C132	V_{LCD} = 12 V; note 3	–	–	10	kΩ
$R_{o(row)}$	row output resistance R0 to R64	V_{LCD} = 12 V; note 3	–	–	3.0	kΩ
$V_{bias(col)}$	bias tolerance C0 to C132		–100	0	+100	mV
$V_{bias(row)}$	bias tolerance R0 to R64		–100	0	+100	mV
LCD supply voltage generator						
$V_{LCD(tol)}$	V_{LCD} tolerance (internal V_{LCD})	T_{amb} = –20 to +85 °C; $V_{LCD} \leq 12$ V	–	–	4.6	%
Temperature coefficient						
T_{cut}	cut point temperature		–	27	–	°C

Notes

1. LCD outputs are open-circuit, inputs at V_{DD} or V_{SS}, bus inactive, f_{OSC} = typical internal oscillator frequency.
2. Conditions are: V_{DD1} to V_{DD3} = 5.0 V; IB = 0; D = 1; E = 0; internal oscillator and RAM contains all 0s.
3. I_{LCD} = 10 µA. Outputs tested one at a time.

11 AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 16.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequencies						
$f_{fr(LCD)}$	LCD frame frequency (internal clock)		48	80	165	Hz
$f_{clk(ext)}$	external clock frequency	see Table 20	120	–	410	kHz
Reset tuning (see Fig.28)						
$t_{W(RESL)}$	reset LOW pulse width		1	–	–	µs
$t_{W(RESH)}$	reset HIGH pulse width		5	–	–	µs
$t_{SU;RESL}$	reset LOW pulse set-up time after power-on	notes 1 and 2	–	–	30	µs
$t_{R(op)}$	end of reset pulse to interface being operational		–	–	3	µs
Serial-bus interface; note 3 (see Fig.27)						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
t_r	rise time SDA and SCL	note 4	$20 + 0.1C_b$	–	300	ns
t_f	fall time SDA and SCL	note 4	$20 + 0.1C_b$	–	300	ns
C_b	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	set-up time repeated START		0.6	–	–	µs
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs
t_{SP}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	bus free time (between a STOP and START condition)		1.3	–	–	µs

Notes

1. V_{DD1} to V_{DD3} = 5 V.
2. Decoupling capacitor on V_{LCD} and V_{SS} is 100 nF (higher capacitor value increases $t_{SU;RESL}$ and higher V_{DD1} to V_{DD3} reduces $t_{SU;RESL}$).
3. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
4. C_b is total capacitance of one bus line in pF.

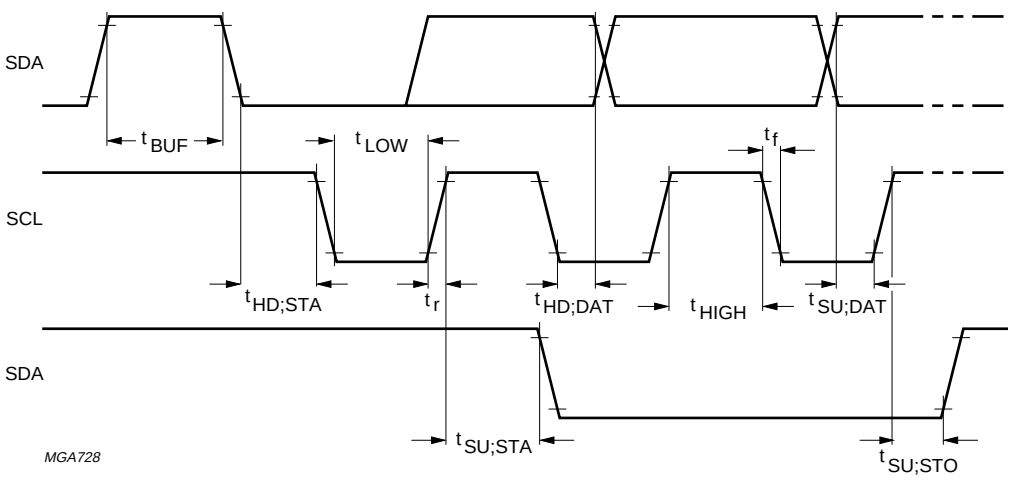


Fig.27 I^2C-bus timing diagram.

Table 20 External clock frequency for an 80 Hz frame frequency

MUX MODE	DIVISION RATIO	EXTERNAL CLOCK FREQUENCY
1 : 65	3168	253 kHz
1 : 48	3136	251 kHz
1 : 34	2720	218 kHz
1 : 26	2592	207 kHz
1 : 17	2592	207 kHz

12 RESET TIMING

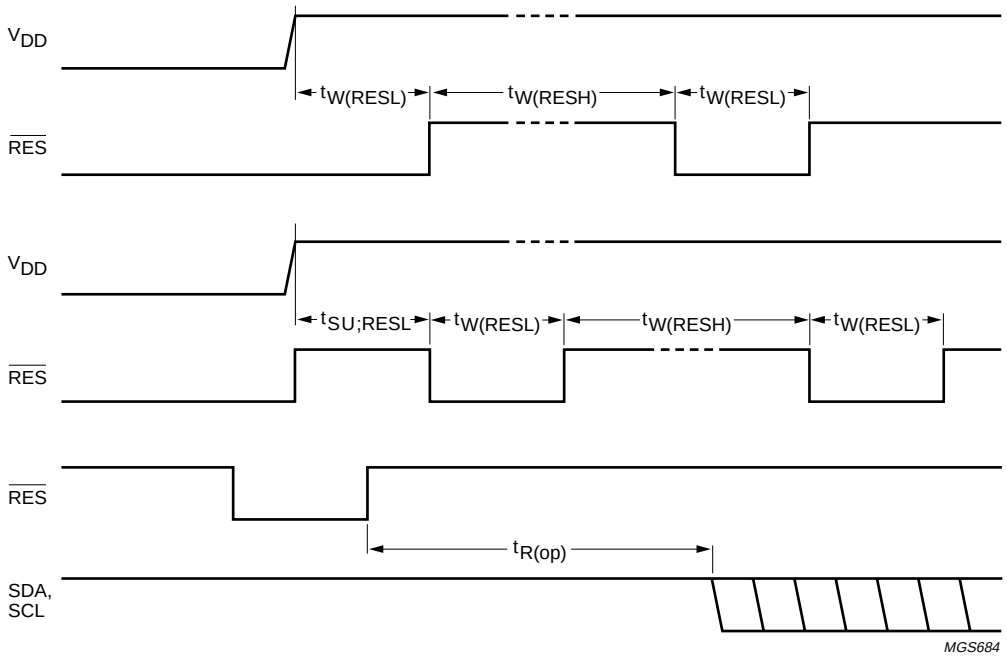
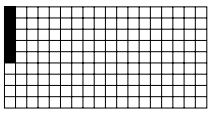
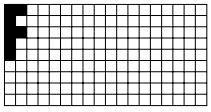
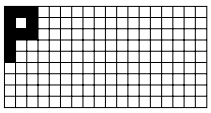
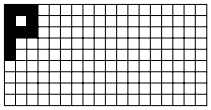
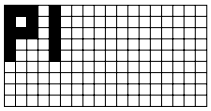
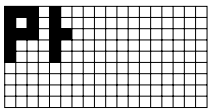
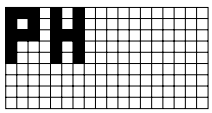
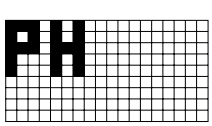


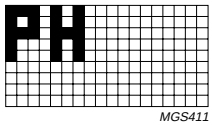
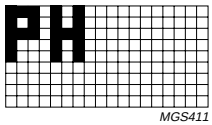
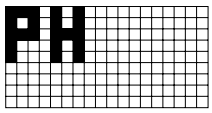
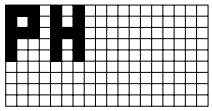
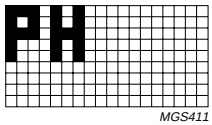
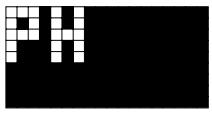
Fig.28 Reset timing.

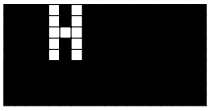
13 APPLICATION INFORMATION

Table 21 Programming example for PCF8535

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
1	START condition								BLANK	start
2	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	slave address, R/$\overline{W}$ = 0
	0	1	1	1	1	SA1	SA0	0		
3	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	control byte, Co = 0, D/$\overline{C}$ = 0
	0	0	0	0	0	0	0	0		
4	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	H[2:0] independent command; select function and RAM command page H[1:0] = 111
	0	0	0	0	0	0	0	1		
5	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	function and RAM command page; PD = 0, V = 0
	0	0	0	1	0	0	0	0		
6	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	function and RAM command page; select display setting command page H[1:0] = 110
	0	0	0	0	1	1	1	0		
7	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	display setting command page; set bias system to $^1/_9$ (BS[2:0] = 010)
	0	0	0	1	0	0	1	0		
8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	display setting command page; set normal mode (D = 1, E = 0)
	0	0	0	0	0	1	1	0		
9	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	select Mux rate 1 : 65
	1	0	0	0	0	1	0	0		
10	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	H[2:0] independent command; select function and RAM command page H[1:0] = 111
	0	0	0	0	0	0	0	1		
11	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	function and RAM command page; select HV-gen command page H[2:0] = 101
	0	0	0	0	1	1	0	1		
12	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	HV-gen command page; select voltage multiplication factor 3 S[1:0] = 01
	0	0	0	0	1	0	0	1		
13	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	HV-gen command page; select temperature coefficient 2 TC[2:0] = 010
	0	0	0	1	0	0	1	0		
14	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	HV-gen command page; set V_{LCD} = 12.02 V; V_{OP}[6:0] = 0101000
	1	0	1	0	1	0	0	0		
15	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	HV-gen command page; select HIGH V_{LCD} programming range (PRS = 1), voltage multiplier on (HVE = 1)
	0	0	0	0	0	1	1	1		
16	START condition								BLANK	repeat start
17	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	slave address, R/$\overline{W}$ = 0
	0	1	1	1	1	SA1	SA0	0		

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
18	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BLANK	control byte, Co = 0, D/$\overline{C}$ = 1
	0	1	0	0	0	0	0	0		
19	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS405	data write; Y, X are initialized to logic 0 by default, so they are not set here
	0	0	0	1	1	1	1	1		
20	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS406	data write
	0	0	0	0	0	1	0	1		
21	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS407	data write
	0	0	0	0	0	1	1	1		
22	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS408	data write
	0	0	0	0	0	0	0	0		
23	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS409	data write
	0	0	0	1	1	1	1	1		
24	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS410	data write
	0	0	0	0	0	1	0	0		
25	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	data write, last data, stop transmission
	0	0	0	1	1	1	1	1		
26	START condition									repeat start
27	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	slave address, R/$\overline{W}$ = 0
	0	1	1	1	1	SA1	SA0	0		

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
28	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	control byte, Co = 1, D/$\overline{C}$ = 0
	1	0	0	0	0	0	0	0		
29	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	H[2:0] independent command; select function and RAM command page H[2:0] = 111
	0	0	0	0	0	0	0	0		
30	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	control byte, Co = 1, D/$\overline{C}$ = 0 function and RAM command page; select display setting command page H[2:0] = 110
	1	0	0	0	0	0	0	0		
31	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	
	0	0	0	0	1	1	1	0		
32	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS411	control byte, Co = 1, D/$\overline{C}$ = 0
	1	0	0	0	0	0	0	0		
33	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS412	display control; set inverse video mode (D = 1, E = 1)
	0	0	0	0	1	1	0	1		
34	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS412	control byte, Co = 1, D/$\overline{C}$ = 0
	1	0	0	0	0	0	0	0		
35	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS412	set X address of RAM; set address to ‘0000000’
	1	0	0	0	0	0	0	0		

STEP	SERIAL BUS BYTE								DISPLAY(1)	OPERATION
36	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS412	control byte, Co = 0, D/$\overline{C}$ = 1
	0	1	0	0	0	0	0	0		
37	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS414	data write
	0	0	0	0	0	0	0	0		
38	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS685	data write
	0	0	0	0	0	0	0	0		
39	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	 MGS686	data write
	0	0	0	0	0	0	0	0		
40	STOP condition									end of transfer

Note

1. Assumes the display RAM was previously empty.

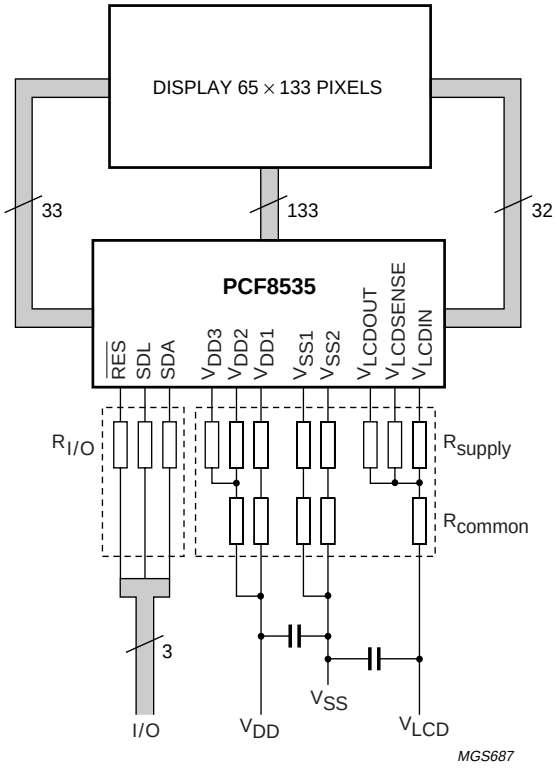


Fig.29 Application diagram (COG).

13.1 Application for chip-on-glass

The pinning of the PCF8535 is optimized for single plane wiring e.g. for chip-on-glass display modules.

The required minimum value for the external capacitors in an application with the PCF8535 are:

Between V_{LCD} and V_{SS} is 100 nF (min.) (recommended 470 nF to 1 µF): Between V_{DD} and V_{SS} is 470 nF (recommended capacitor larger than the capacitor between V_{LCD} and V_{SS}).

Higher capacitor values are recommended for ripple reduction.

For COG applications the recommended ITO track resistance is to be minimized for the I/O and supply connections. Maximum resistance for supply tracks (R_{supply}) are 120 Ω. Maximum values for the common resistance to the source (R_{common}) are 120 Ω. Higher track resistance reduces performance and increases current consumption.

Three I/O lines are required for the COG module: SDA, SCL and $\overline{RES}$ (optional). Other signals may be fixed on the module to appropriate levels. $R_{I/O}$ should also be minimized. In particular, if the I^2C-bus acknowledge or temperature read back is required, the $R_{I/O}$ for the SDA line must be carefully considered in conjunction with the value of the external pull-up resistor.

Inputs SA0, SA1, OSC, T4, T5 and $\overline{RES}$ are CMOS inputs and hence may be routed to V_{SS} or V_{DD} using relatively high track impedances e.g. up to 100 kΩ.

14 BONDING PAD LOCATIONS

Table 22 Bonding pad locations

All x and y coordinates are referenced to the centre of the chip (dimensions in μm; see Fig.33).

SYMBOL	PAD	x	y
dummy	1	+1050	−6156
bump/align 1	2	+1050	−6081
R0	3	+1050	−5985
R1	4	+1050	−5915
R2	5	+1050	−5845
R3	6	+1050	−5775
R4	7	+1050	−5705
R5	8	+1050	−5635
R6	9	+1050	−5565
R7	10	+1050	−5495
R8	11	+1050	−5425
R9	12	+1050	−5355
R10	13	+1050	−5285
R11	14	+1050	−5215
R12	15	+1050	−5145
R13	16	+1050	−5075
R14	17	+1050	−5005
R15	18	+1050	−4935
C0	19	+1050	−4725
C1	20	+1050	−4655
C2	21	+1050	−4585
C3	22	+1050	−4515
C4	23	+1050	−4445
C5	24	+1050	−4305
C6	25	+1050	−4235
C7	26	+1050	−4165
C8	27	+1050	−4095
C9	28	+1050	−4025
C10	29	+1050	−3955
C11	30	+1050	−3885
C12	31	+1050	−3815
C13	32	+1050	−3745
C14	33	+1050	−3675
C15	34	+1050	−3605
C16	35	+1050	−3535
C17	36	+1050	−3465
C18	37	+1050	−3395
C19	38	+1050	−3325
C20	39	+1050	−3255
C21	40	+1050	−3185
C22	41	+1050	−3115
C23	42	+1050	−3045
C24	43	+1050	−2975
C25	44	+1050	−2905
C26	45	+1050	−2835
C27	46	+1050	−2765
C28	47	+1050	−2695
C29	48	+1050	−2625
C30	49	+1050	−2555
C31	50	+1050	−2485
C32	51	+1050	−2415
C33	52	+1050	−2345
C34	53	+1050	−2275
C35	54	+1050	−2205
C36	55	+1050	−2135
C37	56	+1050	−1995
C38	57	+1050	−1925
C39	58	+1050	−1855
C40	59	+1050	−1785
C41	60	+1050	−1715
C42	61	+1050	−1645
C43	62	+1050	−1575
C44	63	+1050	−1505
C45	64	+1050	−1435
C46	65	+1050	−1365
C47	66	+1050	−1295
C48	67	+1050	−1225
C49	68	+1050	−1155
C50	69	+1050	−1085
C51	70	+1050	−1015
C52	71	+1050	−945
C53	72	+1050	−875
C54	73	+1050	−805
C55	74	+1050	−735
C56	75	+1050	−665
C57	76	+1050	−595
C58	77	+1050	−525
C59	78	+1050	−455

SYMBOL	PAD	x	y
C60	79	+1050	−385
C61	80	+1050	−315
C62	81	+1050	−245
C63	82	+1050	−175
C64	83	+1050	−105
C65	84	+1050	−35
C66	85	+1050	+35
C67	86	+1050	+105
C68	87	+1050	+175
C69	88	+1050	+315
C70	89	+1050	+385
C71	90	+1050	+455
C72	91	+1050	+525
C73	92	+1050	+595
C74	93	+1050	+665
C75	94	+1050	+735
C76	95	+1050	+805
C77	96	+1050	+875
C78	97	+1050	+945
C79	98	+1050	+1015
C80	99	+1050	+1085
C81	100	+1050	+1155
C82	101	+1050	+1225
C83	102	+1050	+1295
C84	103	+1050	+1365
C85	104	+1050	+1435
C86	105	+1050	+1505
C87	106	+1050	+1575
C88	107	+1050	+1645
C89	108	+1050	+1715
C90	109	+1050	+1785
C91	110	+1050	+1855
C92	111	+1050	+1925
C93	112	+1050	+1995
C94	113	+1050	+2065
C95	114	+1050	+2135
C96	115	+1050	+2205
C97	116	+1050	+2275
C98	117	+1050	+2345
C99	118	+1050	+2415
C100	119	+1050	+2485

SYMBOL	PAD	x	y
C101	120	+1050	+2625
C102	121	+1050	+2695
C103	122	+1050	+2765
C104	123	+1050	+2835
C105	124	+1050	+2905
C106	125	+1050	+2975
C107	126	+1050	+3045
C108	127	+1050	+3115
C109	128	+1050	+3185
C110	129	+1050	+3255
C111	130	+1050	+3325
C112	131	+1050	+3395
C113	132	+1050	+3465
C114	133	+1050	+3535
C115	134	+1050	+3605
C116	135	+1050	+3675
C117	136	+1050	+3745
C118	137	+1050	+3815
C119	138	+1050	+3885
C120	139	+1050	+3955
C121	140	+1050	+4025
C122	141	+1050	+4095
C123	142	+1050	+4165
C124	143	+1050	+4235
C125	144	+1050	+4305
C126	145	+1050	+4375
C127	146	+1050	+4445
C128	147	+1050	+4515
C129	148	+1050	+4585
C130	149	+1050	+4655
C131	150	+1050	+4725
C132	151	+1050	+4795
R47	152	+1050	+5005
R46	153	+1050	+5075
R45	154	+1050	+5145
R44	155	+1050	+5215
R43	156	+1050	+5285
R42	157	+1050	+5355
R41	158	+1050	+5425
R40	159	+1050	+5495
R39	160	+1050	+5565

SYMBOL	PAD	x	y
R38	161	+1050	+5635
R37	162	+1050	+5705
R36	163	+1050	+5775
R35	164	+1050	+5845
R34	165	+1050	+5915
R33	166	+1050	+5985
bump/align 2	167	+1050	+6081
dummy	168	−1050	+6094
R48	169	−1050	+5954
R49	170	−1050	+5884
R50	171	−1050	+5814
R51	172	−1050	+5744
R52	173	−1050	+5674
R53	174	−1050	+5604
R54	175	−1050	+5534
R55	176	−1050	+5464
R56	177	−1050	+5394
R57	178	−1050	+5324
R58	179	−1050	+5254
R59	180	−1050	+5184
R60	181	−1050	+5114
R61	182	−1050	+5044
R62	183	−1050	+4974
R63	184	−1050	+4904
R64	185	−1050	+4834
bump/align 3	186	−1050	+4414
dummy	187	−1050	+4274
dummy	188	−1050	+3996
dummy	189	−1050	+3574
OSC	190	−1050	+3154
V_{LCDIN}	191	−1050	+2874
V_{LCDIN}	192	−1050	+2804
V_{LCDIN}	193	−1050	+2734
V_{LCDIN}	194	−1050	+2664
V_{LCDIN}	195	−1050	+2594
V_{LCDIN}	196	−1050	+2524
V_{LCDOUT}	197	−1050	+2384
V_{LCDOUT}	198	−1050	+2314
V_{LCDOUT}	199	−1050	+2244
V_{LCDOUT}	200	−1050	+2174
V_{LCDOUT}	201	−1050	+2104

SYMBOL	PAD	x	y
V_{LCDOUT}	202	−1050	+2034
V_{LCDOUT}	203	−1050	+1964
$V_{LCDSENCE}$	204	−1050	+1894
dummy	205	−1050	+1544
dummy	206	−1050	+1264
$\overline{RES}$	207	−1050	+914
T3	208	−1050	+704
T2	209	−1050	+494
T1	210	−1050	+284
V_{DD2}	211	−1050	+144
V_{DD2}	212	−1050	+74
V_{DD2}	213	−1050	+4
V_{DD2}	214	−1050	−66
V_{DD2}	215	−1050	−136
V_{DD2}	216	−1050	−206
V_{DD2}	217	−1050	−276
V_{DD2}	218	−1050	−346
V_{DD3}	219	−1050	−416
V_{DD3}	220	−1050	−486
V_{DD3}	221	−1050	−556
V_{DD3}	222	−1050	−626
V_{DD1}	223	−1050	−696
V_{DD1}	224	−1050	−766
V_{DD1}	225	−1050	−836
V_{DD1}	226	−1050	−906
V_{DD1}	227	−1050	−976
V_{DD1}	228	−1050	−1046
dummy	229	−1050	−1186
SDA	230	−1050	−1466
SDA	231	−1050	−1536
SDAOUT	232	−1050	−1886
SA1	233	−1050	−2166
SA0	234	−1050	−2376
V_{SS2}	235	−1050	−2586
V_{SS2}	236	−1050	−2656
V_{SS2}	237	−1050	−2726
V_{SS2}	238	−1050	−2796
V_{SS2}	239	−1050	−2866
V_{SS2}	240	−1050	−2936
V_{SS2}	241	−1050	−3006
V_{SS2}	242	−1050	−3076

SYMBOL	PAD	x	y
V_{SS1}	243	−1050	−3146
V_{SS1}	244	−1050	−3216
V_{SS1}	245	−1050	−3286
V_{SS1}	246	−1050	−3356
V_{SS1}	247	−1050	−3426
V_{SS1}	248	−1050	−3496
V_{SS1}	249	−1050	−3566
V_{SS1}	250	−1050	−3636
T5	251	−1050	−3846
T4	252	−1050	−4056
dummy	253	−1050	−4126
SCL	254	−1050	−4406
SCL	255	−1050	−4476
bump/align 4	256	−1050	−4605
R32	257	−1050	−4826
R31	258	−1050	−4896
R30	259	−1050	−4966
R29	260	−1050	−5036
R28	261	−1050	−5106
R27	262	−1050	−5176
R26	263	−1050	−5246
R25	264	−1050	−5316
R24	265	−1050	−5386
R23	266	−1050	−5456
R22	267	−1050	−5526
R21	268	−1050	−5596
R20	269	−1050	−5666
R19	270	−1050	−5736
R18	271	−1050	−5806
R17	272	−1050	−5876
R16	273	−1050	−5946

Table 23 Alignment marks

MARKS	x	y
Alignment mark 1	−1045	−4720
Alignment mark 2	−1045	+4620
Alignment mark 3	+1045	+6196
Alignment mark 4	+1045	−6196
Dummy bump/alignment mark 1	+1050	−6081
Dummy bump/alignment mark 2	+1050	+6081
Dummy bump/alignment mark 3	−1050	+4414
Dummy bump/alignment mark 4	−1050	−4605
Bottom left	−1180	−6330
Top right	+1180	+6330

Table 24 Dimensions

PAD	SIZE	UNIT
Pad pitch	minimum 70 (see Fig.32)	μm
Pad size; Al	62 × 100 (see Fig.32)	μm
CBB opening	36 × 76 (see Fig.32)	μm
Bump dimensions	50 × 90 × 17.5 (± 5)	μm
Wafer thickness	381 ± 25	μm
Alignment mark	ϕ100 (see Fig.30)	μm
Dummy/alignment mark	ϕ80 (see Fig.31)	μm
Wafer dimensions	12.660 x 2360 (see Fig.32)	μm

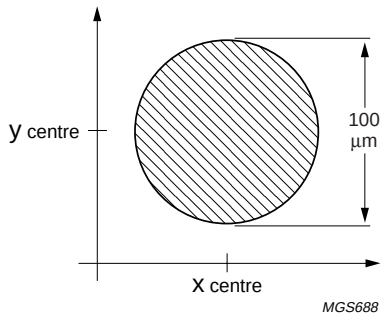


Fig.30 Shape of alignment mark.

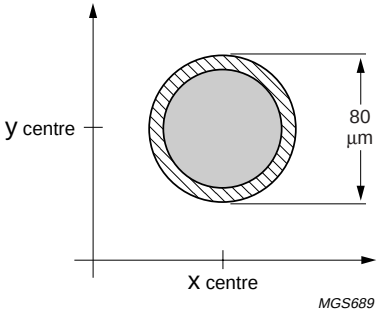


Fig.31 Shape of dummy bump/alignment mark.

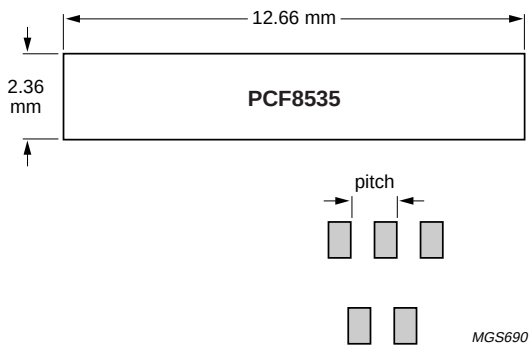
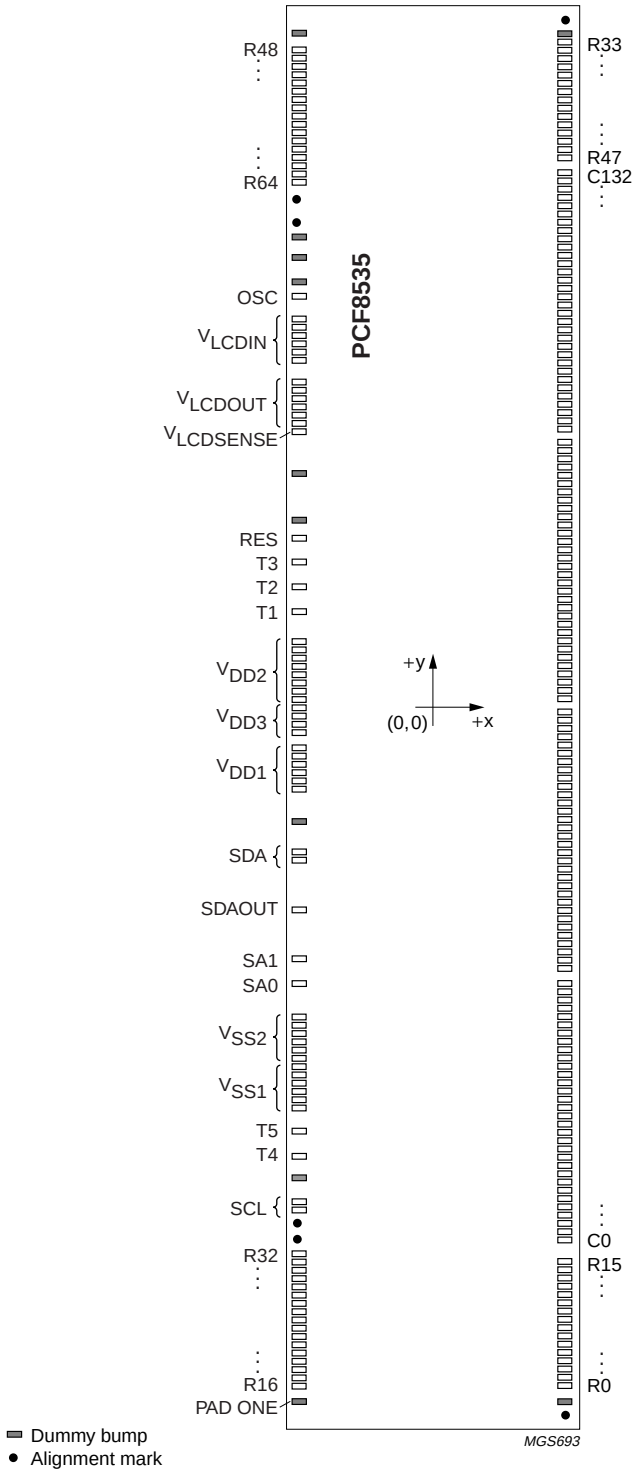


Fig.32 Bonding pads.



The position of the bonding pads is not to scale.

Fig.33 Bonding pad location (viewed from bump side).

15 DEVICE PROTECTION

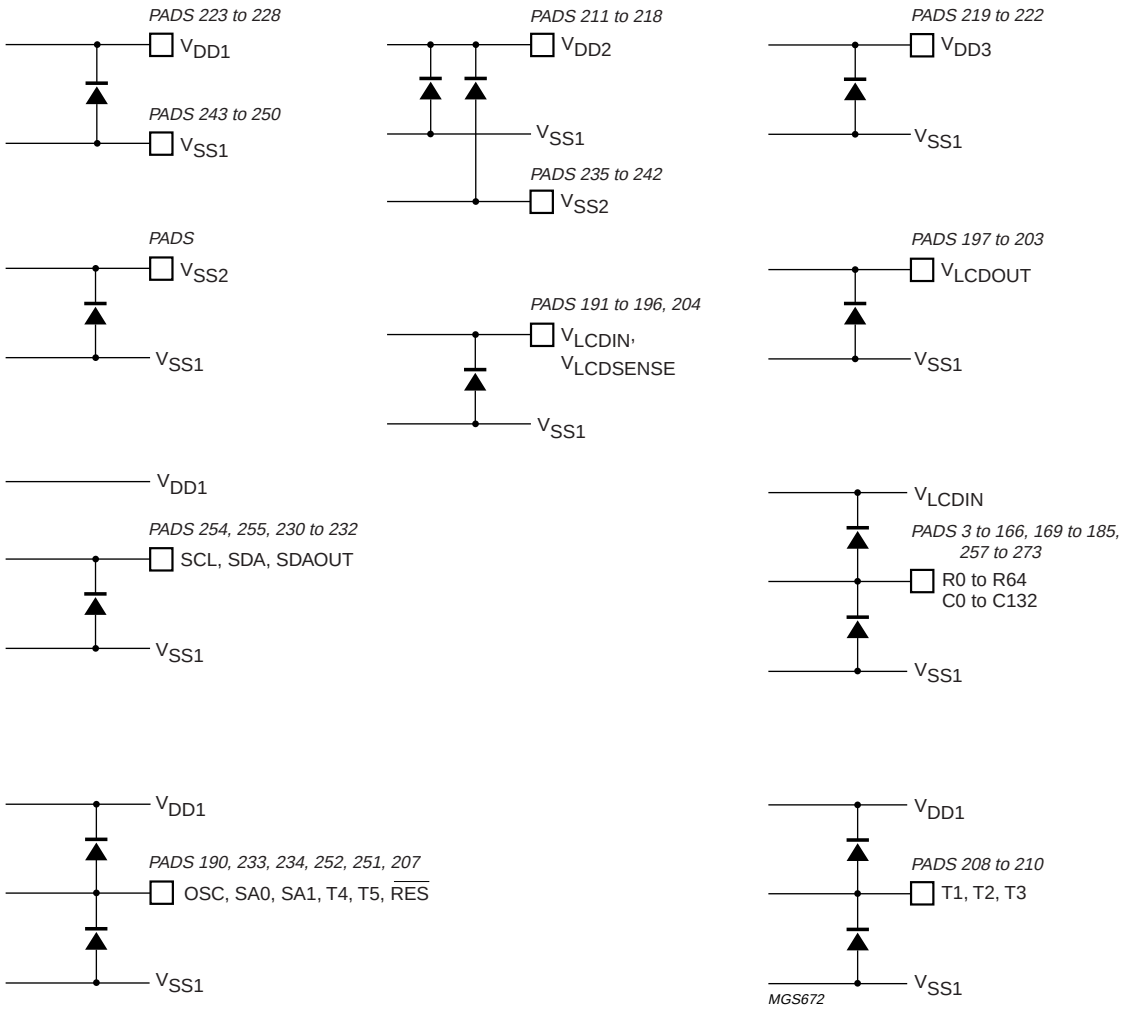
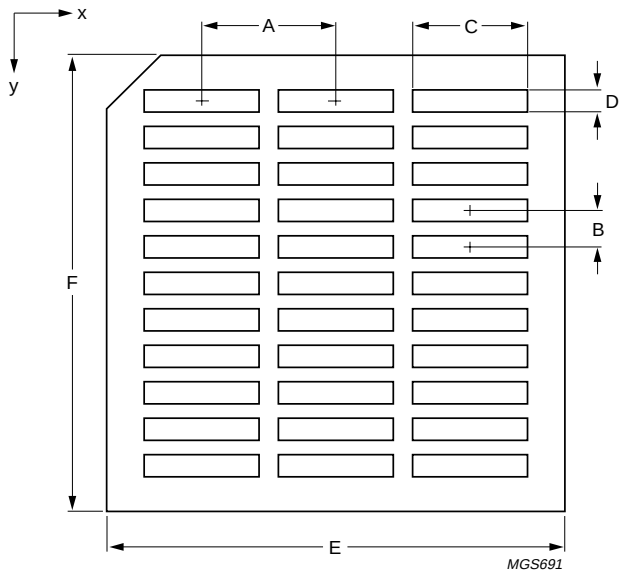


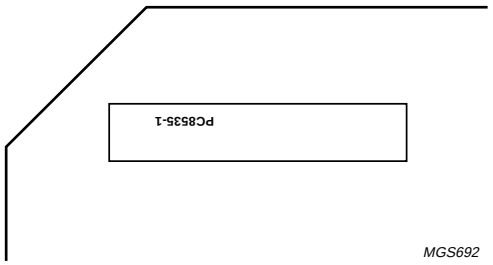
Fig.34 Device diode protection diagram.

16 TRAY INFORMATION



The dimensions are given in Table 25.

Fig.35 Tray details.



The orientation of the device in a pocket is indicated by the position of the device type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.36 Tray alignment.

Table 25 Tray dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch in x direction	14.88 mm
B	pocket pitch in y direction	4.06 mm
C	pocket width in x direction	12.76 mm
D	pocket width in y direction	2.46 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	11

17 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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