Power amplifier controller for GSM and PCN systems

PCF5075

FEATURES

- CMOS low-voltage, low-power
- Can be used in burst mode with power-down
- Three-wire serial bus interface with the bus available in power-down mode
- On-chip ramp generator for 256 different power levels
- Extendable dynamic range
- Two programmable regulator start conditions, V_{KICK} and V_{HOME}
- Programmable analog output voltage limitation
- Ramping speed depending on the 13 MHz system frequency clock for Global System for Mobile communications (GSM) and Personnel Communications Network (PCN)
- Low swing input buffer for the 13 MHz master clock
- Compatible to a large number of different RF power modules
- Programmable temperature matching
- Quick restart option.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	2.7	5.0	5.5	V
V_{DDA}	analog supply voltage	2.7	5.0	5.5	V
$I_{DD(tot)}$	total supply current	–	9	15	mA
T_{amb}	operating ambient temperature	–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF5075	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266

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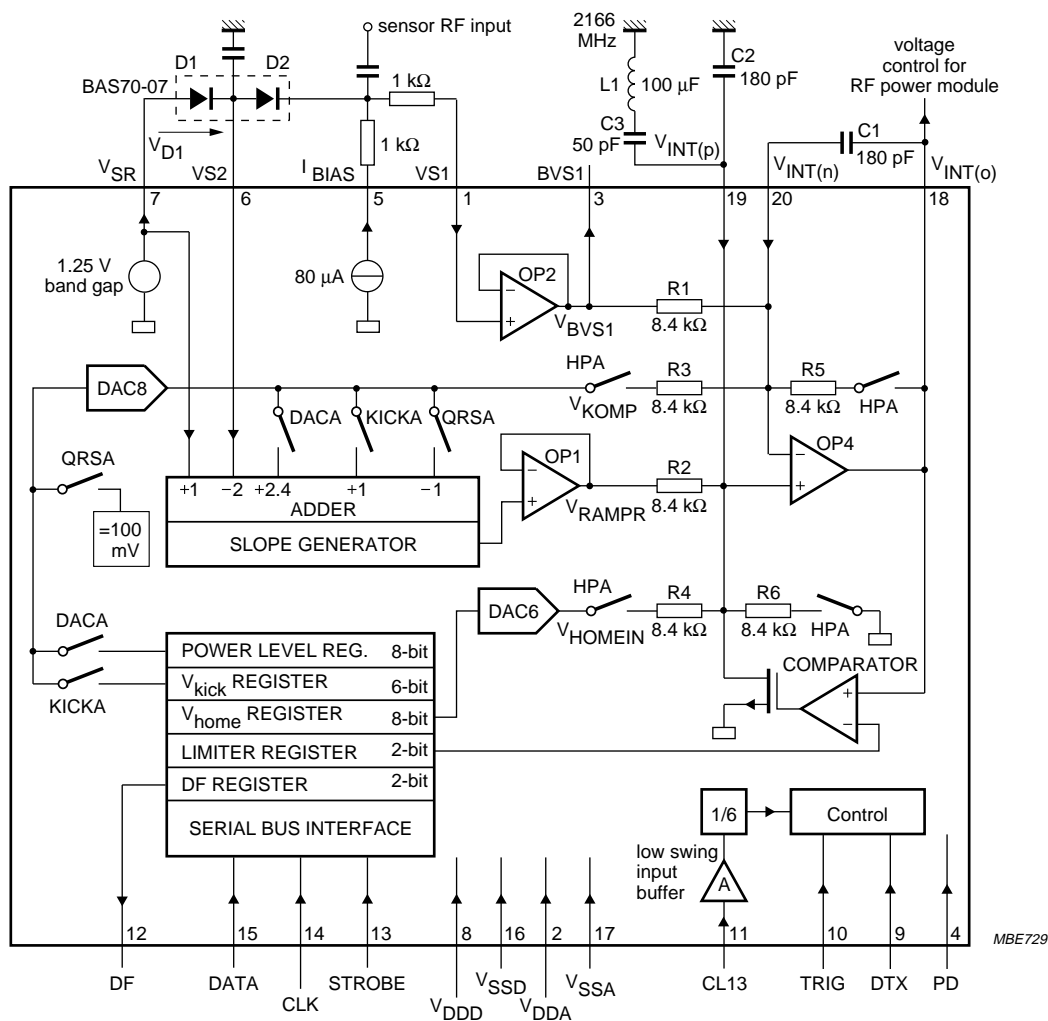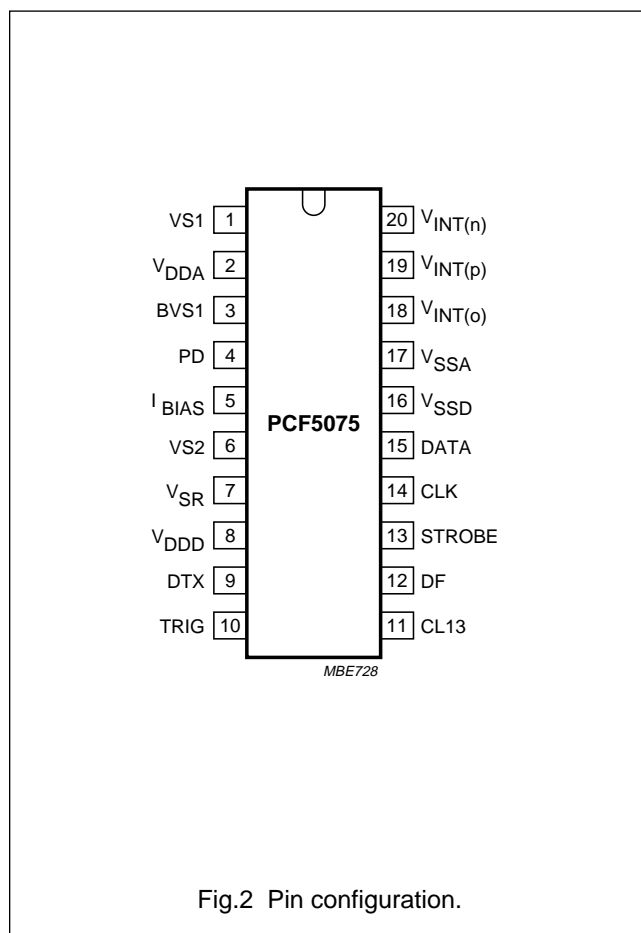
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BLOCK DIAGRAM

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
VS1	1	sensor signal input 1
V_{DDA}	2	analog supply voltage
BVS1	3	buffered sensor output signal
PD	4	power-down input
I_{BIAS}	5	bias current output for external rectifier
VS2	6	sensor signal input 2
V_{SR}	7	bias voltage output for sensor
V_{DDD}	8	digital supply voltage
DTX	9	test, disable or stop TX burst (has to be connected to V_{SSD})
TRIG	10	trigger signal input
CL13	11	13 MHz master clock pulse input (LOW swing input)
DF	12	programmable 3-state output
STROBE	13	serial bus strobe input signal
CLK	14	serial bus clock input signal
DATA	15	serial bus data input signal
V_{SSD}	16	digital ground
V_{SSA}	17	analog ground
$V_{INT(o)}$	18	integrator output voltage
$V_{INT(p)}$	19	integrator positive input voltage
$V_{INT(n)}$	20	integrator negative input voltage

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

This CMOS device integrates operational amplifiers, two digital-to-analog converters and a serial interface to implement an 'Integrating-Controller'. It is designed to control both the power level and the up and down-ramping of GSM-transmit bursts.

The GSM/PCN power-up power-down ramping curves are generated on-chip, using an internal clock frequency of 2.166 MHz ($T_{cy} = 1/f_{clk}$), that is generated internally by dividing the external 13 MHz clock by six.

Generally, the power amplifier is ramped-up after a rising edge on TRIG (pin 10) and ramped-down after a falling edge. When TRIG goes LOW for less than two clock periods ($2T_{cy}$), a special function for base station applications is activated (see Chapter "Appendix A: base station features").

When DTX (pin 9) becomes active during a ramp-up, ramping is stopped and a normal ramp-down is executed thereby turning the power module off. To restart the ramp generator, DTX and TRIG have to go LOW (TRIG has to stay LOW for more than two clock periods). The next LOW-to-HIGH transition will cause a ramp-up again.

The contents of the power-level register (PL7-to-PL0) determines which of 256 possible values the top of the clock period burst will have.

To match the controller to different power modules and sensors several parameters must be adapted:

1. The typical value of the external capacitors C1 and C2; C1 determines the maximum bandwidth of the power control loop, depending on the highest steepness of the control curve of the power module and on the sensor attenuation (see Fig.4).

2. The upper voltage limit of $V_{O(INT)}$ (pin 18) to protect the power module; the output of $V_{O(INT)}$ can be limited to 4.0 V, 3.4 V or 2.7 V, depending on the contents of the limiter register (lim1-to-lim0). The fourth limiter register word can be used to switch the limiter option off. This limiting results in a ringing at $V_{O(INT)}$ (200 mV (p-p) typ.) but, because the power module is in saturation, it will not transfer the ringing to the antenna.

3. The HOME $V_{O(INT)}$ position; the integrator output voltage at home position, (PD and TRIG LOW) must be programmed with the V_{HOME} register. Bits Vh5-to-Vh0 are fed into a 6-bit DAC that generates a part of V_{HOME}.

4. The temperature behaviour of the home position; bits Dvh1 and Dvh0 must be used to add 0, 1 or 2 internally generated diode voltages to V_{HOME}. In this manner it is possible to compensate for a possible temperature dependence (-2 mV/°C or -4 mV/°C) of the control curves of the power module.

5. The KICK voltage; the 6 bits of the KICK voltage register (Vk5-to-Vk0) determine the differential integrator input voltage just after a ramp-up starting signal is detected.

The register information is written via a three-wire serial bus (see Sections "Serial bus programming" and "Data format").

The DF output (pin 12) is a general purpose pin which can have three different states, LOW, HIGH and 3-state, depending on the values of DF0 and DF1 in the serial register.

Separate power supply pins are provided for the analog and digital blocks.

Primary start condition

When the power supply is first switched on, the PCF5075 is in an undefined state because the chip has neither a power-on-reset nor a reset pin. Consequently, a first initialisation of the digital part is necessary.

The easiest way of doing this is to perform a short dummy ramp-up/ramp-down sequence, apply the 13 MHz master clock, make PD LOW and then toggle TRIG LOW-HIGH-LOW for more than two clock periods in the HIGH state. The chip will stay initialized as long as the supplies are on. After this, recognition of the 13 MHz master clock and TRIG will be influenced by PD.

PD LOW

The serial bus is operating, e.g. all registers can be programmed but no effect will be seen on any pin. The contents of these registers are passed to the rest of the circuit only during power-up and with the 13 MHz master clock applied.

Also, because the LOW-input swing buffer at pin CL13 is switched off, neither the adder nor the slope generator will function. This means that after the chip is powered-up, the outputs have to settle again to the programmed register values. The settling time is dominated by the slow power-up of the band gap of typically 250 μs.

If the chip is used in the burst mode, it is important to switch on the PCF5075 before the power module or the

RF-power. Otherwise it is possible that a positive spike at $V_{O(INT)}$ will open the power module.

A save value is t_{ON} = 400 μs between the PCF5075 and the power module respectively the next TRIG pulse (see Fig.3).

PD HIGH

The whole chip is active. Pin CL13 clocks the internal state machine as well as the adder and slope generator. Every change at TRIG is recognized if the master clock is running. The contents of the serial bus registers are processed. If the master clock is switched off during power-up, the state machine is stopped and the output of the adder/slope generator becomes undefined. Nevertheless, by reactivating the master clock, the output of the adder/slope generator will settle to the old values again.

The analog integrating controller

The analog integrating controller consists of three operational amplifiers (OP1, OP2 and OP4) and one comparator. OP1 and OP2 are only used for buffering purposes, OP 4 is used to form a differential integrator. The comparator is used to limit the integrator output voltage to the value selected by the 'lim'-bits in the serial register.

A two (Schottky) diode external rectifier is connected to pins V_{SR}, VS2, I_{BIAS} and VS1.

The SC-Adder block basically generates the voltage $V_{SR} - 2V_{D1} + V_{PL}$. The differential integrator then integrates the difference of this voltage and the voltage $V_{SR} - 2V_{D1} + V_{RFIN}$. The integrator output voltage $V_{O(INT)}$ is used to control the power amplifier module.

Table 1 Definition of some voltages (see Fig.1)

SYMBOL	DESCRIPTION
V_{SR}	band gap voltage, typically 1.25 V
V_{D1}	voltage over the (external) Schottky diode D1
V_{PL}	voltage determining the power level; it is generated in the SC-Adder block if switch DACA is closed (i.e. if the signal DACA is HIGH); equals 2.4 times the DAC8 output
V_{RFIN}	voltage difference at pin VS1 when RF is rectified at the sensor diode D2
V_{BVS1}	buffered voltage from pin VS1
V_{KICK}	kick voltage; if KICKA is HIGH, DAC8 outputs this voltage
V_{KOMP}	voltage at R3 if the circuit is switched to the home position by HPA; V_{KOMP} compensates V_{KICK} at R2

V_{RAMPR}	buffered output voltage of the slope generator; steady state limits of some succeeding filtered voltage steps (not 1:1 visible at pin $V_{INT(p)}$)
	
	    HPA/KICKA active: $V_{SR} - 2V_{D1} + V_{KICK}$
	
	    DACA active: $V_{SR} - 2V_{D1} + V_{PL}$
	
	    QRSA active: $V_{SR} - 2V_{D1} - V_{QRS}$

V_{HOMEIN}	if HPA is active, DAC6 outputs the value of the V_{HOME} register which is directly visible only at pin 18; V_{HOMEIN} also contains the diode forward voltages nV_F (with n = 0,1 or 2; $V_F \approx$ 700 mV at T_{amb} = 27 °C)
V_{QRS}	0 or 100 mV; 0 V only if a 'Quick Restart' condition is detected; otherwise, if QRSA is active, DAC8 outputs 100 mV; this voltage is inverted by the adder and causes a ramp-down with a shortened tail

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Ramp generation (see Fig.3)

The circuit is activated with the PD signal going LOW before time mask 'AS' and deactivated after ramping-down, e.g. at 'GS' to 'HS'. For this usual "power-down burst mode" application in GSM/PCN mobile stations the RF input power at the power module must be activated between 'AS' and 'BS' (when the home position at $V_{O(INT)}$ has already reached its stable value) and deactivated between 'GS' and 'HS'.This is necessary for many types of power modules to meet the −70 dB margin. For quick restart after ramping-down see Chapter "Appendix A: base station features".

A ramp-up is started by a positive edge on TRIG. To be able to detect a quick restart (base station applications only) the TRIG signal is internally delayed by two clock periods. Because of this, all other internal signals are delayed by two clock periods with respect to the signal at pin TRIG.

The timing diagram shows a possible relationship between the chip timing ('B' to 'G') relative to the GSM-mask ('AS' to 'HS'). However, the user is free to choose t_1 and t_2 independently so that the mask is not violated.

Description of the signals starting at a stable home position of $V_{O(INT)}$ at time $B − 2T_{cy}$.

The integrator output voltage is regulated to the value defined in the V_{HOME} register. The output of the slope generator is $V_{SR} − 2V_{D1} + V_{KICK}$ and is connected to the positive input $V_{INT(p)}$ of operational amplifier OP4 (V_{KICK} is defined by the 'V_k'-bits in the V_{KICK} register). Two clock periods after a positive edge on TRIG the integrator start condition circuitry is turned off and OP4 is switched into an integrator configuration ('B'). Now the HPA switches are open. Due to the positive differential input voltage V_{KICK}, the integrator output will start to rise. After $18T_{cy}$ ('C') the output of DAC8 is connected to the adder and slope generator block. The input of the 8-bit DAC comes from PL7 to PL0 of the power level register. The slope generator will generate a smooth curve between the former and the new output value of the adder block. The voltage V_{RAMPR} at the end is $V_{SR} − 2V_{D1} + VPL$, thus the power amplifier is ramped-up via the integrator in approximately $22T_{cy}$.

This condition is stable providing TRIG remains HIGH. Two clock periods after a negative edge at TRIG the ramp-down is started ('E').The adder output voltage will change to $V_{SR} − 2V_{d1} − V_{QRS}$ (V_{QRS} = 100 mV typ.), because DACA becomes inactive and QRSA active. This additional subtraction of 100 mV causes a ramp-down with a shortened tail.The slope generator again generates a smooth curve between the new adder output voltage and the old adder output voltage. The slope generator must have reached its final value $38T_{cy}$ after the recognized falling edge of TRIG because the signal HPA is activated again and by that turning the integrator into its 'home position' ('G').The integrator output voltage will be regulated once more to the value defined in the V_{HOME} register. The adder output voltage is $V_{SR} − 2V_{D1} + V_{KICK}$. The voltage V_{KICK} is subtracted at $V_{INT(n)}$ by V_{KOMP} while the home position is active (see Fig.1). Thus the resulting voltage at $V_{O(INT)}$ has the programmed value V_{HOME}.

Figs 4, 5 and 6 show measurements of the circuit in application.

STABILITY

Figure 6 shows the result of a special test. A static power level was chosen where the steepness of the control curve of a worst case power module sample has the highest value. This value usually is approximately 6 to 10 dB less than the maximum possible power. Capacitors C1 and C2 are now reduced to the point where the loop is close to the limit of stability. A gain peaking at the critical frequency occurs and noise increases. By this easy procedure the critical frequency and the critical value for C1 = C2 can be found. These capacitances must now be increased by a factor of 2 to 4 for sufficient stability reserve.

CLOCK INFLUENCE

The resulting loop band width must be smaller than the internal clock frequency f_{clk} = 2.166 MHz. A gain peaking effect at f_{clk} must be avoided, low pass filters between pin $V_{O(INT)}$ and the input of the power module will reduce the stability margin and this can cause an unwanted gain at f_{clk}. As shown in the block diagram (see Fig.1) an uncritical serial resonant circuit at pin $V_{INT(p)}$ is recommended.

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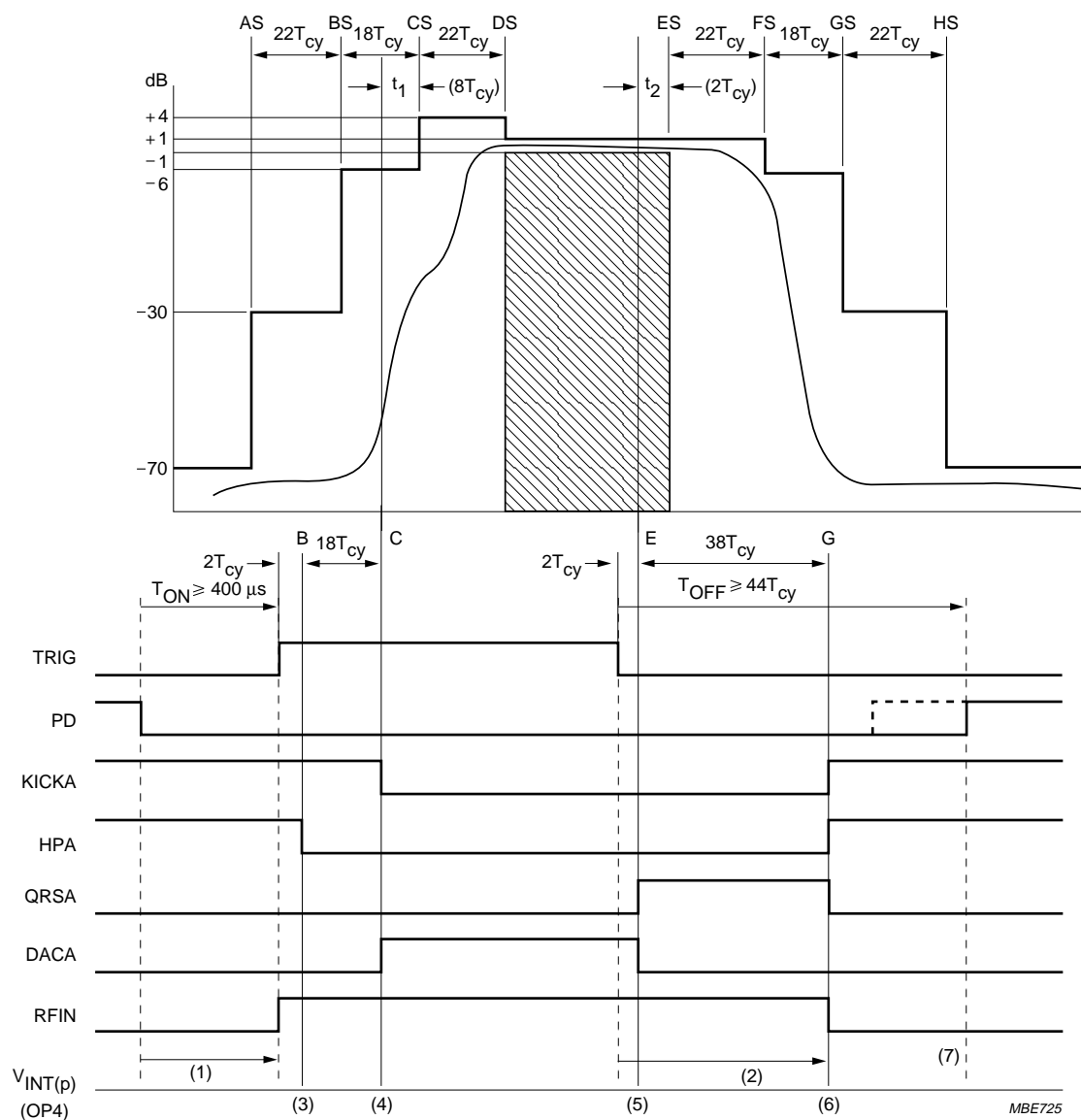
(1) $t_{RFON} = t_{ON} - 12T_{cy}$ to $t_{ON} + 2T_{cy}$.

(2) $t_{RFOFF} = 44T_{cy}$ to $66T_{cy}$.

(3) $V_{SR} - 2V_{d1} + V_{kick}$ (start integrator).

(4) $V_{SR} - 2V_{d1} + V_{PL}$.

(5) $V_{SR} - 2V_{d1} - V_{qrs}$.

(6) $(V_{SR} - 2V_{d1} + V_{kick} + V_{HOMEIN})/3$.

(7) This timing to the RF input power of the power module ensures that the −70 dB margin, even if the isolation of the power module is bad, is met.

Fig.3 Timing of a typical ramp-up/ramp-down curve.

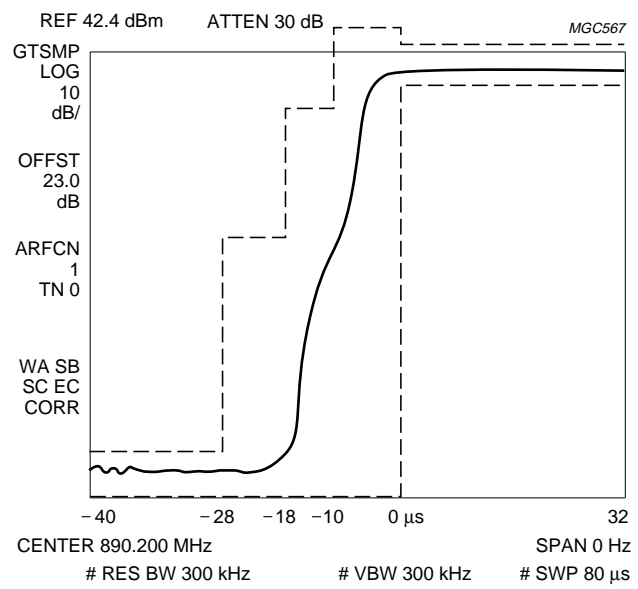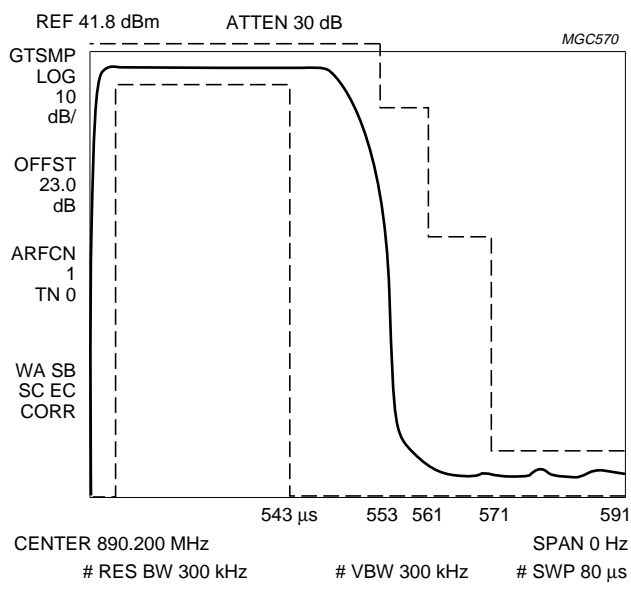# Power amplifier controller for GSM and PCN systems

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REF 42.4 dBm ATTEN 30 dB MGC567

GTSMP LOG 10 dB/

OFFST 23.0 dB

ARFCN 1 TN 0

WA SB SC EC CORR

−40 −28 −18 −10 0 μs 32

CENTER 890.200 MHz SPAN 0 Hz

\# RES BW 300 kHz # VBW 300 kHz # SWP 80 μs

Fig.4 Ramp-up.

REF 41.8 dBm ATTEN 30 dB MGC570

GTSMP LOG 10 dB/

OFFST 23.0 dB

ARFCN 1 TN 0

WA SB SC EC CORR

543 μs 553 561 571 591

CENTER 890.200 MHz SPAN 0 Hz

\# RES BW 300 kHz # VBW 300 kHz # SWP 80 μs
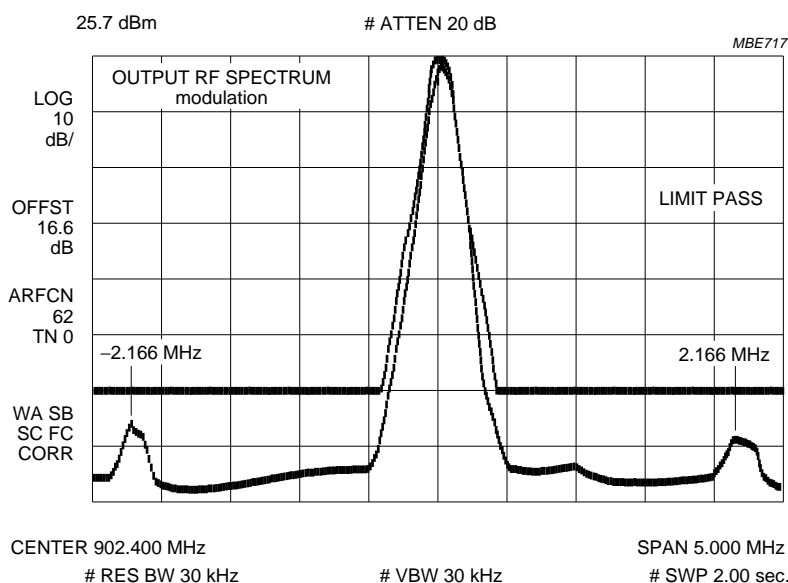
Fig.5 Ramp-down.

Fig.6 Modulation spectrum.

Serial bus programming

A simple 3–wire unidirectional serial bus is used to program the circuit. The 3 wires are Data, Clock and Strobe. The data sent to the device is loaded in bursts framed by Strobe. Programming clock edges and their appropriate data bits are ignored until Strobe goes active LOW. The programmed information is loaded into the addressed latch when Strobe returns inactive HIGH. Only the last 16 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. The bus is also programmable during power-down.

Data format

Data is entered with the most significant bit (MSB) first. The leading bits make up the data field, while the trailing four bits are an address field. The PCF5075 uses only one of the available addresses. The format is given in Table 2.

The trailing address bits are decoded upon the inactive Strobe edge. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous circuit operation, the strobe pulse is not allowed during internal data reads by the rest of the circuit. This condition is guaranteed by respecting a minimum Strobe pulse width after data transfer (see Chapter "Timing characteristics").

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Table 2 Programming register bit usage

DATA BITS				SUBADDRESS		DEVICE ADDRESS			
MSB			LSB						
p15	pxx	p7	p6	p5	p4	p3	p2	p1	p0
data9	datax	data1	data0	Sadd1	Sadd0	add3	add2	add1	add0

The correspondence between data and address fields is given in Table 3.

Table 3 Register bit allocation

DATA FIELD (D9 TO D0)										SUB ADDRESS		DEVICE ADDRESS			
MSB									LSB						
p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	0
Vk5	Vk4	Vk3	Vk2	Vk1	Vk0	Lim1	Lim0	nu[1]	nu[1]	0	0	1	0	1	0
Vh5	Vh4	Vh3	Vh2	Vh1	Vh0	DVh1	DVh0	nu[1]	nu[1]	0	1	1	0	1	0
PL7[2]	PL6[2]	PL5[2]	PL4[2]	PL3[2]	PL2[2]	PL1[2]	PL0[2]	DF1[4]	DF0[3]	1	1	1	0	1	0

Notes

1. nu = not used.

2. PL = power level.

3. DF0 = data on DF output.

4. DF1 = enable of this output for DF1 = 0 pin DF is in 3-state mode.

Table 4 Limiter voltage

LIM1	LIM0	LIMITER VOLTAGE	TOLERANCE AT $T_{amb} = 27\,°C$	TOLERANCE AT $T_{amb} = 85\,°C$
1	1	limiter off	−	−
0	0	2.7 V	±250 mV	±450 mV
0	1	3.4 V	±250 mV	±450 mV
1	0	4.0 V	±250 mV	+250 to −750 mV

Table 5 DVh diode offset for V_{HOME}

DVH1	DVH0	V_{HOME}[1][2]
0	0	Vh
0	1	Vh+ VF
1	0	Vh + 2VF
1	1	V_{DD}

Notes

1. Vh = voltage programmed into Vh5 to Vh0 generated by DAC6 (max. 2 V at $V_{SR} = 1.25$ V).

2. VF = an internally generated diode voltage drop with 0.7 V ±50 mV at $T_{amb} = 25\,°C$ or 0.7 V +50 to −100 mV at $T_{amb} = 85\,°C$ ($T_C \approx −2$ mV/°C).

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Vk BITS

The Vk bits control the kick voltage in 64 steps of 4.8 mV per step.

Vh BITS

The Vh bits control the home position voltage in 64 steps of 32 mV per step.

PL BITS

The PL bits control the ramp-up top level voltage (equal to power level) in 256 steps of 11.7 mV per step.

LIMITING VALUES

$V_{DD} = V_{DDD} = V_{DDA}$; $V_{SS} = V_{SSD} = V_{SSA}$; in accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	7.0	V
V_i	DC input voltage on all pins	−0.5	7.0	V
I_i	DC current into any signal pin	−10	+10	mA
P_{tot}	total power dissipation	−	83	mW
T_{stg}	storage temperature	−65	150	°C
T_{amb}	operating ambient temperature	−40	85	°C

OPERATING CHARACTERISTICS

T_{amb} = −40 to 85 °C; $V_{DD} = V_{DDA} = V_{DDD}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operational amplifier (OP1)						
V_{DD}	supply voltage		2.7	−	5.5	V
B_G	gain bandwidth	at −3 dB	−	4	−	MHz
SR(p)	positive slew rate		−	0.3	−	V/µs
SR(n)	negative slew rate		−	0.3	−	V/µs
Operational amplifiers (OP2 and OP4)						
V_{DD}	supply voltage		2.7	−	5.5	V
B_G	gain bandwidth	at −3 dB; unity gain; C_L = 220 pF; note 1	4	−	−	MHz
CMRR	common mode rejection ratio		−	45	−	dB
PSRR	power supply ripple rejection	for unity gain	50	−	−	dB
SR(p)	positive slew rate	for unity gain; note 2	4.5	−	−	V/µs
SR(n)	negative slew rate	for unity gain; note 2	4.5	−	−	V/µs
V_{os}	voltage offset	no load at output	−7	0	+7	mV
CM_{il}	common mode input low limit	± 5% tolerance; note 3	−	−	0.5	V
CM_{ih}	common mode input high limit	± 5% tolerance; notes 3 and 4	$0.9V_{DD}$	−	−	V

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SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$V_{o(min)}$	minimum output voltage	for unity gain	–	–	0.3	V
$V_{o(max)}$	maximum output voltage	for unity gain; note 4	$0.85V_{DDD}$	–	–	V
R_O	small signal output resistance	I_{load} = 2 mA at 1.9 V	–	5	10	Ω
Resistors R1 and R2						
R1	value of R1	T_{amb} = 25 $^\circ$C	6.7	8.4	10	kΩ
R2	value of R2	T_{amb} = 25 $^\circ$C	6.7	8.4	10	kΩ
R_{match}	matching between R1 and R2		–	2	–	%
T_C	temperature coefficient		–	0.13	–	%/$^\circ$C
Programmability and accuracy of V_{PL}						
INLE	integral non-linearity error		–	–	$\pm$10	LSB
DNLE	differential non-linearity error		–	–	$\pm$1	LSB
$V_{o(min)}$	minimum output voltage	note 5	–	11.5	–	mV
$V_{o(max)}$	maximum output voltage	notes 5 and 6	–	$2.4V_{SR}$	–	V
Programmability and accuracy of V_{KICK}						
INLE	integral non-linearity error		–	–	$\pm$10	LSB
DNLE	differential non-linearity error		–	–	$\pm$1	LSB
$V_{o(min)}$	minimum output voltage	note 5	–	4.8	–	mV
$V_{o(max)}$	maximum output voltage	note 5	–	312	–	mV
Programmability and accuracy of V_{HOME}						
INLE	integral non-linearity error		–	–	$\pm$10	LSB
DNLE	differential non-linearity error		–	–	$\pm$1	LSB
$V_{o(min)}$	minimum output voltage	V_{SR} = 1.25 V; Dvh1 = 0; Dvh0 = 0; note 5	–	32	–	mV
$V_{o(max)}$	maximum output voltage	V_{SR} = 1.25 V; Dvh1 = 0; Dvh0 = 0; note 5	–	2	–	V

Notes

1. Minimum specified frequency at T_{amb} = 27 $^\circ$C; for T_{amb} = 85 $^\circ$C a typical value of 4 MHz is specified.

2. Slew rates are measured between 10% and 90% of output voltage interval with a load of approximately 40 pF to ground.

3. The tolerance band for the input range is defined as the interval where the output follows the input with $\pm$5% tolerance of the actual input value.

4. These values at T_{amb} = 25 $^\circ$C are supply voltage and temperature dependent (T_C = 3 mV/$^\circ$C).

5. The value is dependent on V_{SR}, for tolerance of V_{SR} (see Chapter "DC characteristics").

6. The maximum output is limited to $V_{PL(max)}$ = $0.85V_{DD}$.

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DC CHARACTERISTICS

$T_{amb} = -40$ to 85 °C; $V_{DD} = V_{DDD} = V_{DDA}$; $V_{SS} = V_{SSD} = V_{SSA} = 0$ V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	5.0	5.5	V
$I_{DD(op)}$	total operating current	$f_i = 13$ MHz	–	9	15	mA
$I_{DD(idle)}$	total idle current	PD = HIGH	–	–	10	μA
Logic I/O's (pins 4, 9, 10, 12 to 15)						
I_{IL}	LOW level input leakage current	$V_{IL} = 0.8$ V	–5	–	5	μA
I_{LH}	HIGH input leakage current	$V_{IH} = 2$ V	–5	–	5	μA
C_i	input capacitance		–	10	–	pF
CL13, low-swing master clock input (pin 11)						
I_{PD}	input pull-down current in power-down	$V_i = 1$ V; $T_{amb} = 25$ °C; $T_C = -0.5\%/°C$; note 1	–	–	25	μA
C_I	input capacitance		–	10	–	pF
$|Z_i|$	input impedance	$f_i = 13$ MHz; note 1	–	5	–	kΩ
$V_{i(p–p)}$	input voltage (peak-to-peak value)	AC coupling = 33 pF	0.5	–	V_{DD}	V
Sensor DC reference input voltage VS1 and VS2 (pins 1 and 6); note 2						
V_{VS2}	input voltage		0	–	V_{SR}	V
V_{VS1}	input voltage		–	–	$0.9V_{DD}$	
Bias current source I_{BIAS} (pin 5)						
I_{BIAS}	bias current source for D1 and D2	$V_i = 1$ V; $T_{amb} = 25$ °C; $T_C = -0.22μA/°C$	60	80	100	μA
V_{CM}	voltage range	note 3	0.3	–	$0.9V_{DD}$	V
Band gap voltage V_{SR} (pin 7)						
V_{SR}	bandgap voltage	$T_{amb} = 25$ °C	1.16	1.25	1.34	V
T_C	temperature coefficient for V_{SR}		–	–0.175	–	mV/°C
T_{pu}	power-up time band gap	note 4	–	250	–	μs
Other analog I/O's (pins 3, 18, 19 and 20)						
I_{IL}	input leakage current	$V_i = 1$ V	–15	–	15	μA
C_I	input capacitance		–	10	–	pF

Notes

1. In power down mode this input is inactive and switched to ground with more than 40 kΩ. An AC coupling with 33 pF is recommended.

2. The voltage at pin VS2 is $VS2 = V_{SR} - V_{d1}$ with the forward voltage $V_{d1} \sim 250$ mV of the DC reference diode D1 of the RF sensor. V_{d1} must not be influenced by RF because a voltage change at pin VS2 moves the input voltage of the adder and slope generator.

3. Two 1 kΩ resistors close to the RF sensor diode D2 in the block diagram are necessary for RF decoupling.

4. The necessary start-up time $T_{ON} = 400$ μs (see Fig.3) between PD and TRIG is more than T_{pd}.

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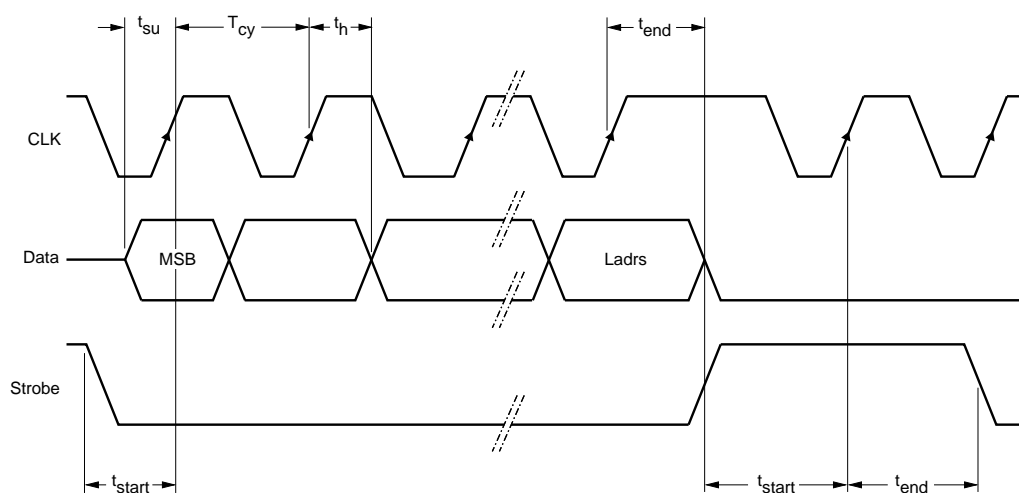
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TIMING CHARACTERISTICS

T_{amb} = −40 to +85 °C; V_{DD} = V_{DDA} = V_{DDD}; V_{SS} = V_{SSA} = V_{SSD} = 0 V; unless otherwise specified.
For timing see Fig.3; T_{cy} = $^6/_{13}$ μs.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Controller timing					
t_{qrs}	negative pulse width on TRIG for quick restart recognition	0.077	–	0.769	μs
t_{noqrs}	negative pulse width on TRIG for no quick restart recognition	1.0	–	–	μs
$t_{d(TRIG-B)}$	delay from positive TRIG edge to point B = $^{13}/_6 T_{cy}$	–	1.0	–	μs
$t_{d(B-C)}$	delay from point B to point C = $18T_{cy}$	–	8.31	–	μs
$t_{d(TRIG-E)}$	delay from negative TRIG edge to point E = $^{13}/_6 T_{cy}$	–	1.0	–	μs
$t_{d(E-G)}$	delay from point E to point G = $38T_{cy}$	–	17.54	–	μs
Serial bus timing					
SERIAL PROGRAMMING CLOCK (PIN 14)					
t_r	rise time	–	10	–	ns
t_f	fall time	–	10	–	ns
T_{cy}	clock period	100	–	–	ns
ENABLE PROGRAMMING (PIN 13); note 1					
t_{start}	strobe set-up time to first clock edge	40	–	–	ns
t_{end}	strobe hold time from first clock edge	20	–	–	ns
REGISTER SERIAL INPUT DATA (PIN 15)					
t_{su}	input data to CLK set-up time	20	–	–	ns
t_h	input data to CLK hold time	20	–	–	ns

Note

1. After rising edge of STROBE one more active CLK edge (LOW-to-HIGH transition) completes the transfer.

Fig.7 Serial bus timing diagram.

APPLICATION INFORMATION

Switching the dynamic range

For GSM phase 2 and PCN, some very low power levels are needed. The control voltage V_{PL} can be as low as 30 mV, which is approximately 3 LSB of the power level register and therefore not accurate enough. Nevertheless it is possible to use this chip. The DF pin (pin 12) can be used to switch a 13 dB attenuator, right after the sensor, into the antenna path.

This has the advantage of not changing the behaviour of the loop, however, the disadvantage is introducing a certain amount of attenuation when switched off. As shown in the application diagram (see Fig.8) another approach is to switch a gain stage at the sensor. By doing this the loop gain and the bandwidth of the loop will be switched. Consequently, at least a 13 dB stability margin is needed if the switchable gain stage has a range of 13 dB.
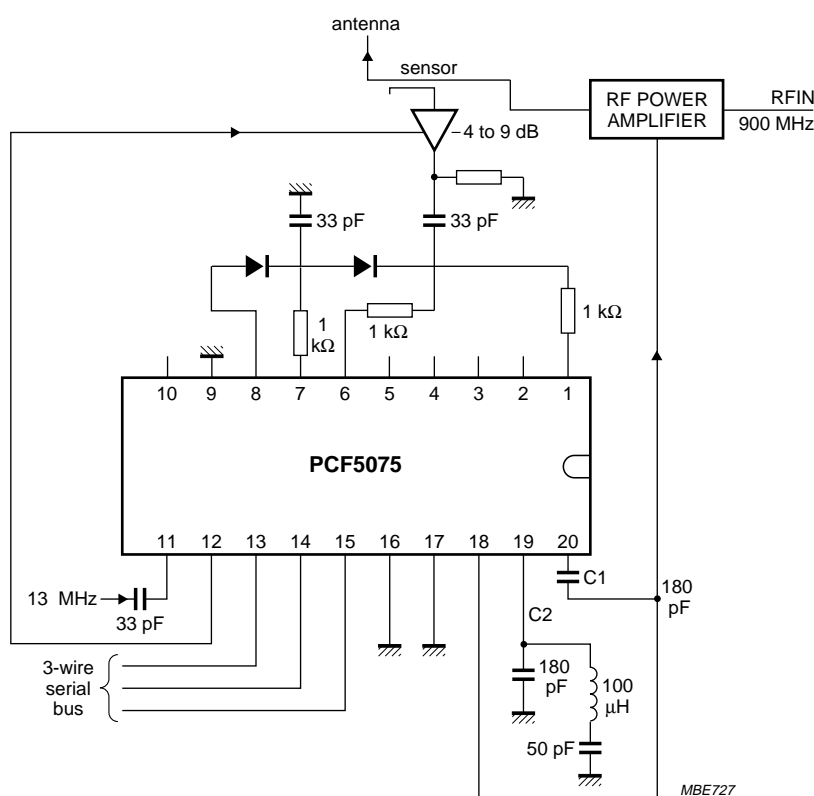
Fig.8 Application diagram for mobile stations.

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Additional application information

An evaluation kit with software and demonstration boards is available for the PCF5075 together with the power modules BGY20x. Additionally, a package of PSPICE models with several plots and descriptions is also available which will provide help for applications.

Very little bus traffic is required for the PCF5075 because the ramping curves are generated on-chip. V_{KICK} and V_{HOME} define the start conditions for up-ramping. V_{PL} determines the power levels. TRIG is the trigger for up and down-ramping.

The non-linear behaviour of the control curves of the power modules have a big influence on the loop. Start conditions in the flat area of the control curve are critical and need some attention. Initially $V_{O(INT)}$ will be at the home position. The switches HPA release the regulator. The integrator now must be moved into the active part of the control curve. This is achieved by integrating V_{KICK}. When $V_{O(INT)}$ has reached the active region of the control curve the loop is closed and the circuit is able to follow the ramping function generated by a voltage step to the slope generator. The step height V_{PL} determines the power of the transmit burst. Down-ramping is started at the slope generator input by a voltage step from V_{PL} back to -100 mV. The loop follows the leading function for down-ramping until the RF sensor measures zero. The sensor signal is not able to go to -100 mV because this would represent a negative power. The reason for the -100 mV in the leading function is to shorten the tail of the slope.

For V_{KICK} a value of 60 mV is recommended, matched to a kick power that is 8 dB below -13 dBm (see Fig.9). Usually V_{KICK} has a constant value for all power levels.

One of the highlights of the PCF5075 is that for matching of the start behaviour only one parameter must be adapted to the individual sample of the power module. This parameter is the home position of $V_{O(INT)}$ that is set by V_{HOMEIN}. An optimized value must be chosen in production for the life of the device. This value can be stored in an EPROM. Software may help to adapt V_{HOMEIN} to different temperatures. The $V_{O(INT)}$ home position that has to be programmed must be matched to the middle of the two curves illustrated in Fig.9.

V_{HOMEIN} is the sum of V_{HOME} and of the diode forward voltages with a typical negative temperature behaviour. Two diodes are necessary for matching the behaviour of the power module BGY20x. But if two diodes are chosen (see Table 5), the absolute value of $V_{O(INT)}$ is so high that there is not enough room for matching the start behaviour.

Therefore, only one diode is recommended for the modules BGY20x. The fine temperature matching must be done by software. Details about this matching are shown in plot 3 of the PSPICE package.

Curve 1 in Fig.9 shows what happens if the home position of $V_{O(INT)}$ has the highest usable value. This behaviour is matched to meet the -6 dB margin and the -30 dB margin at the power level -13 dBm. The -70 dB margin will be met by optimizing the time where the RF input power of the power module is activated.

Curve 2 in Fig.9 results if the home position has the lowest usable value. Here the ramping curve seems to be optimal, but the switching spectrum is at the limit. This behaviour occurs when the regulator, which is integrating V_{KICK}, has not yet reached the active part of the power module control curve and thus the step of the slope generator has the highest steepness. In this situation the power ramps-up with a delay and with increased steepness as can be seen in the curve.

For the power level -13 dBm the TRIG time may be shifted a little by software. At all other power levels TRIG can be kept constant.

THEORETICAL LIMIT FOR CORRECT DOWN-RAMPING

No loop is able to follow a leading value which is beyond a physical limit. The power limit of any power module depends on RF input power, transmit frequency, supply voltage and load impedance. The maximum V_{PL} must be matched to the worst case output power and reduced by 1 dB. A distance of 1 dB is necessary because the steepness of the control curve of the power module decreases for higher output power. A wrong behaviour is shown in Fig.10. Curve 1 works fine, but the module is at the power limit. If the supply voltage is reduced now, the theoretical principle of a loop design is violated. Thus the down-ramping in curve 2 starts with a delay followed by an increased steepness. The GSM margin for the switching spectrum will only be met if the maximum value of V_{PL} is matched to the possibilities of the loop.

The programmable $V_{O(INT)}$ limiter (see Table 4) is foreseen to protect the power module during error conditions such as, for example, wrong antenna connection and not to avoid the down-ramping behaviour of curve 2.
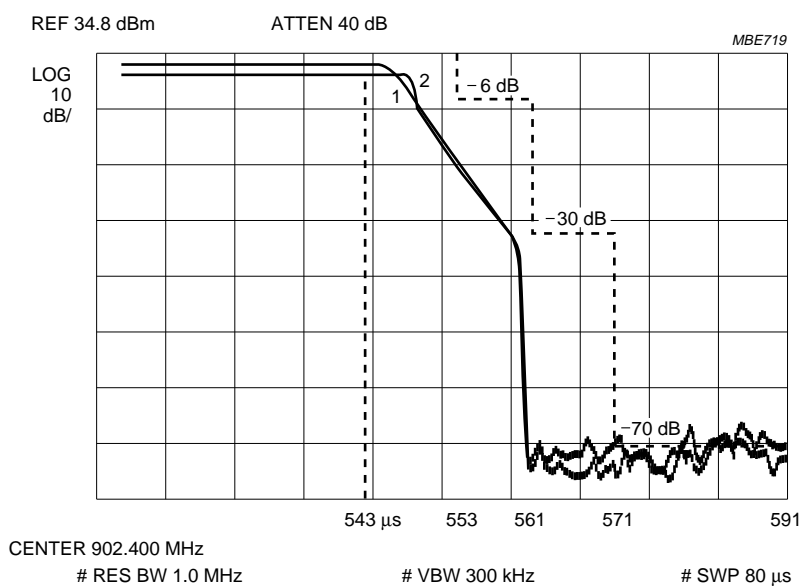
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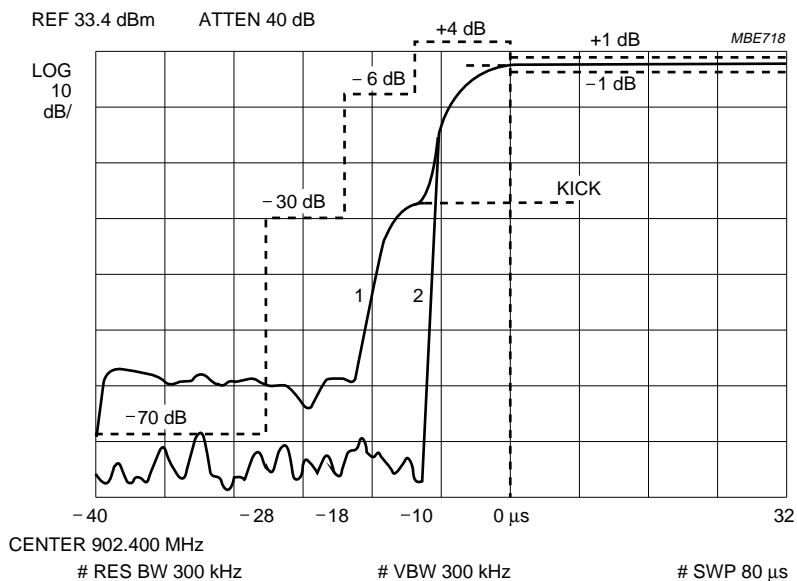
(1) Curve 1: highest usable value.

(2) Curve 2: lowest usable value.

Fig.9 Power as a function of time; rising edge (behaviour at different worst case home positions of $V_{O(INT)}$).

(1) Curve 1: correct behaviour.

(2) Curve 2: unusable behaviour with wrong V_{PL} value.

Fig.10 Power as a function of time, falling edge.
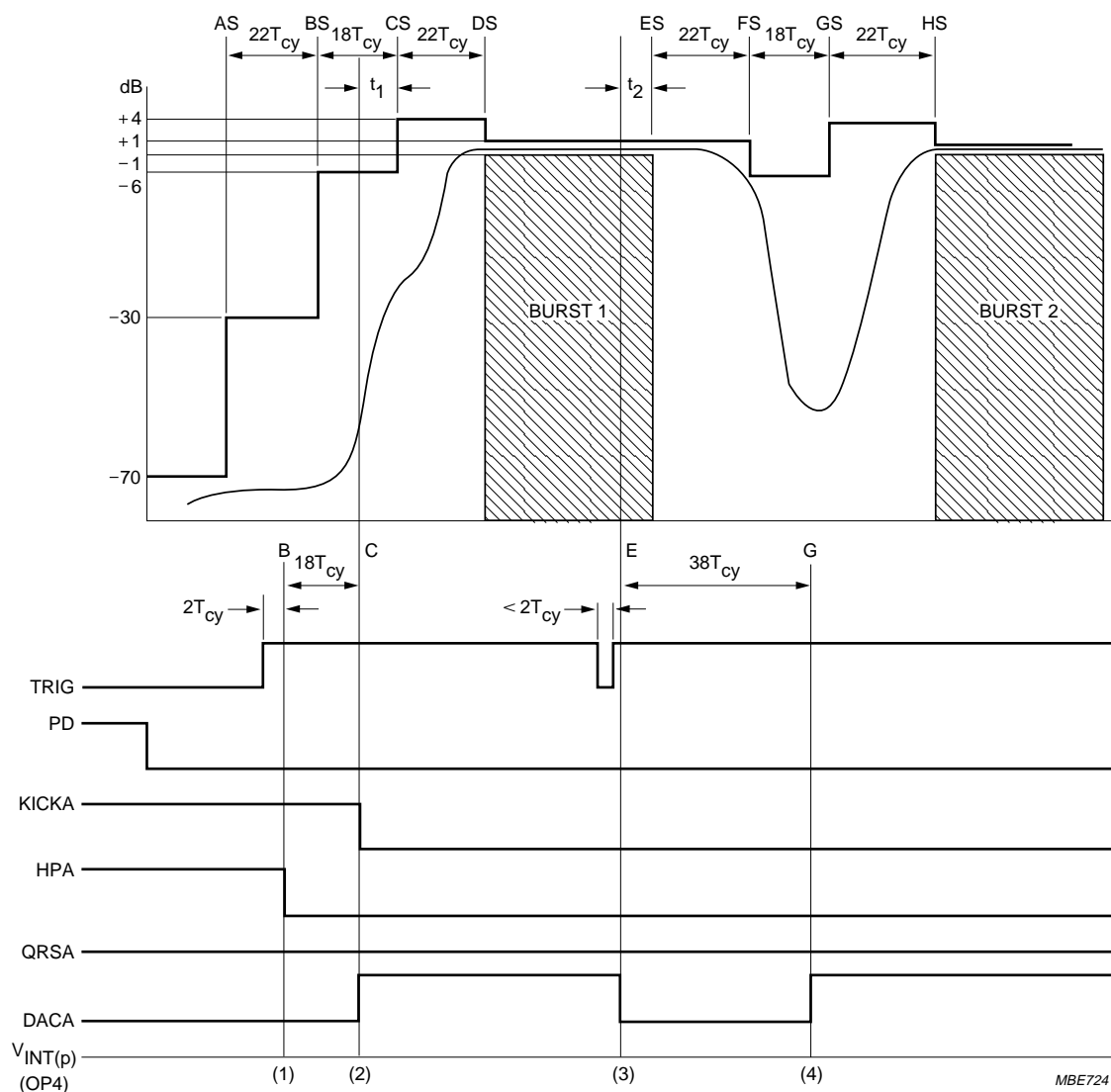
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APPENDIX A: BASE STATION FEATURES

In base station applications a so called 'quick restart' is used and performs the following. When a quick restart condition is detected, which means TRIG goes LOW for a period of less than two clock periods, the integrating controller is not totally turned off. This enables the controller to ramp-up faster after a ramp-down

(see Fig.11). It should be noted that at time 'E' the voltage at the positive input of OP4 is now 100 mV higher than without quick restart, which causes the slower and less steep ramp-down. A normal ramp-up will restart after 38 clock periods. Burst 1 and Burst 2 can have different power levels if the PL register is reprogrammed between time 'E' and 'G'.

(1) $V_{SR} - 2V_{d1} + V_{KICK}$ (start integrator).

(2) $V_{SR} - 2V_{d1} + V_{PL}$

(3) $V_{SR} - 2V_{d1}$

(4) $V_{SR} - 2V_{d1} + V_{PL}$

Fig.11 Base station features timing diagram.

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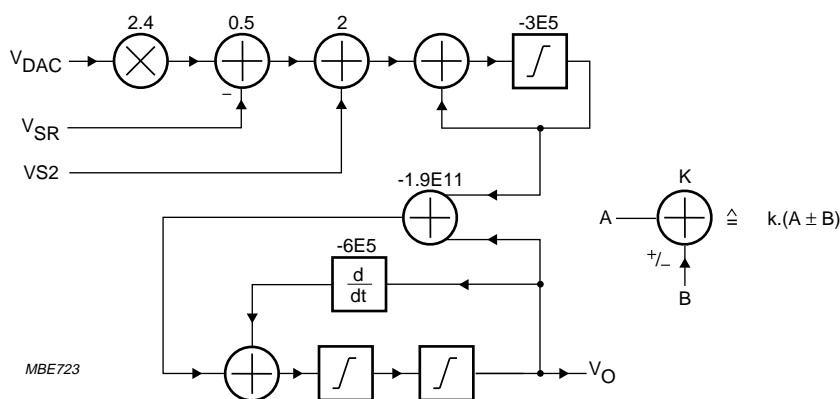
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APPENDIX B: BEHAVIOURAL MODELS

Fig.12 Schematic diagram.

In ESPICE syntax:

```
bm0 gain v(a0) = 2.4 * v(vdac)
bm1 sub v(a1) = 0.5 * (v(a0) − v(VSR))
bm2 add v(a2) = 2.0 * (v(a1) + v(VS2))
bm3 add v(v1) = (v(a2) + v(v2))
bm4 int v(v2) = −3e5 * INT v(v1)
bm5 dif v(v3) = −6e5 *  DIF v(vout)
bm6 add v(v4) = −1.9e11 * (v(vout) + v(v2))
bm7 add v(v5) = (v(v3) + v(v4))
bm8 int v(v6) = INT v(v5)
bm9 int v(vout) = INT v(v6)
```
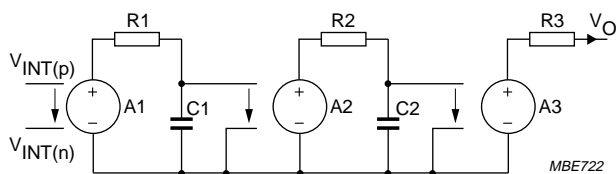
Power amplifier controller for GSM and PCN systems

First pole at 1.7 kHz (typ.) $\rightarrow$ R1 = 1/2/pi/1700; C1 = 1.

Second pole at 7 MHz (typ.) $\rightarrow$ R2 = 1/2/pi/7000000; C1 = 1.

DC gain 72 dB $\rightarrow$ A1 = 3980; A2 = 1; A3 = 1.

R_O = 5 Ω (typ.) $\rightarrow$ R3 = 5 Ω.

A1, A2 and A3 are the gains of voltage controlled voltage sources.

Fig.13 Operational amplifiers 2 and 4 schematic diagram.

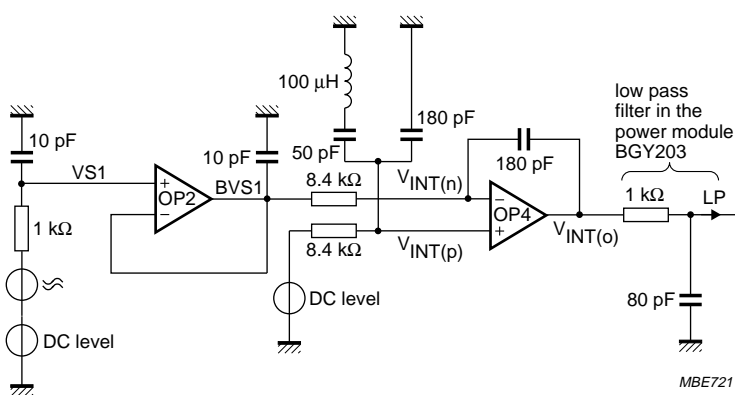**APPENDIX C: AC SIMULATIONS FOR OPERATIONAL AMPLIFIERS 2 AND 4**

Fig.14 Operational amplifiers 2 and 4 circuit diagram.

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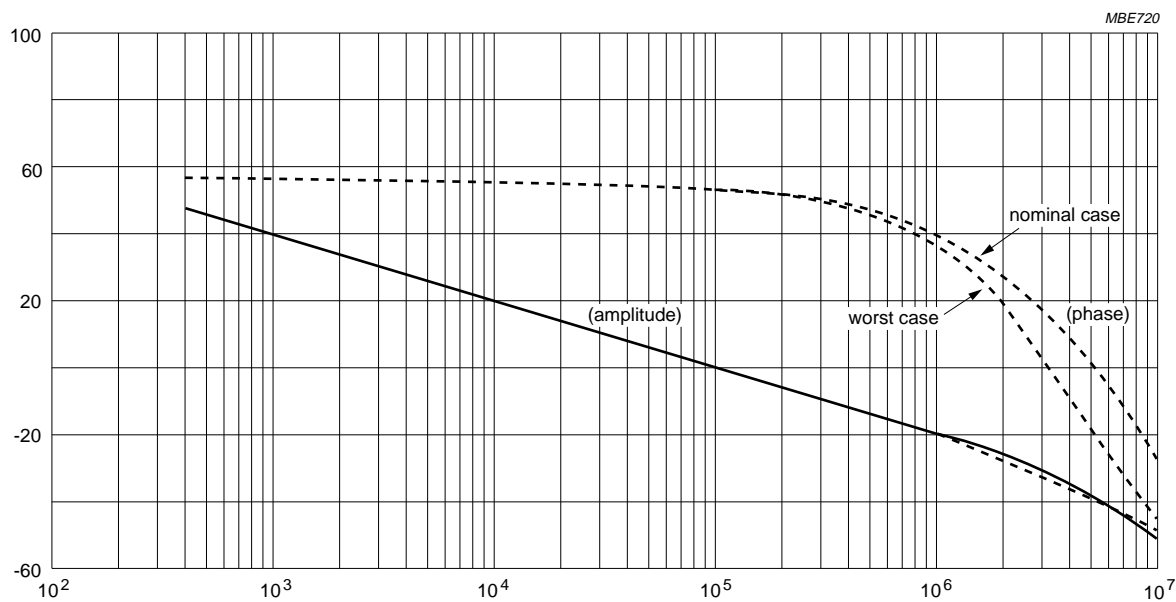The simulation output illustrated in Fig.15 shows the worst and typical cases for the integrator configuration (TRIG HIGH). The signals are drawn for node LP.

Fig.15 Simulation output.