P5 (microarchitecture)

The Intel P5 Pentium family

Produced	From 1993 to 1999
Common manufacturer(s)	• Intel
Max. CPU clock rate	60 MHz to 300 MHz
FSB speeds	50 MHz to 66 MHz
Min. feature size	0.8µm to 0.25µm
Instruction set	x86
Socket(s)	• Socket 4, Socket 5, Socket 7
Core name(s)	• P5. P54C, P54CS, P55C, Tillamook

The original **Pentium** microprocessor was introduced on March 22, 1993.[1][2] Its microarchitecture, deemed **P5**, was Intel's fifth-generation and first superscalar x86 microarchitecture. As a direct extension of the 80486 architecture, it included dual integer pipelines, a faster FPU, wider data bus, separate code and data caches and features for further reduced address calculation latency. In 1996, the **Pentium with MMX Technology** (often simply referred to as **Pentium MMX**) was introduced with the same basic microarchitecture complemented with an MMX instruction set, larger caches, and some other enhancements.

The P5 Pentium competitors included the Motorola 68060 and the PowerPC 601 as well as the SPARC, MIPS, and Alpha microprocessor families, most of which also used a superscalar in-order dual instruction pipeline configuration at some time.

Intel's Larrabee multicore architecture project uses a processor core derived from a P5 core (P54C), augmented by multithreading, 64-bit instructions, and a 16-wide vector processing unit.[3] Intel's low-powered Bonnell microarchitecture employed in Atom processor cores also uses an in-order dual pipeline similar to P5.[4]

Development

The P5 microarchitecture was designed by the same Santa Clara team which designed the 386 and 486.[5] Design work started in 1989;[6] the team decided to use a superscalar architecture, with on-chip cache, floating-point, and branch prediction. The preliminary design was first successfully simulated in 1990, followed by the laying-out of the design. By this time the team had several dozen engineers. The design was taped out, or transferred to silicon, in April 1992, at which point beta-testing began.[7] By mid-1992, the P5 team had 200 engineers.[8] Intel at first planned to demonstrate the P5 in June 1992 at the trade show PC Expo, and to formally announce the processor in September 1992,[9] but design problems forced the demo to be cancelled, and the official introduction of the chip was delayed until the spring of 1993.[10][11]

John H. Crawford, chief architect of the original 386, co-managed the design of the P5,[12] along with Donald Alpert, who managed the architectural team. Dror Avnon managed the design of the FPU.[13] Vinod K. Dham was general manager of the P5 group.[14]

Major improvements over i486 microarchitecture

- *Performance*:
  - Superscalar architecture — The Pentium has two datapaths (pipelines) that allow it to complete two instructions per clock cycle in many cases. The main pipe (U) can handle any instruction, while the other (V) can handle the most common simple instructions. Some RISC proponents had argued that the "complicated" x86 instruction set would probably never be implemented by a tightly pipelined microarchitecture, much less by a dual pipeline design. The 486 and the Pentium demonstrated that this was indeed possible and feasible.
  - 64-bit external databus doubles the amount of information possible to read or write on each memory access and therefore allows the Pentium to load its code cache faster than the 80486; it also allows faster access and storage of 64-bit and 80-bit x87 FPU data.
  - Separation of code and data caches lessens the fetch and operand read/write conflicts compared to the 486. To reduce access time and implementation cost, both of them are 2-way associative, instead of the single 4-way cache of the 486. A related enhancement in the Pentium is the ability to read a contiguous block from the code cache even when it is split between two cache lines (at least 17 bytes in worst case).
  - Much faster floating point unit. Some instructions showed an enormous improvement, most notably FMUL, with up to 15 times higher throughput than in the 80486 FPU. The Pentium is also able to execute a FXCH ST(x) instruction in parallel with an ordinary (arithmetical or load/store) FPU instruction.
  - Four-input address-adders enables the Pentium to further reduce the address calculation latency compared to the 80486. The Pentium can calculate full addressing modes with *segment-base* + *base-register* + *scaled register* + *immediate offset* in a single cycle; the 486 has a three-input address-adder only, and must therefore divide such calculations between two cycles.
  - The microcode can employ both pipelines to enable auto-repeating instructions such as rep movsw perform one iteration every clock cycle, while the 80486 needed three clocks per iteration (and the earliest x86-chips significantly more than the 486). Also, optimization of the access to the first microcode words during the decode stages helps in making several frequent instructions execute significantly more quickly, especially in their most common forms, and in typical cases. Some examples are (486→Pentium, in clock cycles): CALL (3→1), RET (5→2), *shifts/rotates* (2~3→1), etc.
  - A faster, fully hardware-based multiplier makes instructions such as MUL and IMUL several times as fast (and more predictable) than in the 80486; the execution time is reduced from 13~42 clock cycles down to 10~11 for 32-bit operands.
  - Virtualized interrupt to speed up virtual 8086 mode.
- *Other features*:
  - Enhanced debug features with the introduction of the Processor-based debug port (See *Pentium Processor Debugging* in the Developers Manual, Vol 1).
  - Enhanced self test features like the L1 cache parity check (see *Cache Structure* in the Developers Manual, Vol 1).
- The later **Pentium MMX** also added the MMX instruction set, a basic integer SIMD instruction set extension marketed for use in multimedia applications. MMX could not be used simultaneously with the x87 FPU instructions because the registers were reused (to allow for fast context switches). More important enhancements were the doubling of the instruction and data cache sizes and a few microarchitectural changes for better performance.

The Pentium was designed to execute over 100 million instructions per second (MIPS),[15] and the 75 MHz model was able to reach 126.5 MIPS in certain benchmarks.[16] The Pentium architecture typically offered just under twice the performance of a 486 processor per clock cycle in common benchmarks. The fastest 80486 parts (with slightly improved microarchitecture and 100 MHz operation) were almost as powerful as the first-generation Pentiums, and the AMD Am5x86 was roughly equal to the Pentium 75 regarding pure ALU performance.

Bugs and problems

The early versions of 60-100 MHz P5 Pentiums had a problem in the floating point unit that resulted in incorrect (but predictable) results from some division operations. This bug, discovered in 1994 by professor Thomas Nicely at Lynchburg College, Virginia, became known as the Pentium FDIV bug and caused embarrassment for Intel, which created an exchange program to replace the faulty processors. Soon afterwards, a bug was discovered which could allow a malicious program to crash a system without any special privileges (the "f00f" bug); fortunately, operating systems were able to implement workarounds to prevent crashes.

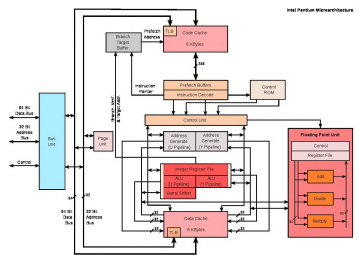
The 60 and 66 MHz 0.8 µm versions of the P5 Pentium processors also had (for the time) high heat production due to their 5V operation, and were often known colloquially as "coffee warmers" or some similar nickname. The P54C used 3.3V and had significantly lower power draw (a quadratic relationship). P5 Pentiums used Socket 4, while P54C started out on Socket 5 before moving to Socket 7 in later revisions. All desktop Pentiums from P54CS onwards used Socket 7.

Cores and steppings

The Pentium was Intel's primary microprocessor for personal computers during the mid-1990s. The original design was reimplemented in newer processes and new features were added to maintain its competitiveness as well as to address specific markets such as portable computers. As a result, there were several variants of the P5 microarchitecture.

P5

The first Pentium microprocessor core was code-named "P5". Its product code was 80501 (80500 for the earliest steppings). There were two versions, specified to operate at 60 MHz and 66 MHz respectively. This first implementation of the Pentium used a traditional 5 Volt power supply (descended from the usual TTL logic compatibility requirements). It contained 3.1 million transistors and measured 16.7 mm by 17.6 mm for an area of 293.92 mm^2.[17] It was fabricated in a 0.8 µm BiCMOS process. The 5 volt design resulted in relatively high energy consumption for its operating frequency compared to the later models.



Intel Pentium microarchitecture.

P54C

The P5 was followed by the P54C (80502); there were versions specified to operate at 75, 90, or 100 MHz using a 3.3 volt power supply. This was the first Pentium processor to operate at a 3.3 volts, reducing energy consumption. It employed an internal clock multiplier to let the internal circuitry work at a higher frequency than the external address and data buses, as it is more complicated and cumbersome to increase the external frequency, due to physical constraints. It also allowed two-way multiprocessing and had new power management features as well as an on chip 8259-compatible interrupt controller. It contained 3.3 million transistors and measured 163 mm^2.[18] It was fabricated in a BiCMOS process which has been described as both 0.5 µm and 0.6 µm due to differing definitions.[18]

P54CQS

The P54C was followed by the P54CQS which operated at 120 MHz. It was fabricated in a 0.35 µm BiCMOS process and was the first commercial microprocessor to be fabricated in a 0.35 µm process.[18] Its transistor count is identical to the P54C and, despite the newer process, it had an identical die area as well. The chip was connected to the package using wire bonding, which only allows connections along the edges of the chip. A smaller chip would have required a redesign of the package, as there is a limit on the length of the wires and the edges of the chip would be further away from the pads on the package. The solution was to keep the chip the same size, retain the existing pad-ring, and only reduce the size of the Pentium's logic circuitry to enable it to achieve higher clock frequencies.[18]

P54CS

The P54CQS was followed by the P54CS, which operated at 133, 150, 166 and 200 MHz. It contained 3.3 million transistors, measured 90 mm^2 and was fabricated in a 0.35 µm BiCMOS process with four levels of interconnect.

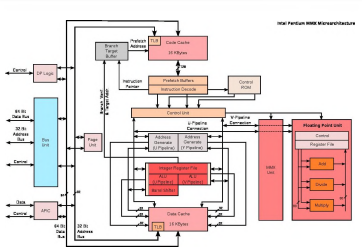
P24T

Further information: Pentium OverDrive

The P24T Pentium OverDrive for 486-systems were released in 1995, which were based on 3.3V 0.6 µm versions using a 63 or 83 MHz clock. Since these used Socket 2/3, some modifications had to be made to compensate for the 32-bit data bus and slower on-board L2 cache of 486-motherboards. They were therefore equipped with a 32KB L1 cache (double that of pre-P55C Pentium CPUs).

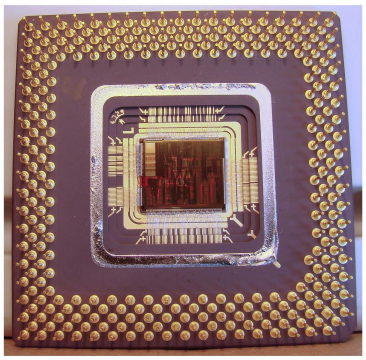
P55C

The P55C (or 80503) was developed by Intel's Research & Development Center in Haifa, Israel. It was sold as **Pentium with MMX Technology** (usually just called **Pentium MMX**); although it was based on the P5 core, it featured a new set of 57 "MMX" instructions intended to improve performance on multimedia tasks, such as encoding and decoding digital media data. The Pentium MMX line was introduced on 22 October 1996.[19]



Intel Pentium MMX microarchitecture.

The new instructions work on new data types: 64-bit packed vectors of either eight 8-bit integers, four 16-bit integers, two 32-bit integers, or one 64-bit integer. So, for example, the PADDUSB (Packed ADD Unsigned Saturated Byte) instruction adds two vectors, each containing eight 8-bit unsigned integers together, pairwise; each addition that would overflow *saturates*, yielding 255, the maximum unsigned value that can be represented in a byte. These rather specialized instructions generally require special coding by the programmer for them to be used. The performance of the P55C was improved over previous versions by a doubling of the Level 1 CPU cache from 16 KB to 32 KB.



Pentium MMX 166 MHz without cover

It contained 4.5 million transistors and had an area of 140 mm^2. It was fabricated in a 0.28 µm CMOS process with the same metal pitches as the previous 0.35 µm BiCMOS process, so Intel described it as "0.35 µm" because of its similar transistor density.[20] The process has four levels of interconnect.[20]

While the P55C is compatible with the common Socket 7 motherboard configuration, the voltage requirements for powering the chip differ from the standard Socket 7 specifications. Most motherboards manufactured for Socket 7 prior to the establishment of the P55C standard are not compliant with the dual intensity required for proper

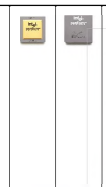
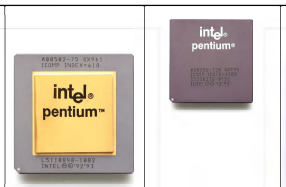
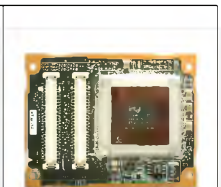
operation of this chip. Intel temporarily manufactured an upgrade kit called the OverDrive that was designed to correct this lack of planning on the motherboard makers part.

Tillamook

Pentium MMX notebook CPUs used a "mobile module" that held the CPU. This module was a PCB with the CPU directly attached to it in a smaller form factor. The module snapped to the notebook motherboard and typically a heat spreader was installed and made contact with the module. However, with the 0.25 µm *Tillamook* Mobile Pentium MMX (named after a city in Oregon), the module also held the 430TX chipset along with the system's 512 KB SRAM cache memory.

Models and variants

Pentium and Pentium with MMX Technology

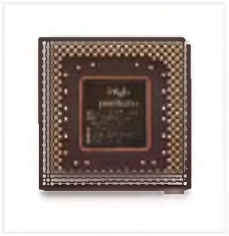
						
Code name	P5	P54C	P54CS	P55C		*Tillamook*
Product code	80500/ 80501	80502		80503		
Process size (µm)	0.80	0.60 or 0.35*	0.35	0.35 (later 0.28)		0.25
Socket	Socket 4	Socket 5/7		Socket 7		
Package	CPGA	CPGA/TCP*	CPGA/PPGA/TCP*	CPGA/PPGA/TCP*		TCP/TCP on MMC-1
Clock speed (MHz)	60 66	75 90 100 120	133 150 166 200	120* 133* 150* 166 200 233		200 233 266 300
Bus speed (MHz)	60 66	50 60 66 60	66 60 66	60 66 60 66		
Voltage	5.0 5.0	3.3 2,9* 3,3 2,9* 3,3 3,1* 2,9* 3.3 3.1* 2.9*	3.3 3.1* 2.9* 3,3 3,1* 2,9* 3.3 3.3	2.8 2.45 2.45 2.8 2.8 2.8		1.8 1.8 2.0 2.0
Introduced	1993-03-22	1994-10-10 1994-03-07 1995-03-27	1995-06-12 1996-01-04 1996-06-10	1997-10-20 1997-05-19 1997-01-08 1997-06-02		1997-08 1998-01 1999-01

An asterisk indicates that these were only available as Mobile Pentium or Mobile Pentium MMX chips for laptops.

Pentium OverDrive with MMX Technology

						
Code name	P54CTB					
Product code	PODPMT60X150		PODPMT66X166	PODPMT60X180		PODPMT66X200
Process size (µm)	0.35					
Socket	Socket 5/7					
Package	CPGA with heatsink, fan and voltage regulator					
Clock speed (MHz)	125	150	166	150	180	200
Bus speed (MHz)	50	60	66	50	60	66
Upgrade for	Pentium 75	Pentium 90	Pentium 100 and 133	Pentium 75	Pentium 90, 120 and 150	Pentium 100, 133 and 166
TDP (max. W)	15.6		15.6	15.6		18
Voltage	3.3		3.3	3.3		3.3

Embedded versions of Pentium with MMX Technology

							
Code name	P55C		*Tillamook*				
Product code	FV8050366200	FV8050366233	FV80503CSM66166	GC80503CSM66166	GC80503CS166EXT	FV80503CSM66266	GC80503CSM66266
Process size (µm)	0.35		0.25				
Clock speed (MHz)	200	233	166	166	166	266	266
Bus speed (MHz)	66	66	66	66	66	66	66
Package	PPGA	PPGA	PPGA	BGA	BGA	PPGA	BGA
TDP (max. W)	15.7	17	4.5	4.1	4.1	7.6	7.6
Voltage	2.8	2.8	1.9	1.8	1.8	1.9	2.0

References

[1] *View Processors Chronologically by Date of Introduction:* (http://www.intel.com/pressroom/kits/quickrefyr.htm#1993), Intel, , retrieved 2007-08-14

[2] *Intel Pentium Processor Family* (http://www.intel.com/pressroom/kits/quickreffam.htm#pentium), Intel, , retrieved 2007-08-14

[3] §3 of Seiler, L.; Carmean, D.; Sprangle, E.; Forsyth, T.; Abrash, M.; Dubey, P.; Junkins, S.; Lake, A. et al (August 2008). "Larrabee: A Many-Core x86 Architecture for Visual Computing" (http://softwarecommunity.intel.com/UserFiles/en-us/File/larrabee_manycore.pdf) (PDF). *ACM Transactions on Graphics*. Proceedings of ACM SIGGRAPH 2008 **27** (3): 18:11–18:11. doi:10.1145/1360612.1360617. ISSN 0730-0301. . Retrieved 2008-08-06.

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[7] "The hot new star of microchips" (http://www.iptegrity.com/index.php?option=com_content&task=view&id=34&Itemid=42), Monica Horten, *New Scientist*, #1871, pp. 31 ff., May 1, 1993. Accessed on line June 9, 2009.

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[9] p. 8, "Intel to offer a peek at its `586' chip", Tom Quinlan, *InfoWorld*, March 16, 1992.

[10] p. 1, "Design woes force Intel to cancel 586 chip demo", Tom Quinlan and Cate Corcoran, *InfoWorld* **14**, #24, June 15, 1992.

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[12] p. 54, "Intel Turns 35: Now What?", David L. Margulius, *InfoWorld*, July 21, 2003, ISSN 0199-6649.

[13] p. 21, " Architecture of the Pentium microprocessor (http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=216745)", D. Alpert and D. Avnon, *IEEE Micro*, **13**, #3 (June 1993), pp. 11–21, doi:10.1109/40.216745.

[14] p. 90, "Inside Intel", *Business Week*, #3268, June 1. 1992.

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[16] http://www.islandnet.com/~kpolsson/micropro/proc1994.htm

[17] Case, Brian (29 March 1993). "Intel Reveals Pentium Implementation Details". *Microprocessor Report*.

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[20] Slater, Michael (5 March 1996). "Intel's Long-Awaited P55C Disclosed". *Microprocessor Report*.

External links

- CPU-Collection.de (http://www.cpu-collection.de/?tn=0&l0=co&l1=Intel&l2=Pentium P54) - Intel Pentium images and descriptions
- Plasma Online Intel CPU Identification (http://www.plasma-online.de/english/identify/picture/intel_cpu.html)
- Pictures of all known Pentium chips at chipdb.org (http://www.chipdb.org/cat-pentium-417.htm)
- The Pentium Timeline Project (http://www.chipdb.org/index.php?template=timeline) The Pentium Timeline Project maps oldest and youngest chip known of every s-spec made. Data are shown in a interactive timeline.

Intel Datasheets

- Pentium (P5) (http://datasheets.chipdb.org/Intel/x86/Pentium/24159502.pdf)
- Pentium (P54) (http://datasheets.chipdb.org/Intel/x86/Pentium/24199710.PDF)
- Pentium MMX (P55C) (http://datasheets.chipdb.org/Intel/x86/Pentium MMX/24318504.PDF)
- Mobile Pentium MMX (P55C) (http://datasheets.chipdb.org/Intel/x86/Pentium MMX/24329204.PDF)
- Mobile Pentium MMX (Tillamook) (http://datasheets.chipdb.org/Intel/x86/Pentium MMX/24346802.PDF)

Intel Manuals

These Manuals do provide a overview of the Pentium Processor and its features:

- Pentium Processor Family Developer's Manual Pentium Processor (Volume 1) (http://download.intel.com/design/intarch/manuals/24142805.pdf) (Intel Order Number 241428)
- Pentium Processor Family Developer's Manual Volume 2: Instruction Set Reference (ftp://download.intel.com/design/pentium/manuals/24319101.PDF) (Intel Order Number 243191)
- Pentium Processor Family Developer's Manual Volume 3: Architecture and Programming Manual (ftp://download.intel.com/design/pentium/manuals/24143004.pdf) (Intel Order Number 241430)