

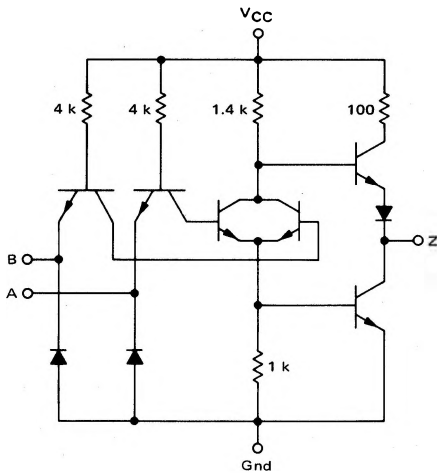
QUAD 2-INPUT "NOR" GATE

MC5400/7400 series

MC5402 • MC7402

Add Suffix F for TO-86 ceramic package (Case 607).  
 Suffix L for TO-116 ceramic package (Case 632).  
 Suffix P for TO-116 plastic package (Case 605) MC7402 only.

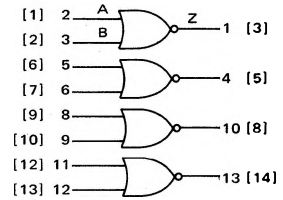
CIRCUIT SCHEMATIC  
 1/4 OF CIRCUIT SHOWN



VCC = Pin 14 [4]  
 Gnd = Pin 7 [11]

[FLAT  
 Pkg  
 Pin]

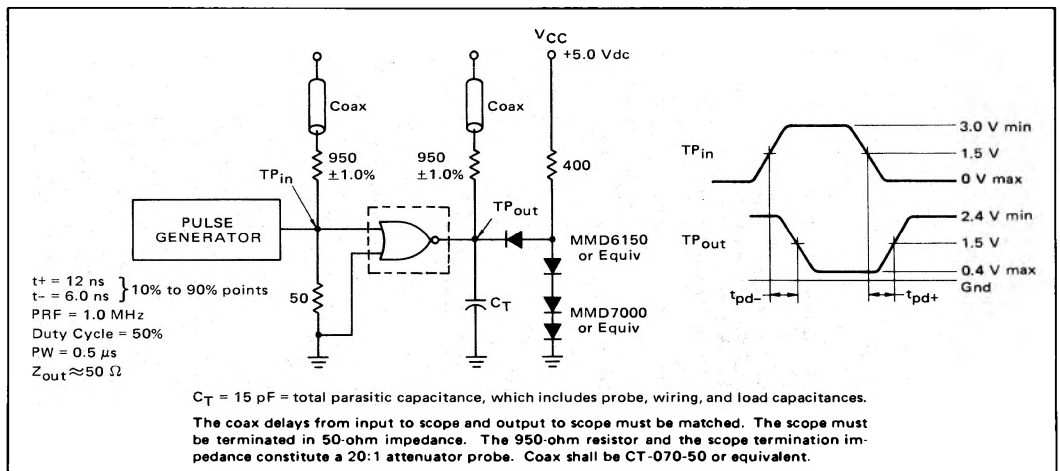
DIL  
 Pkg  
 Pin



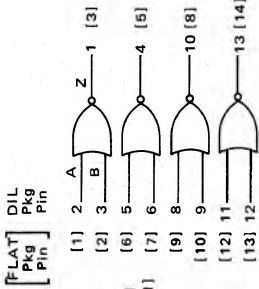
Positive Logic:  $Z = \overline{A + B}$   
 Negative Logic:  $Z = \overline{A \cdot B}$

Input Loading Factor = 1  
 Output Loading Factor = 10  
 Total Power Dissipation = 40 mW typ/pkg  
 Propagation Delay Time = 10 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC5402, MC7402 (continued)



V = V<sub>CC</sub> = Pin 14 [4]  
Gnd = Pin 7 [11]

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

Characteristic	Symbol	Pin Under Test	MC5402 Test Limits -55 to +125°C				MC7402 Test Limits 0 to +70°C				TEST CURRENT/VOLTAGE VALUES (All Temperatures)													Gnd						
			Min	Max	Unit	Min	Max	Unit	Volts																					
			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																											
Input Forward Current	I <sub>F</sub>	A	-	-1.6	mAdc	-	-1.6	mAdc	V <sub>IL</sub>	0.4	2.4	5.5	4.5	4.5	5.0	5.0	0.8	0.8	5.0	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>	*	
		A	-	40	µAdc	-	40	µAdc	V <sub>OL</sub>	16	0.4	2.4	5.5	4.5	4.5	5.0	2.0	2.0	5.0	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>		
Leakage Current	I <sub>R1</sub>	A	-	40	µAdc	-	40	µAdc	V <sub>OL</sub>	16	0.4	2.4	5.5	4.5	4.5	5.0	2.0	2.0	5.0	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>	B*	
		A	-	1.0	mAdc	-	1.0	mAdc	V <sub>OL</sub>	16	0.4	2.4	5.5	4.5	4.5	5.0	2.0	2.0	5.0	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>		
Output Output Voltage	V <sub>OL</sub>	Z	-	0.4	Vdc	-	0.4	Vdc	V <sub>OL</sub>	-	-	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>	B*	
		Z	2.4	-	Vdc	2.4	-	Vdc	V <sub>OH</sub>	-	-	-	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>		V <sub>CCH</sub>
Short-Circuit Current	I <sub>SC</sub> †	Z	-20	-55	mAdc	-18	-55	mAdc	V <sub>OL</sub>	-	-	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>	Z, A, B*	
Power Requirements (Total Device) Power Supply Drain	I <sub>PDH</sub>	V	-	27	mAdc	-	27	mAdc	V <sub>OL</sub>	-	-	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>	A*	
		V	-	16	mAdc	-	16	mAdc	V <sub>OL</sub>	-	-	-	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>		V <sub>CCH</sub>
Switching Parameters Turn-On Delay	t <sub>pd-</sub>	A, Z	-	15**	ns	-	15**	ns	Pulse In	A	Z	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>	A*	
		A, Z	-	22**	ns	-	22**	ns	Pulse Out	A	Z	-	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>		V <sub>CCH</sub>
Turn-Off Delay	t <sub>pd+</sub>	A, Z	-	22**	ns	-	22**	ns	Pulse In	A	Z	-	-	-	-	-	-	-	-	-	V <sub>R2</sub>	V <sub>R1</sub>	V <sub>IHH</sub>	V <sub>IH</sub>	V <sub>IH1</sub>	V <sub>IH0</sub>	V <sub>CC</sub>	V <sub>CCL</sub>	V <sub>CCH</sub>	A*

\*Ground inputs to gates not under test.

\*\*Tested only at 25°C.

†Only one output should be shorted at a time.

Pin 7 [11] is grounded for all tests in addition to the pins listed below: