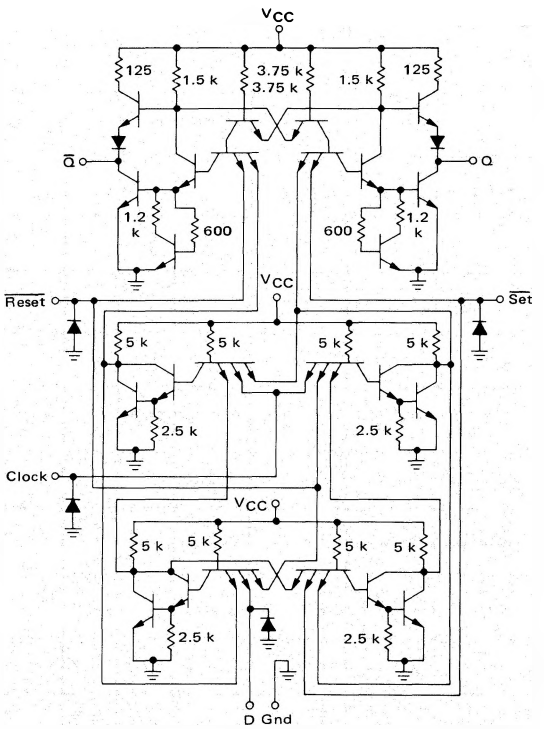
DUAL TYPE D FLIP-FLOP

MC5479 • MC7479

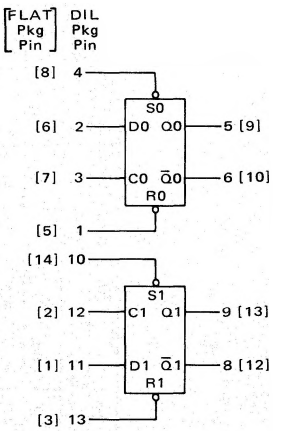
Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7479 only.)

CIRCUIT SCHEMATIC
1/2 OF DEVICE SHOWN



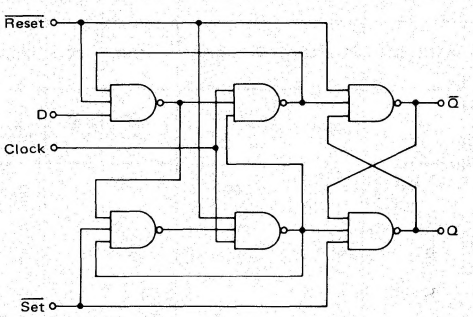
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

This dual type D flip-flop triggers on the positive edge of the clock input. During the clock transition the state of the D input is transferred to the Q output. The device is useful in shift registers and simple counters.



t_n	t_{n+1}	
D	Q	$\bar{Q}$
0	0	1
1	1	0

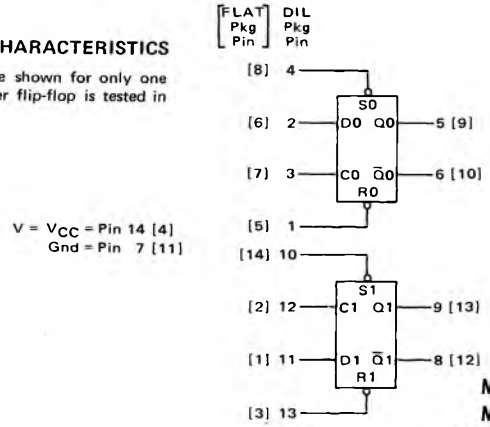
Input Loading Factor:
D = 1
$\overline{\text{Set}}$, Clock = 2
$\overline{\text{Reset}}$ = 3
Output Loading Factor = 10
Total Power Dissipation = 84 mW typ/pkg
Propagation Delay Time = 16 ns typ
Operating Frequency = 30 MHz typ



LOGIC DIAGRAM
1/2 OF DEVICE SHOWN

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
mA		Volts								
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}
16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.50	5.50
16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25

MC5479
MC7479

Pin 7[11] is grounded for all tests in addition to the pins listed below:

Characteristic	Symbol	Pin Under Test	MC5479 Test Limits −55 to +125°C Min	Max	Unit	MC7479 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																				
Forward Current D	I_F	D	-	-1.6	mAdc	-	-1.6	mAdc	-	-	D	-	-	R,S	-	-	-	-	V	C0,C1
$\overline{\text{Set}}$		S	-	-3.2	↓	-	-3.2	↓	-	-	S	-	-	R	-	-	-	-	↓	C0,C1,D0
$\overline{\text{Reset}}$		R	-	↓	↓	-	↓	↓	-	-	R	-	-	D,S	-	-	-	-		C0,C1
Clock		C	-	↓	↓	-	↓	↓	-	-	C	-	-	R	-	-	-	-	↓	C1,D0,S0
Leakage Current D	I_{R1}	D	-	40	μAdc	-	40	μAdc	-	-	-	D	-	C,S	-	-	-	-	V	C1,R0
$\overline{\text{Set}}$		S	-	80	↓	-	80	↓	-	-	-	S	-	C*,D,R	-	-	-	-	↓	C1
$\overline{\text{Reset}}$		R	-	120	↓	-	120	↓	-	-	-	R	-	C*,S	-	-	-	-		C1, D0
Clock		C	-	80	↓	-	80	↓	-	-	-	C	-	S	-	-	-	-	↓	C1,D0,R0
D	I_{R2}	D	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	D	C,S	-	-	-	-	V	C1,R0
$\overline{\text{Set}}$		S	-	↓	↓	-	↓	↓	-	-	-	-	S	C*,D,R	-	-	-	-	↓	C1
$\overline{\text{Reset}}$		R	-	↓	↓	-	↓	↓	-	-	-	-	R	C*,S	-	-	-	-		C1,D0
Clock		C	-	↓	↓	-	↓	↓	-	-	-	-	C	S	-	-	-	-	↓	C1,D0,R0
Output																				
Output Voltage	V_{OL}	Q	-	0.4	Vdc	-	0.4	Vdc	Q	-	-	-	-	-	S	R	-	V	-	C0,C1,D0
		$\bar{Q}$	-	0.4	Vdc	-	0.4	Vdc	$\bar{Q}$	-	-	-	-	-	R	S	-	V	-	C0,C1,D0
	V_{OH}	Q	2.4	-	Vdc	2.4	-	Vdc	-	Q	-	-	-	-	R	S	-	V	-	C0,C1,D0
		$\bar{Q}$	2.4	-	Vdc	2.4	-	Vdc	-	$\bar{Q}$	-	-	-	-	S	R	-	V	-	C0,C1,D0
Short-Circuit Current	I_{SC}†	Q	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	V	C0,S0,Q0
		$\bar{Q}$	-20	-57	mAdc	-18	-57	mAdc	-	-	-	-	-	-	-	-	-	-	V	C1,R0,Q0
Power Requirements (Total Device)																				
Power Supply Drain	I_{PD}	V	-	30	mAdc	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	V	C0,C1,D0,D1,S0,S1
		V	-	30	mAdc	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	V	C0,D0,R0,C1,D1,R1

*Momentarily ground pin prfor to taking measurement, then set to state indicated.

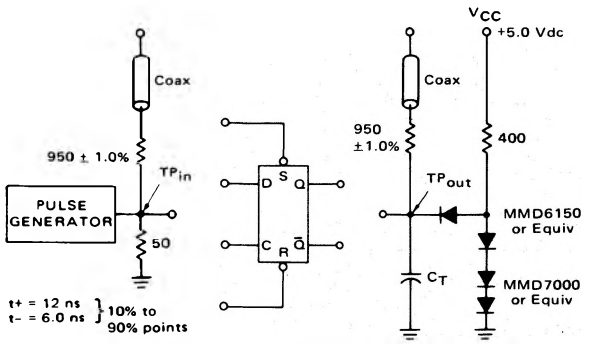
†Only one output should be shorted at a time.

OPERATING CHARACTERISTICS

Data may be applied to the D input any time following 5.0 ns after the leading edge of a clock pulse and 20 ns before the leading edge of the following clock pulse. The state of the D input when the clock changes from the positive logic "0" state to the positive logic "1" state is transferred to the Q output of the flip-flop. The data input cannot be changed between the setup time (20 ns) and the hold time (5.0 ns) without adversely affecting the operation of the flip-flop.

The direct $\overline{\text{Set}}$ and $\overline{\text{Reset}}$ inputs override the clock, and may be applied any time during the operating cycle.

SWITCHING TIME TEST CIRCUIT



PRF = 20 MHz for waveform 1
= 1.0 MHz for waveforms 2 thru 5

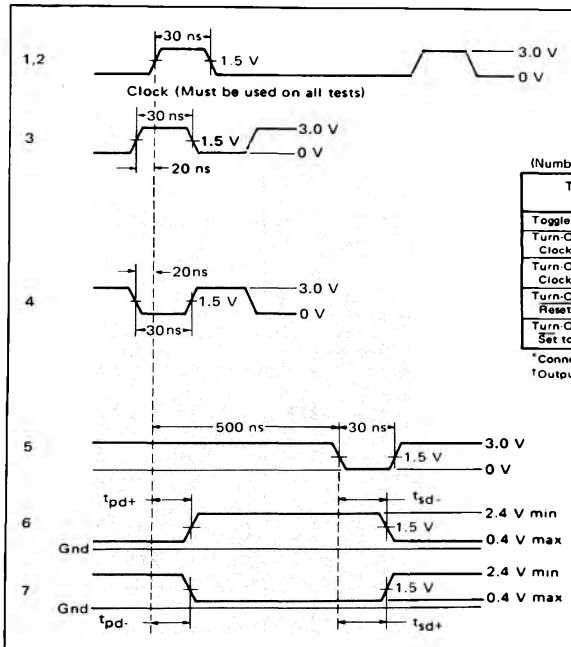
$Z_{out} \approx 50\ \Omega$

Two pulse generators are required and must be slaved together to provide the waveforms shown. Only one pulse generator (duty cycle = 50%) is required to test toggle frequency.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

(Numbers shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				Q	Q̄	LIMITS		
		C	D	R̄	S̄			Min	Max	Unit
Toggle Frequency	f_{Tog}	1	*	2.4 V	2.4 V	↑	↑	20	–	MHz
Turn-On Delay Clock to Q	t_{pd-}	2	4	2.4 V	2.4 V	7	6	–	30	ns
Turn-Off Delay Clock to Q	t_{pd+}	2	3	2.4 V	2.4 V	6	7	–	30	ns
Turn-On Delay $\overline{\text{Reset}}$ to Q	t_{sd-}	2	3	5	2.4 V	7	6	–	25	ns
Turn-Off Delay $\overline{\text{Set}}$ to Q	t_{sd+}	2	4	2.4 V	5	6	7	–	25	ns

*Connect to Q̄.
†Output shall toggle with each input pulse.