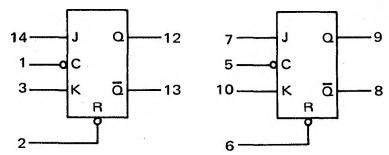
DUAL J-K FLIP-FLOP

MC5473 • MC7473

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7473 only.



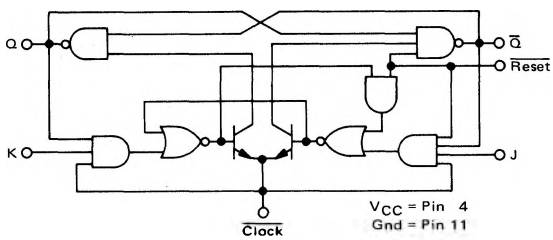
This negative-edge-clocked dual J-K flip-flop operates on the master-slave principle. The device is quite useful for simple registers and counters where multiple J and K inputs are not required.

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Input Loading Factor:
J, K = 1
$\overline{\text{Reset}}$, $\overline{\text{Clock}}$ = 2

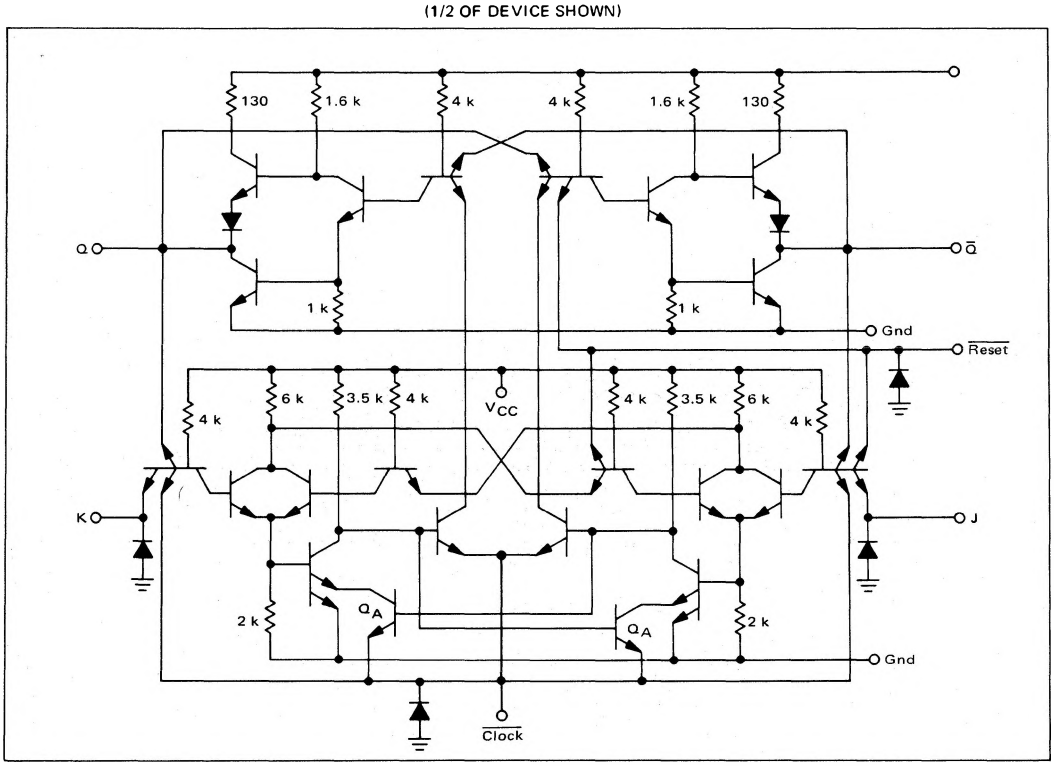
Output Loading Factor = 10
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 30 ns typ
Operating Frequency = 15 MHz typ

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



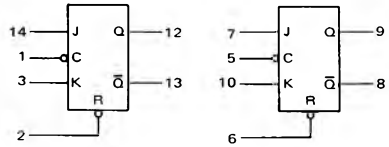
Pin numbers are the same in all packages.

LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



V = V_{CC} = Pin 4
Gnd = Pin 11

	TEST CURRENT/VOLTAGE VALUES (All Temperatures)													
	mA		Volts											
	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}			
MC5473	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.50	5.50			
MC7473	16	-0.4	0.4	2.4	5.5	4.5	2.0	0.8	5.0	4.75	5.25			

Characteristic	Symbol	Pin Under Test	MC5473 Test Limits −55 to +125°C Min	Max	Unit	MC7473 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{th1}	V_{th0}	V_{CC}	V_{CCL}	V_{CCH}	**	Pin 11 is grounded for all tests in addition to the pins listed below: Gnd
Input																					
Forward Current J	I_F	J	-	-1.6	mAdc	-	-1.6	mAdc	-	-	J	-	-	C,R	-	-	-	-	V	Q	-
K		K	-	-1.6	↓	-	-1.6	↓	-	-	K	-	-	C,R	-	-	-	-	↓	$\bar{Q}$	-
$\overline{\text{Reset}}$		R	-	-3.2		-	-3.2		-	-	R	-	-	C,J	-	-	-	-		-	-
$\overline{\text{Clock}}$		C	-	-3.2	↓	-	-3.2	↓	-	-	C	-	-	J,K,R	-	-	-	-	↓	R	-
Leakage Current J	I_{R1}	J	-	40	μAdc	-	40	μAdc	-	-	-	J	-	-	-	-	-	-	V	-	C,R*
K		K	-	40	↓	-	40	↓	-	-	-	K	-	R	-	-	-	-	↓	R	C*
$\overline{\text{Reset}}$		R	-	80		-	80		-	-	-	R	-	-	-	-	-	-		$\bar{Q}$	C,J*
$\overline{\text{Clock}}$		C†	-	80	↓	-	80	↓	-	-	-	C	-	-	-	-	-	-	↓	-	J*,K,R
J	I_{R2}	J	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	J	-	-	-	-	-	V	-	C,R*
K		K	-	↓	↓	-	↓	↓	-	-	-	-	K	R	-	-	-	-	↓	R	C*
$\overline{\text{Reset}}$		R	-			-			-	-	-	-	R	-	-	-	-	-		$\bar{Q}$	C,J*
$\overline{\text{Clock}}$		C	-	↓	↓	-	↓	↓	-	-	-	-	C	-	-	-	-	-	↓	-	J*,K,R
Output																					
Output Voltage	V_{OL}	Q	-	0.4	Vdc	-	0.4	Vdc	Q	-	-	-	-	-	-	R	-	V	-	-	C,J*,K
		$\bar{Q}$	-	0.4	Vdc	-	0.4	Vdc	$\bar{Q}$	-	-	-	-	-	R	-	-	V	-	$\bar{Q}$	C,J*,K
	V_{OH}	Q	2.4	-	Vdc	2.4	-	Vdc	-	Q	-	-	-	-	-	-	-	V	-	$\bar{Q}$	C,J*,K
		$\bar{Q}$	2.4	-	Vdc	2.4	-	Vdc	-	$\bar{Q}$	-	-	-	-	-	R	-	V	-	-	C,J*,K
Short-Circuit Current	I_{SC}‡	Q	-20	-57	mAdc	-18	-57	mAdc	-	-	-	C,J,K	-	-	-	-	-	-	V	-	Q,$\bar{Q}$*
		$\bar{Q}$	-20	-57	mAdc	-18	-57	mAdc	-	-	-	C,J,K	-	-	-	-	-	-	V	-	R,$\bar{Q}$*
Power Requirements (Total Device)																					
Power Supply Drain	I_{PD}	V	-	40	mAdc	-	40	mAdc	-	-	-	-	-	-	-	-	-	-	V	-	Both R Inputs
		V	-	40	mAdc	-	40	mAdc	-	-	-	-	-	-	-	-	-	-	V	Both $\bar{Q}$	-

*Ground inputs to flip-flop not under test.

**Momentarily ground pin prior to taking measurement to set flip-flop in the desired state. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

‡Only one output should be shorted at a time.

†Under normal operating conditions this current is negative. This test guarantees that positive leakage current will not exceed the limit shown.

OPERATING CHARACTERISTICS

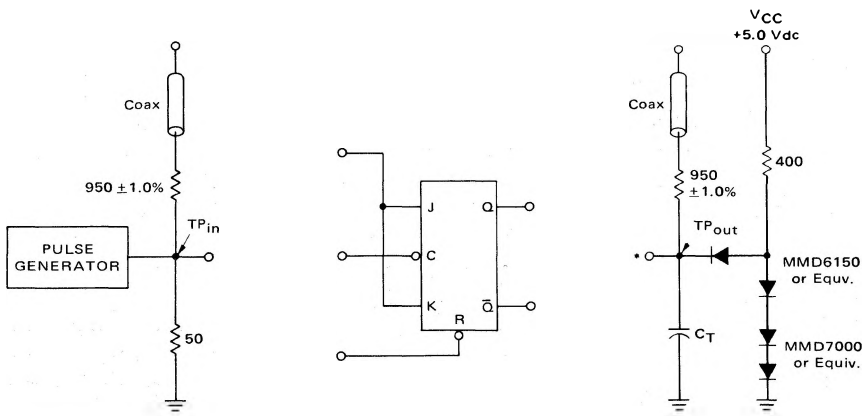
Data must be applied to the J-K inputs while the clock is low. When the clock input goes to the positive logic "1" state, the data at the J and K inputs is transferred to the master section, where it is stored until the clock changes to the positive logic "0" state. Data at the J and K inputs must not be changed while the clock is high. When the clock returns to the positive logic "0" state, information in the master section is transferred to the slave section.

Application of a logic "0" to the $\overline{\text{Reset}}$ input will force the $\overline{Q}$ output to the logic "1" state. The $\overline{\text{Reset}}$ input overrides the clock.

Since no charge storage is involved in this flip-flop, rise and fall times are not important to its operation. Clock fall times as long as 1.0 μs will not adversely affect the operation of the flip-flop. The clock pulse need only be wide enough to allow the data to settle in the master section. This time, which is the setup time for a logic "1", is 20 ns minimum.

Transistors Q_A have been added to the standard flip-flop circuit to protect the device against negative clock transients. This addition prevents both outputs from changing to the logic "1" state when transients in excess of -2.0 V appear at the clock.

SWITCHING TIME TEST CIRCUIT



t+ = 12 ns
t- = 6.0 ns } 10% to 90% Points
f = 15 MHz for waveform 1
1.0 MHz for waveforms 2 and 3

*A load is connected to each output during the test.

Two pulse generators are required and must be slaved together for t_{sd} tests.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

TEST PROCEDURES

(Numbers shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT			Q	$\overline{Q}$	LIMITS		
		$\overline{C}$	J, K	$\overline{R}$			Min	Max	Unit
Toggle Frequency	f_{Tog}	1	1	2.4 V	†	†	15	–	MHz
Turn-On Delay	t_{pd-}	2	2	2.4 V	4	4	10	40	ns
Turn-Off Delay	t_{pd+}	2	2	2.4 V	5	5	10	25	ns
Turn-On Delay	t_{sd-}	2	2	3	6	7	–	40	ns
Turn-Off Delay	t_{sd+}	2	2	3	6	7	–	25	ns
Enable Voltage	V_{EN}	2	2.0 V	2.4 V	†	†	†	–	–
Inhibit Voltage	V_{INH}	2	0.8 V	2.4 V	‡	‡	‡	–	–

†Output shall toggle with each input pulse.
‡Output shall NOT toggle.

VOLTAGE WAVEFORMS AND DEFINITIONS