# **Dual Timing Circuit**

The MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output can Source or Sink 200 mA
- Output can Drive MTTL

10

0.1 uF

t = 1.1: R and C = 22 sec

Time delay (t) is variable by changing R and C (see Figure 16).

0.01 u

- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1455 Timer

1/2

MC3456

1.0 k

7

1.0 μF

Figure 1. 22 Second Solid State Time Delay Relay Circuit

21FASE

R ≶ 20 M

С

1N4740



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# DUAL TIMING CIRCUIT SEMICONDUCTOR TECHNICAL DATA

P SUFFIX LASTIC PACKAGE CASE 646

D SUFFIX PLASTIC PACKAGE CASE 751A (SO-14)

## **PIN CONNECTIONS**

SEM

	$\neg$	1
Discharge A 1		14 V <sub>CC</sub>
Threshold A 2		13 Discharge B
Control A 3		12 Threshold B
Reset A 4		11 Control B
Output A 5		10 Reset B
Trigger A 6		9 Output B
Gnd 7		8 Trigger B
	(Top View)	

OR	DERING INFORMA	TION
	Operating	Deeke

Device	Temperature Range	Package
MC3456P	- 0° to +70°C	Plastic DIP
NE556D		SO-14

Load

1N4003

10 սե

Vac/60 Hz

MT2

G

-10 V

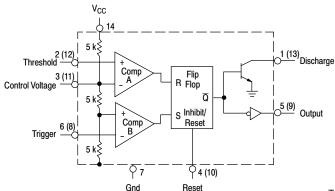
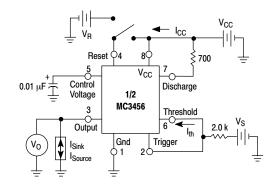


Figure 2. Block Diagram (1/2 Shown)



Test circuit for measuring DC parameters (to set output and measure parameters):

a) When  $V_S \ge 2/3 V_{CC}$ ,  $V_O$  is low. b) When  $V_S \ge 1/3 V_{CC}$ ,  $V_O$  is high. c) When  $V_O$  is low. Pin 7 sinks current. To test for Reset, set  $V_O$  high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to V<sub>CC</sub>.

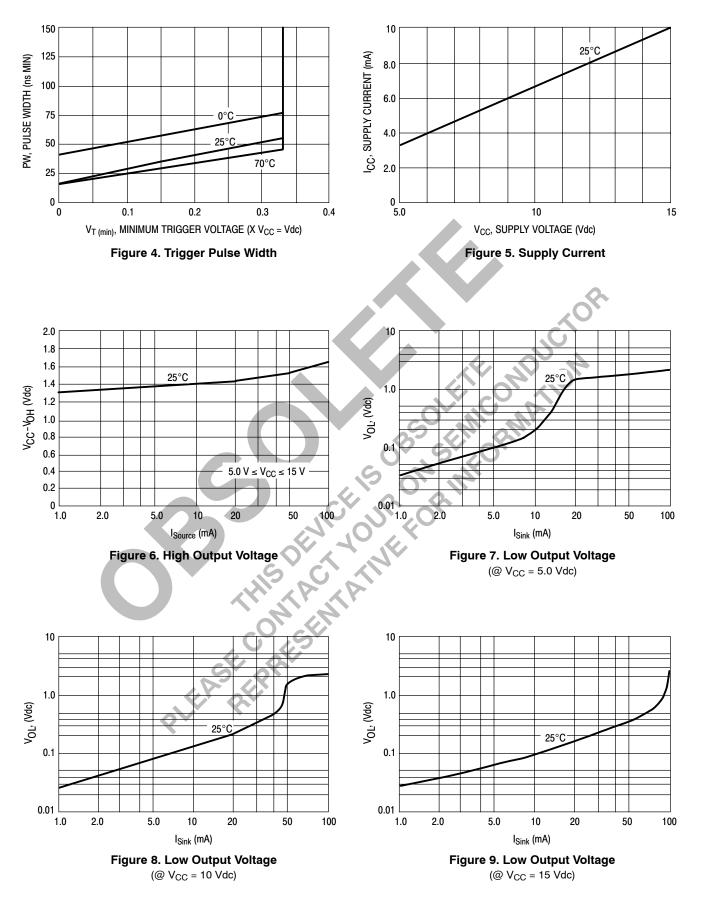
Figure 3. General Test Circuit

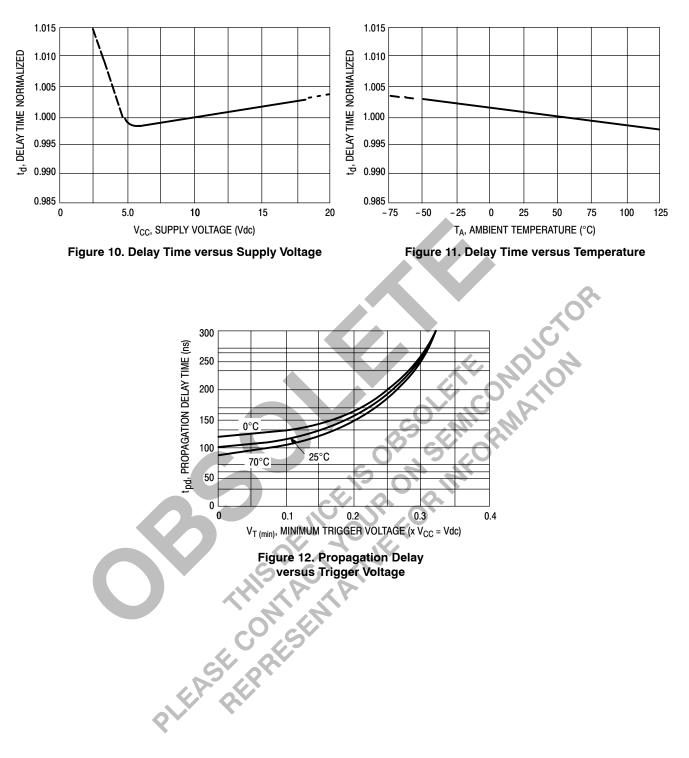
#### **MAXIMUM RATINGS** ( $T_A = +25^{\circ}C$ , unless otherwise noted.)

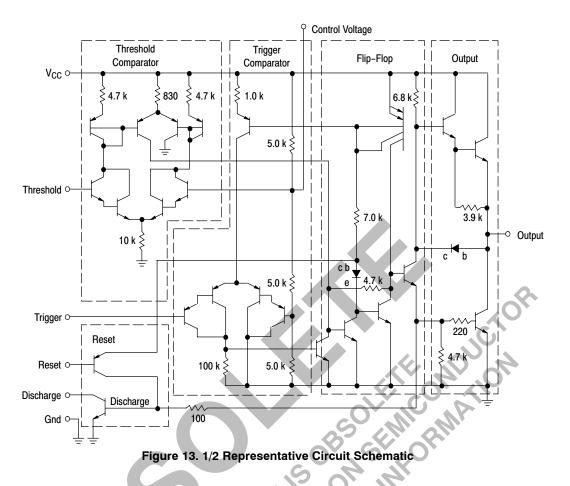
	Rating		Symbol	Value	Unit
Power Supply Voltage			V <sub>CC</sub>	+18	Vdc
Discharge Current			Idis	200	mA
Power Dissipation (Package Limitation) P Suffix, Plastic Package, Case 646 Derate above $T_A = +25^{\circ}C$ D Suffix, Plastic Package, Case 751 Derate above $T_A = +25^{\circ}C$		OBSE	Pp	625 5.0 1.0 8.0	mW mW/°C W mW/°C
Operating Ambient Temperature Range		2014	T <sub>A</sub>	0 to +70	°C
Storage Temperature Range		A A	T <sub>stg</sub>	-65 to +150	°C
O PLE	SE PRESENTA				

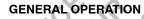
Characteristics	Symbol	Min	Тур	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	-	16	V
Supply Current $V_{CC} = 5.0 \text{ V}, \text{ R}_{L} = \infty$ $V_{CC} = 15 \text{ V}, \text{ R}_{L} = \infty$ [Low State, (Note 1)	Icc	-	6.0 20	12 30	mA
Timing Error (Note 2) Monostable Mode ( $R_A = 2.0 \text{ k}\Omega$ ; $C = 0.1 \mu\text{F}$ ) Initial Accuracy Drift with Temperature Drift with Supply Voltage Astable Mode ( $R_A = R_B = 2.0 \text{ k}\Omega$ to 100 k $\Omega$ ; $C = 0.01 \mu\text{F}$ ) Initial Accuracy Drift with Temperature Drift with Temperature		-	0.75 50 0.1 2.25 150		% PPM/°C %/V PPM/°C
Drift with Supply Voltage Threshold Voltage	N	-	0.3	_	%/V
Trigger Voltage $V_{CC} = 15 V$ $V_{CC} = 5.0 V$	V <sub>th</sub> V <sub>T</sub>		5.0 1.67	-	×V <sub>CC</sub> V
Trigger Current	Ι <sub>Τ</sub>	-	0.5		μΑ
Reset Voltage	V <sub>R</sub>	0.4	0.7	1.0	V
Reset Current	IR	-	0.1	- (	mA
Threshold Current (Note 3)	I <sub>th</sub>	-	0.03	0.1	μA
Control Voltage Level $\begin{array}{c} V_{CC} = 15 \ V \\ V_{CC} = 5.0 \ V \end{array}$	V <sub>CL</sub>	9.0 2.6	10 3.33	11 4.0	V
Output Voltage Low (V <sub>CC</sub> = 15 V) I <sub>Sink</sub> = 10 mA I <sub>Sink</sub> = 50 mA I <sub>Sink</sub> = 200 mA (V <sub>CC</sub> = 5.0 V) I <sub>Sink</sub> = 5.0 mA	VoL OB	OF MI	0.1 0.4 2.0 2.5 0.25	0.25 0.75 2.75 - 0.35	V
Output Voltage High (I <sub>Source</sub> = 200 mA) V <sub>CC</sub> = 15 V	Vон	Sr_	12.5	_	V
(I <sub>Source</sub> = 100 mA) V <sub>CC</sub> = 15 V V <sub>CC</sub> = 5.0 V		12.75 2.75	13.3 3.3		
Toggle Rate R <sub>A</sub> = 3.3 k $\Omega$ , R <sub>B</sub> = 6.8 k $\Omega$ , C = 0.003 $\mu$ F (Figure 17, 19)	-	-	100	-	kHz
Discharge Leakage Current	I <sub>dis</sub>	-	20	100	nA
Rise Time of Output	t <sub>OLH</sub>	-	100	-	ns
Fall Time of Output	t <sub>OHL</sub>	-	100	-	ns
Matching Characteristics Between Sections Monostable Mode Initial Timing Accuracy Timing Drift with Temperature Drift with Supply Voltage		- - -	1.0 ±10 0.2	2.0 - 0.5	% ppm/°C %/V

**NOTES:** 1. Supply current is typically 1.0 mA less for each output which is high. 2. Tested at  $V_{CC} = 5.0$  V and  $V_{CC} = 15$  V. 3. This will determine the maximum value of  $R_A + R_B$  for 15 V operation. The maximum total R = 20 m $\Omega$ .









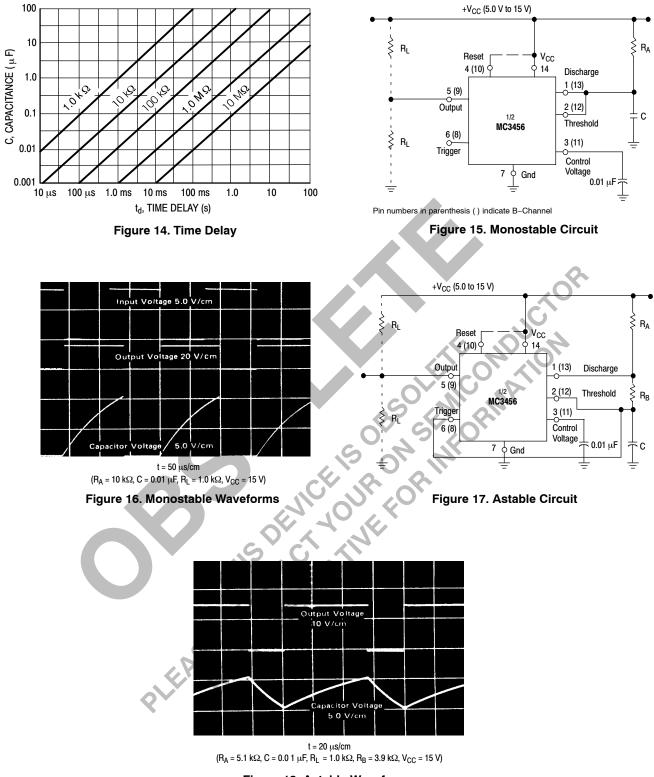
The MC3456 is a dual timing circuit which uses as its timing elements an external resistor/capacitor network. It can be used in both the monostable (one shot) and astable modes with frequency and duty cycle, controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip–flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

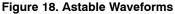
#### **Monostable Mode**

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode (refer to circuit Figure 15). When the input voltage to the trigger comparator falls below  $1/3 V_{CC}$  the

comparator output triggers the flip–flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V<sub>CC</sub> the threshold comparator resets the flip–flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip–flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation t = 1.1 R<sub>A</sub> C. Various combinations of R and C and their associated times are shown in Figure 14. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.





### Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between  $1/3 V_{CC}$  and  $2/3 V_{CC}$  (see Figure 17).

The external capacitor charges to  $2/3 V_{CC}$  through  $R_A$  and  $R_B$  and discharges to 1/3 V<sub>CC</sub> through  $R_B$ . By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by:  $t_1 = 0.695 (R_A + R_B) C$ 

The discharge time (output low) by: t<sub>2</sub> = 0.695 (R<sub>B</sub>) C

Thus the total period is given by:  

$$T = t_1 + t_2 = 0.695 (R_A + 2R_B) C$$

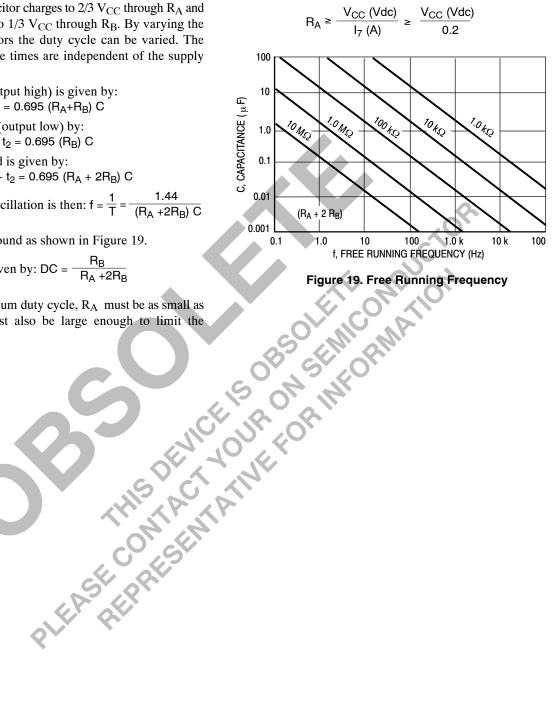
The frequency of oscillation is then:  $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$ 

and may be easily found as shown in Figure 19.

The duty cycle is given by: DC =  $\frac{R_B}{R_A + 2R_B}$ 

To obtain the maximum duty cycle, RA must be as small as possible; but it must also be large enough to limit the discharge current (Pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R<sub>A</sub> is given by:



# Figure 19. Free Running Frequency

#### **APPLICATIONS INFORMATION**

#### **Tone Burst Generator**

For a tone burst generator, the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

#### **Dual Astable Multivibrator**

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

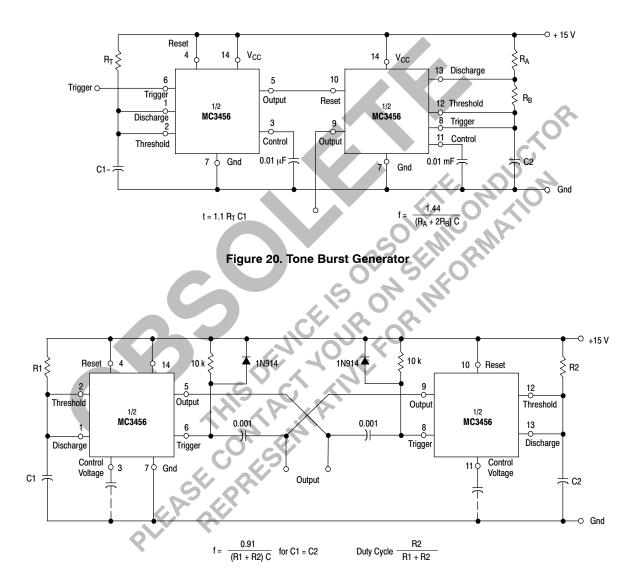


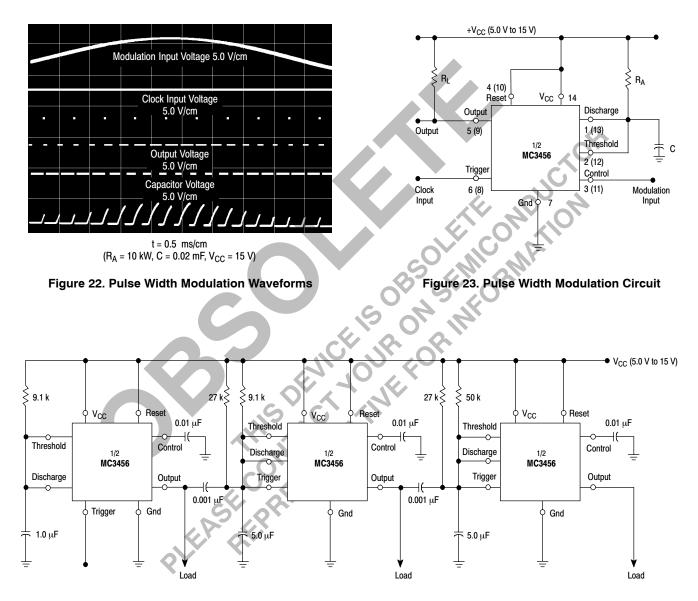
Figure 21. Dual Astable Multivibrator

#### **Pulse Width Modulation**

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

#### **Test Sequences**

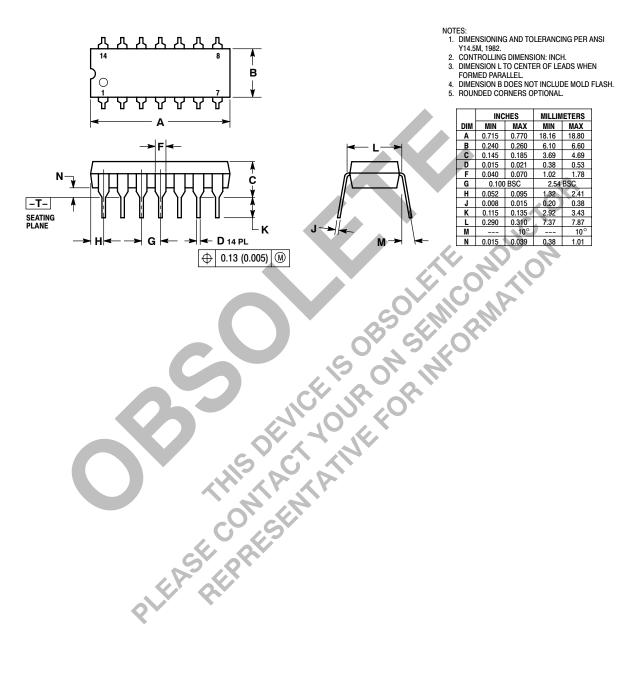
Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.





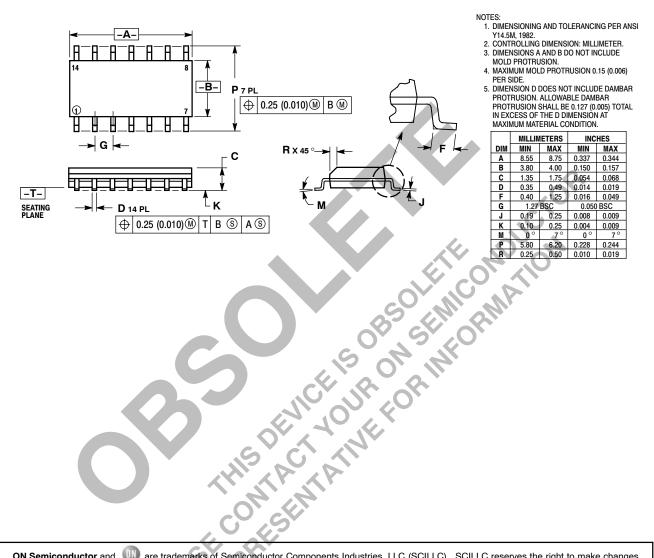
#### PACKAGE DIMENSIONS

P SUFFIX PLASTIC PACKAGE CASE 646–06 ISSUE M



#### PACKAGE DIMENSIONS

D SUFFIX PLASTIC PACKAGE CASE 751A-03 ISSUE F



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