

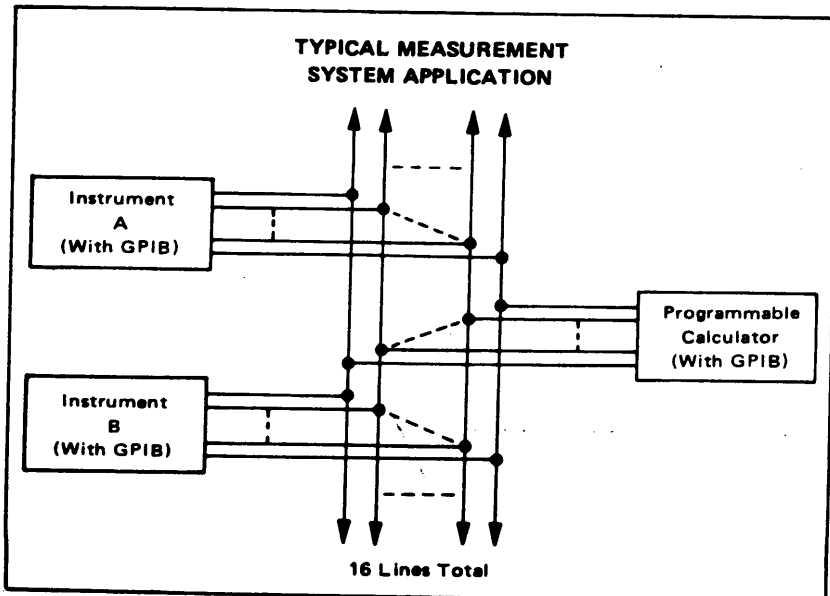
**BIDIRECTIONAL INSTRUMENTATION  
 BUS (GPIB) TRANSCEIVER**

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

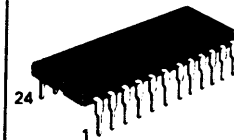
Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- **Low Power —**  
 Average Power Supply Current = 30 mA Listening  
 75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection  
 (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

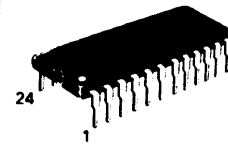


**MC3447**

**OCTAL BIDIRECTIONAL  
 BUS TRANSCEIVER  
 WITH  
 TERMINATION NETWORKS  
 SILICON MONOLITHIC  
 INTEGRATED CIRCUIT**

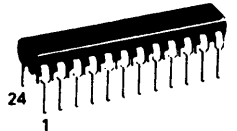


**L SUFFIX  
 CERAMIC PACKAGE  
 CASE 623**

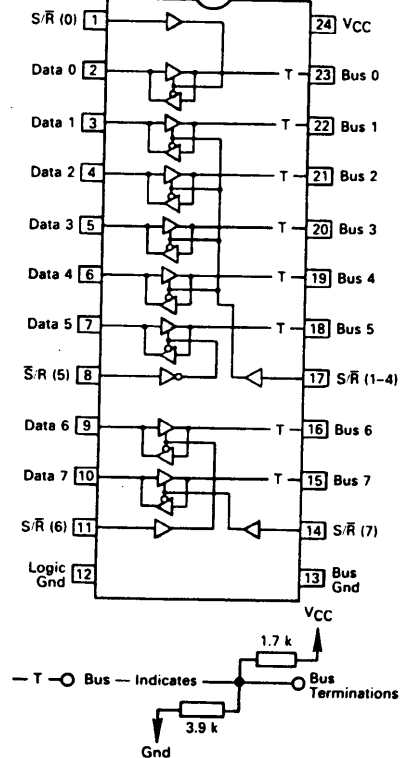


**P SUFFIX  
 PLASTIC PACKAGE  
 CASE 649**

**P3 SUFFIX  
 PLASTIC PACKAGE  
 CASE 724**



**PIN CONNECTIONS**



# MC3447

## MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	7.0	Vdc
Input Voltage	$V_I$	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Operating Ambient Temperature Range	$T_A$	0 to +70	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted  $4.50\text{ V} < V_{CC} < 5.50\text{ V}$  and  $0 < T_A < 70^\circ\text{C}$ ; typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ )

Characteristic — Note 1	Symbol	Min	Typ	Max	Unit	
Bus Voltage (Bus Pin Open) ( $V_{I(S/R)} = 0.8\text{ V}$ ) ( $I_{(Bus)} = -12\text{ mA}$ )	$V_{(Bus)}$ $V_{IC(Bus)}$	2.5 —	— —	3.7 -1.5	V mA	
Bus Current ( $5.0\text{ V} < V_{(Bus)} < 5.5\text{ V}$ ) ( $V_{(Bus)} = 0.5\text{ V}$ ) ( $V_{CC} = 0\text{ V}$ , $0\text{ V} < V_{(Bus)} < 2.75\text{ V}$ )	$I_{(Bus)}$	0.7 -1.3 —	— — —	2.5 -3.2 +0.04	mA	
Receiver Input Hysteresis ( $V_{I(S/R)} = 0.8\text{ V}$ )	—	400	600	—	mV	
Receiver Input Threshold ( $V_{I(S/R)} = 0.8\text{ V}$ )	Low to High High to Low	$V_{ILH(R)}$ $V_{IHL(R)}$	— 0.8	1.6 1.0	2.0 —	V
Receiver Output Voltage — High Logic State ( $V_{I(S/R)} = 0.8\text{ V}$ , $I_{OH(R)} = -200\text{ }\mu\text{A}$ , $V_{(Bus)} = 2.0\text{ V}$ )	$V_{OH(R)}$	2.4	—	—	V	
Receiver Output Voltage — Low Logic State ( $V_{I(S/R)} = 0.8\text{ V}$ , $I_{OL(R)} = 4.0\text{ mA}$ , $V_{(Bus)} = 0.8\text{ V}$ )	$V_{OL(R)}$	—	—	0.5	V	
Receiver Output Short Circuit Current ( $V_{I(S/R)} = 0.8\text{ V}$ , $V_{(Bus)} = 2.0\text{ V}$ )	$I_{OS(R)}$	-4.0	—	-20	mA	
Driver Input Voltage — High Logic State ( $V_{I(S/R)} = 2.0\text{ V}$ )	$V_{IH(D)}$	2.0	—	—	V	
Driver Input Voltage — Low Logic State ( $V_{I(S/R)} = 2.0\text{ V}$ )	$V_{IL(D)}$	—	—	0.8	V	
Driver Input Current — Data Pins ( $V_{I(S/R)} = 2.0\text{ V}$ ) ( $0.5 < V_{I(D)} < 2.7\text{ V}$ ) ( $V_{I(D)} = 5.5\text{ V}$ )	$I_{I(D)}$ $I_{IB(D)}$	-100 —	— —	40 200	$\mu\text{A}$	
Input Current — Send/Receive ( $0.5 < V_{I(S/R)} < 2.7\text{ V}$ ) ( $V_{I(S/R)} = 5.5\text{ V}$ )	$I_{I(S/R)}$ $I_{IB(S/R)}$	-250 —	— —	20 100	$\mu\text{A}$	
Driver Input Clamp Voltage ( $V_{I(S/R)} = 2.0\text{ V}$ , $I_{IC(D)} = -18\text{ mA}$ )	$V_{IC(D)}$	—	—	-1.5	V	
Driver Output Voltage — High Logic State ( $V_{I(S/R)} = 2.0\text{ V}$ , $V_{IH(D)} = 2.0\text{ V}$ )	$V_{OH(D)}$	2.5	—	—	V	
Driver Output Voltage — Low Logic State (Note 2) ( $V_{I(S/R)} = 2.0\text{ V}$ , $V_{IL(D)} = 0.8\text{ V}$ , $I_{OL(D)} = 48\text{ mA}$ )	$V_{OL(D)}$	—	—	0.5	V	
Power Supply Current (Listening Mode — All Receivers On) (Talking Mode — All Drivers On)	$I_{CCL}$ $I_{CCH}$	— —	30 75	45 95	mA	

## SWITCHING CHARACTERISTICS ( $V_{CC} = 5.0\text{ V}$ , $T_A = 25^\circ\text{C}$ unless otherwise noted)

Propagation Delay of Driver (Output Low to High)	$t_{PLH(D)}$	—	7.0	15	ns
(Output High to Low)	$t_{PHL(D)}$	—	16	30	
Propagation Delay of Receiver (Channels 0 to 5, 7)	$t_{PLH(R)}$	—	28	50	ns
(Output Low to High)	$t_{PHL(R)}$	—	15	30	
Propagation Delay of Receiver (Channel 6, Note 3)	$t_{PLH(R)}$	—	17	30	ns
(Output Low to High)	$t_{PHL(R)}$	—	12	22	
(Output High to Low)					

- NOTES: 1. Specified test conditions for  $V_{I(S/R)}$  are 0.8 V (Low) and 2.0 V (High). Where  $V_{I(S/R)}$  is specified as a test condition,  $V_{I(S/R)}$  uses the opposite logic levels.  
 2. The IEEE 488-1979 Bus Standard changes  $V_{OL(D)}$  from 0.4 to 0.5 V maximum to permit the use of Schottky technology.  
 3. In order to meet the IEEE 488-1978 Standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (Pins 9 and 16).

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## SWITCHING CHARACTERISTICS (continued) ( $V_{CC} = 5.0\text{ V}$ , $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Send/Receiver to Data					
Logic High to Third State	$t_{PHZ}(R)$	–	15	30	ns
Third State to Logic High	$t_{PZH}(R)$	–	15	30	ns
Logic Low to Third State	$t_{PLZ}(R)$	–	15	25	ns
Third State to Logic Low	$t_{PZL}(R)$	–	10	25	ns
Propagation Delay Time – Send/Receiver to Bus					
Logic Low to Third State	$t_{PLZ}(D)$	–	13	25	ns
Third State to Logic Low	$t_{PZL}(D)$	–	30	50	ns

### PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)

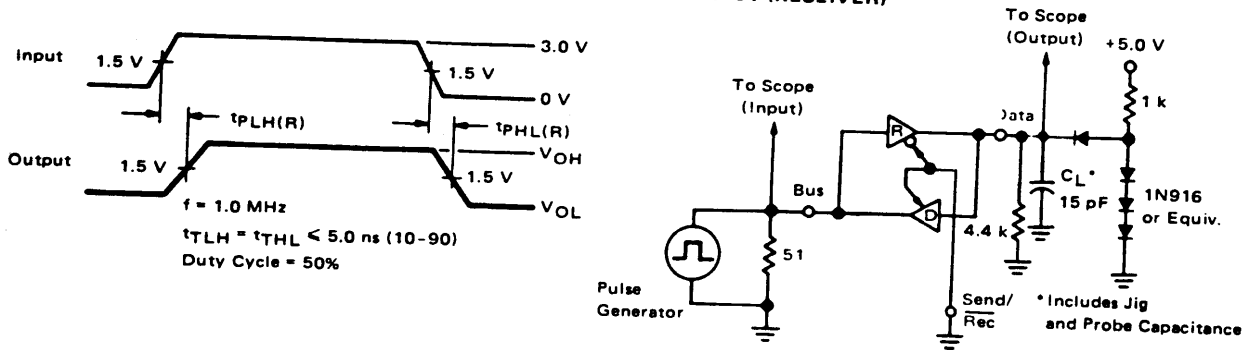


FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)

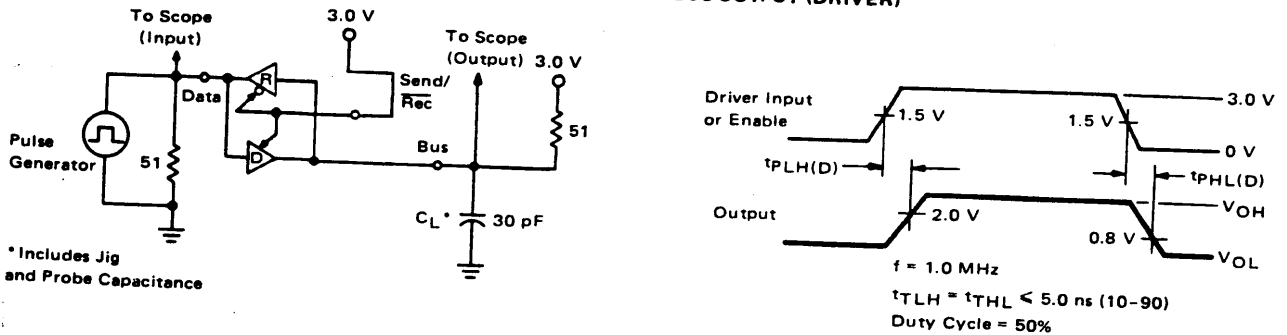
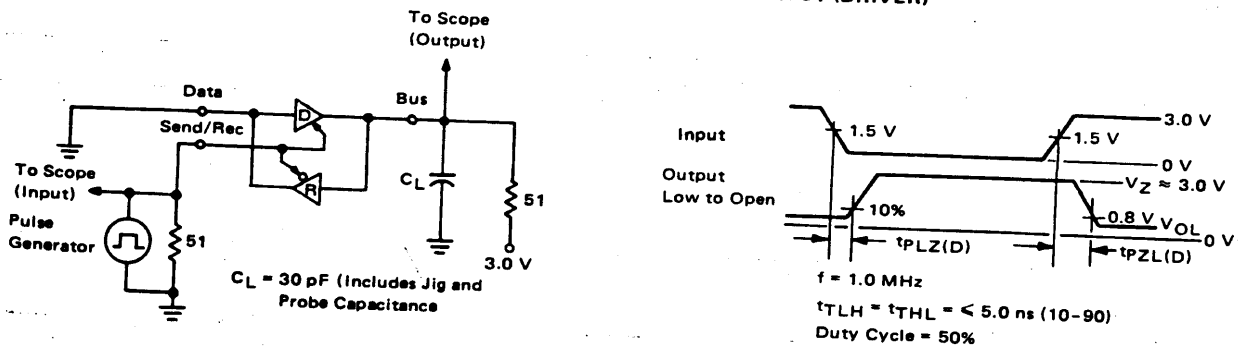


FIGURE 3 – SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)



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FIGURE 4 - SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

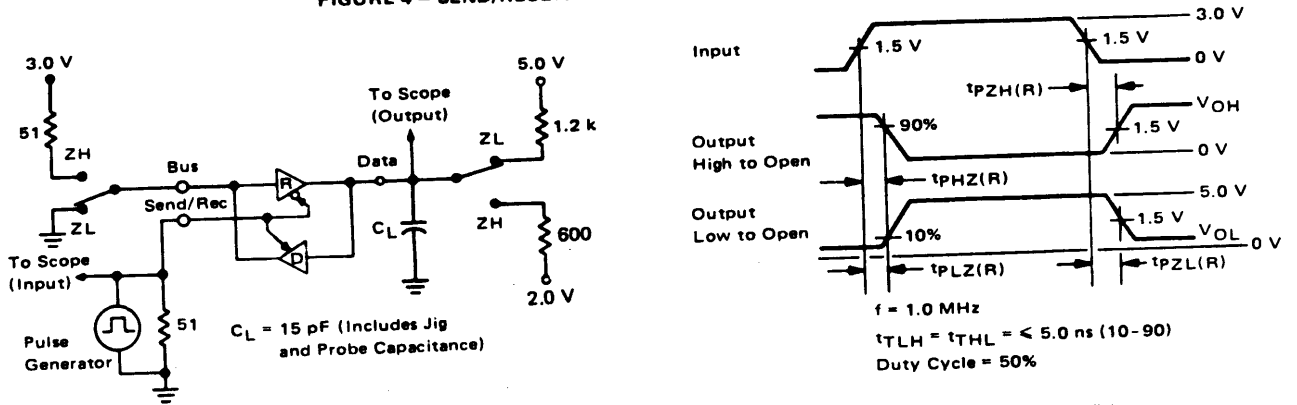


FIGURE 5 - TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

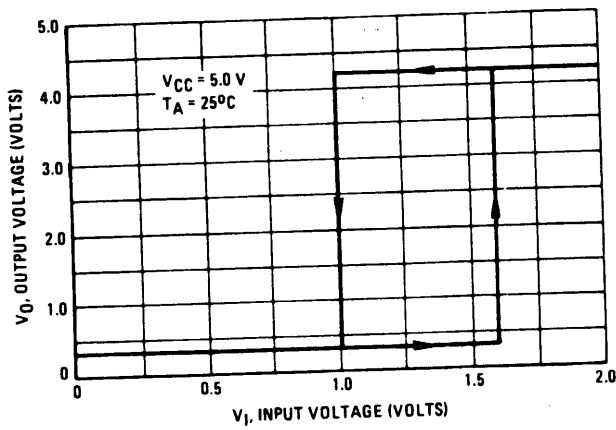


FIGURE 6 - TYPICAL BUS LOAD LINE

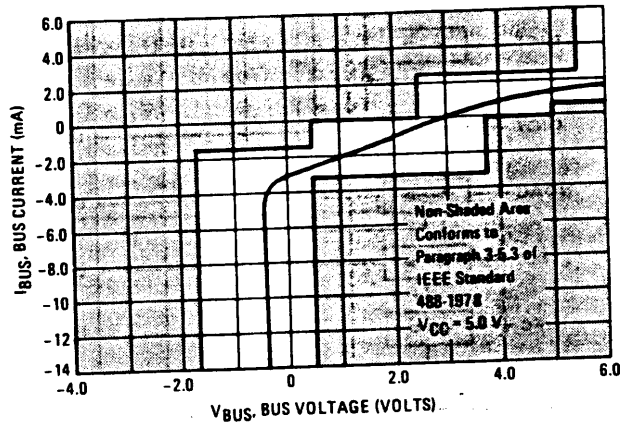
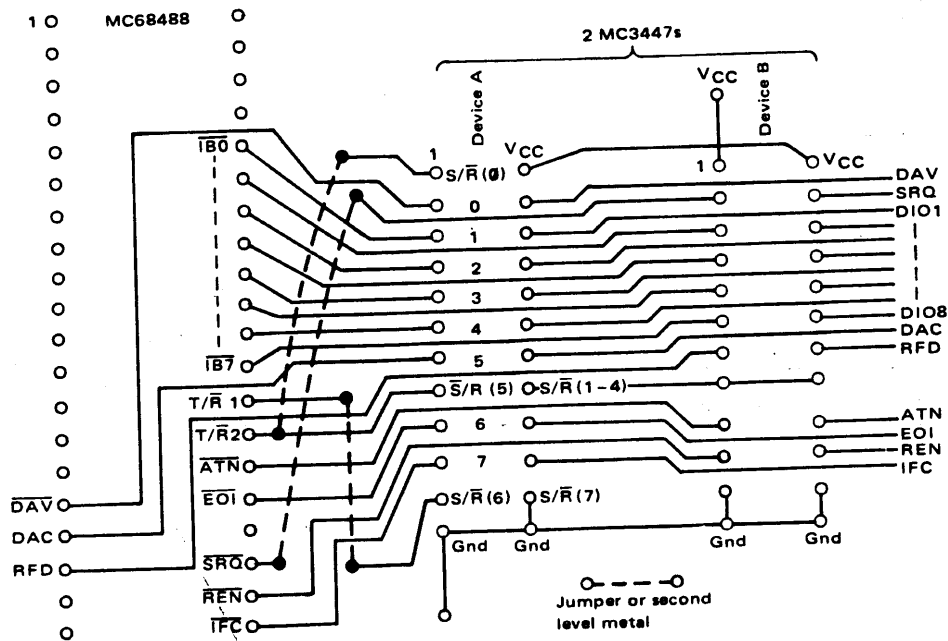
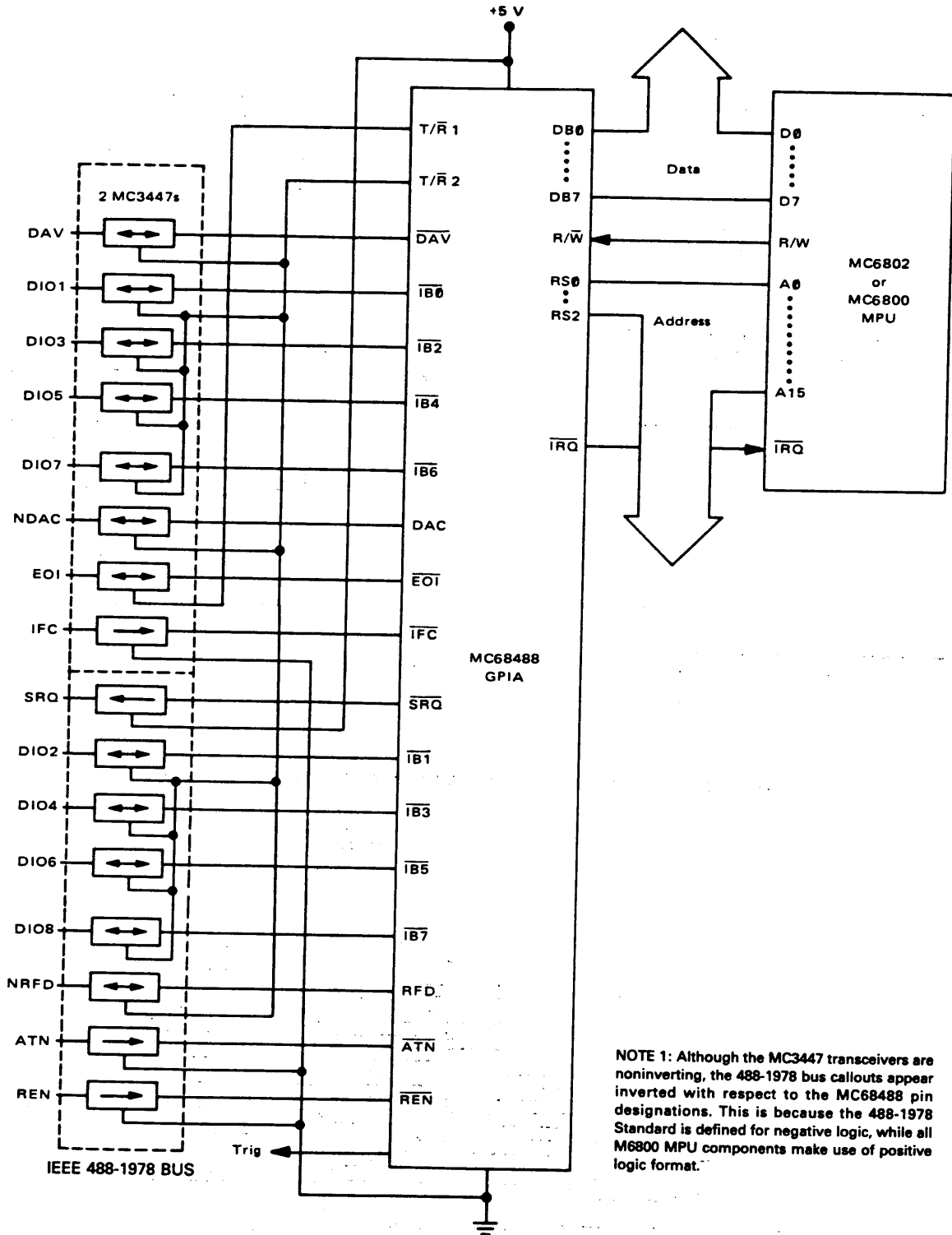


FIGURE 7 - SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488



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FIGURE 8 - SIMPLE SYSTEM CONFIGURATION

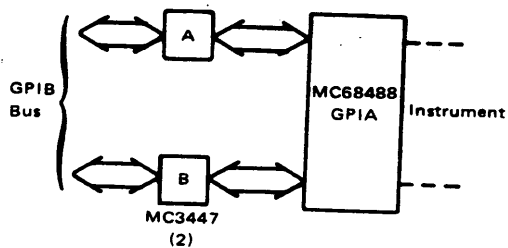


NOTE 1: Although the MC3447 transceivers are noninverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

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FIGURE 9 - SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

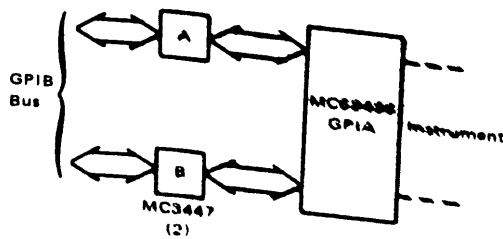
MC68488 Connections		MC3447 Pin Designations						MC68488 Connections	
A	B							A	B
T/R 2	VCC	S/R (0)	1	24	VCC			VCC	VCC
DAV	SRQ	Data 0 0	2	23	Bus 0			DAV	SRQ
IB0	IB1	Data 1	3	22	Bus 1			DIO 1	DIO 2
IB2	IB3	Data 2	4	21	Bus 2			DIO 3	DIO 4
IB4	IB5	Data 3	5	20	Bus 3			DIO 5	DIO 6
IB6	IB7	Data 4	6	19	Bus 4	Octal GPIB		DIO 7	DIO 8
DAC	RFD	Data 5	7	18	Bus 5	Transceiver		NDAC	NRFD
T/R 2	T/R 2	S/R (5)	8	17	S/R (1-4)			T/R 2	T/R 2
EOI	ATN	Data 6	9	16	Bus 6			EOI	ATN
IFC	REN	Data 7	10	15	Bus 7			IFC	REN
T/R 1	Gnd	S/R (6)	11	14	S/R (7)			Gnd	Gnd
Gnd	Gnd	Logic Gnd	12	13	Bus Gnd			Gnd	Gnd



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FIGURE 9 - SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations				MC68488 Connections	
A	B				A	B	
T/R 2	VCC	S/R (0)	1	24	VCC	VCC	
DAV	SRQ	Data 0	2	23	Bus 0	DAV	
IB0	IB1	Data 1	3	22	Bus 1	DIO 1	
IB2	IB3	Data 2	4	21	Bus 2	DIO 3	
IB4	IB5	Data 3	5	20	Bus 3	DIO 5	
IB6	IB7	Data 4	6	19	Bus 4	DIO 7	
DAC	RFD	Data 5	7	18	Bus 5	DIO 8	
T/R 2	T/R 2	S/R (5)	8	17	S/R (1-4)	NDAC	
E01	ATN	Data 6	9	16	Bus 6	T/R 2	
IFC	REN	Data 7	10	15	Bus 7	E01	
T/R 1	Gnd	S/R (6)	11	14	S/R (7)	IFC	
Gnd	Gnd	Logic Gnd	12	13	Bus Gnd	Gnd	



# MC3447

FIGURE 9 - SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations				MC68488 Connections	
A	B					A	B
T/R 2	VCC	S/R (0)	1	24	VCC	VCC	VCC
DAV	SRQ	Data 0 0	2	23	Bus 0	DAV	SRQ
IB0	IB1	Data 1	3	22	Bus 1	DIO 1	DIO 2
IB2	IB3	Data 2	4	21	Bus 2	DIO 3	DIO 4
IB4	IB5	Data 3	5	20	Bus 3	DIO 5	DIO 6
IB6	IB7	Data 4	6	19	Bus 4	DIO 7	DIO 8
DAC	RFD	Data 5	7	18	Bus 5	NDAC	NRFD
T/R 2	T/R 2	S/R (5)	8	17	S/R (1-4)	T/R 2	T/R 2
EOI	ATN	Data 6	9	16	Bus 6	EOI	ATN
IFC	REN	Data 7	10	15	Bus 7	IFC	REN
T/R 1	Gnd	S/R (6)	11	14	S/R (7)	Gnd	Gnd
Gnd	Gnd	Logic Gnd	12	13	Bus Gnd	Gnd	Gnd

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