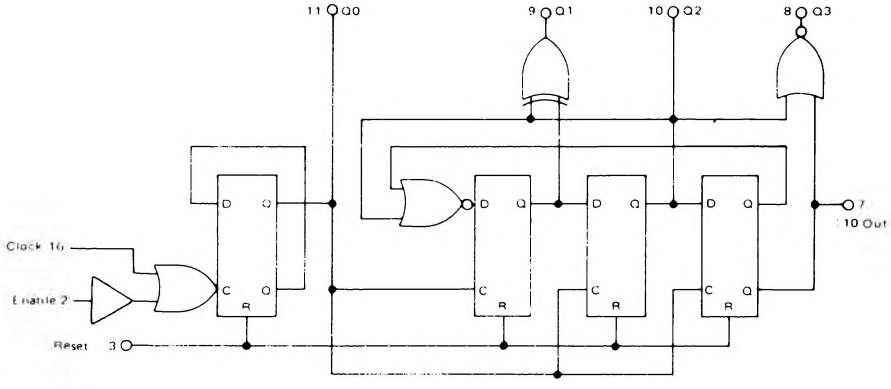
1-GHz Divide-by-ten Counter

The MC1696 is a gigahertz bi-quinary decade counter. Its features include clock enable, BCD decoded outputs, and reset. The clock input is internally referenced to −4.2 volts, and requires an a c coupled sinewave input of 800 millivolts peak to peak (typical). The enable input can be driven with a MECL III gate and is ORed with clock input. The reset operates only when either the clock or the enable is high.

A divide-by-ten output (60%/o/40%/o high/-low duty cycle) connects to following MECL III or MECL 10,000 circuits for longer counter chains. Additional outputs decoded to standard BCD are available for decoding or display driving. These BCD outputs will not follow the MC1696 operating at top speed, but would normally be read after the counter is stopped.



f_{tog} = 1.2 GHz typ
P_D = 650 mW typ/pkg (No Load)
Output Rise and Fall Times = 1.0 ns (20%/o to 80%/o)

V_{CC1} = Pin 4
V_{CC2} = Pin 5
V_{EE1} = Pin 13
V_{EE2} = Pin 12
Bias Point = Pin 1