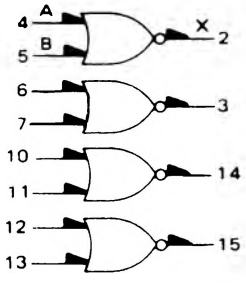

$X = \overline{A + B}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = −25 mAdc max

Quad 2-input NOR Gate

Four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (−30 to +85°C).
Input pulldown resistors eliminate the need to the unused inputs to V_{EE}.