

MC1545 MC1445

HIGH-FREQUENCY CIRCUITS

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

... designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN475 and AN491 for design details.

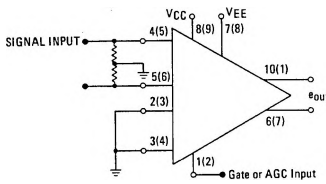
- Large Bandwidth; 75 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

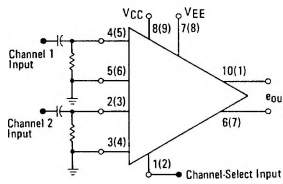
MONOLITHIC SILICON
EPITAXIAL PASSIVATED

TYPICAL APPLICATIONS

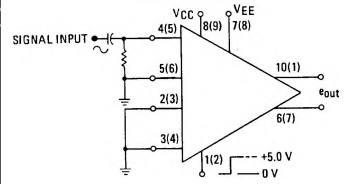
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



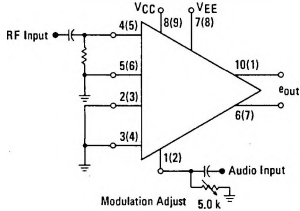
MULTIPLEX OR FSK



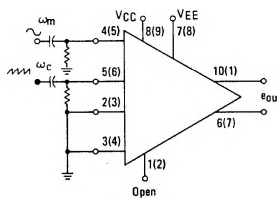
ANALOG SWITCH



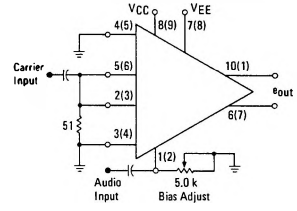
AMPLITUDE MODULATOR



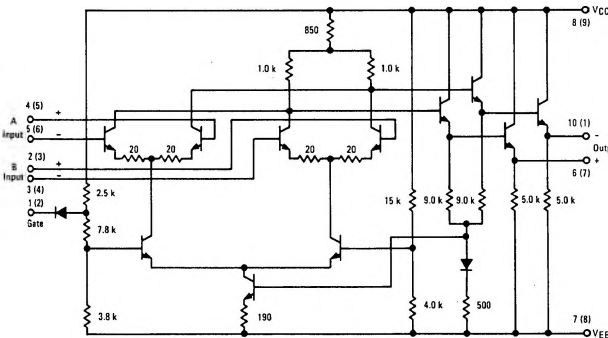
PULSE-WIDTH MODULATOR



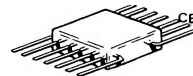
BALANCED MODULATOR



CIRCUIT SCHEMATIC

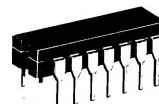


Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.



F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

G SUFFIX
METAL PACKAGE
CASE 602A



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MC1545, MC1445 (continued)

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+12	Vdc
	V_{EE}	-12	Vdc
Differential Input Signal	V_{ID}	± 5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	Flat Package Derate above $T_A = +25^\circ\text{C}$	500	mW
		3.3	mW/ $^\circ\text{C}$
	Ceramic Dual In-Line Package Derate above $T_A = +25^\circ\text{C}$	625	mW
		5.0	mW/ $^\circ\text{C}$
	Metal Can Derate above $T_A = +25^\circ\text{C}$	680	mW
	4.6	mW/ $^\circ\text{C}$	
Operating Temperature Range	MC1445	T_A	0 to +75
	MC1545		-55 to +125
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0$ Vdc, $V_{EE} = 5.0$ Vdc, at $T_A = +25^\circ\text{C}$, specifications apply to both input channels unless otherwise noted)

Characteristic	Fig. No.	Symbol*	Min	Typ	Max	Unit	
Single-Ended Voltage Gain	MC1445 MC1545	1, 12	A_{vs}	16 16	19 18	22 20	dB
Bandwidth	MC1445 MC1545	1, 12	BW	— 50	75 75	—	MHz
Input Impedance ($f = 50$ kHz)	MC1445 MC1545	5, 14	z_{is}	3.0 4.0	10 10	—	k ohms
Output Impedance ($f = 50$ kHz)		6, 15	z_{os}	—	25	—	Ohms
Output Voltage Swing ($R_L = 1.0$ k ohm, $f = 50$ kHz)		4, 13	V_{OD}	1.5	2.5	—	V_{p-p}
Input Bias Current ($I_{IB} = (I_1 + I_2)/2$)	MC1445 MC1545	16	I_{IB}	— —	15 15	30 25	μA
Input Offset Current		16	$ I_{IO} $	—	2.0	—	μA
Input Offset Voltage	MC1445 MC1545	17	$ V_{IO} $	— —	— 1.0	7.5 5.0	mVdc
Quiescent Output dc Level		17	V_O	—	0.2	—	Vdc
Output dc Level Change (Gate Voltage Change: +5.0 V to 0 V)		17	$ \Delta V_O $	—	15	—	mV
Common-Mode Rejection Ratio ($f = 50$ kHz)		9, 18	CMRR	—	85	—	dB
Input Common-Mode Voltage Swing		18	V_{ICR}	—	± 2.5	—	V_p
Gate Characteristics		8	V_{GOL}	—	—	—	Vdc
Gate Voltage Low (See Note 1)	MC1445 MC1545			0.20 0.45	0.40 0.70	—	
Gate Voltage High (See Note 2)	MC1445 MC1545			— —	1.3 1.5	3.0 2.2	
Gate Current Low (Gate Voltage = 0 V)	MC1445 MC1545	18	I_{GOL}	— —	— —	4.0 2.5	mA
Gate Current High (Gate Voltage = +5.0 V)	MC1445 MC1545	18	I_{GOH}	— —	— —	4.0 2.0	μA
Step Response ($e_{in} = 20$ mV)	MC1445	19	t_{PLH}	—	6.5	—	ns
	MC1545			—	6.5	10	
	MC1445		t_{PHL}	—	6.3	—	
	MC1545			—	6.3	10	
	MC1445		t_r	—	6.5	—	
	MC1545			—	6.5	10	
MC1445	t_f	—	7.0	—			
MC1545		—	7.0	10			
Wideband Input Noise (5.0 Hz – 10 MHz, $R_S = 50$ ohms)		10, 20	$V_{N(in)}$	—	25	—	$\mu\text{V(rms)}$
DC Power Dissipation	MC1445	11, 20	P_D	—	70	150	mW
	MC1545			—	70	110	

Note 1 V_{GOL} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.

Note 2 V_{GOH} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

*Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

MC1545, MC1445 (continued)

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

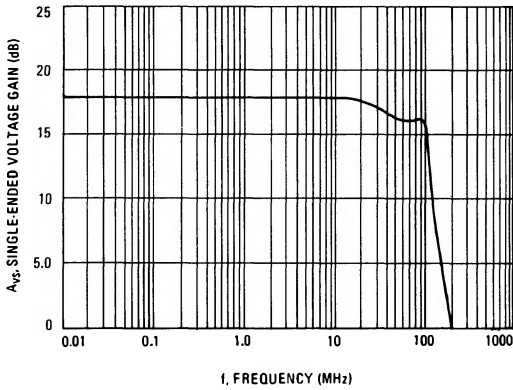


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

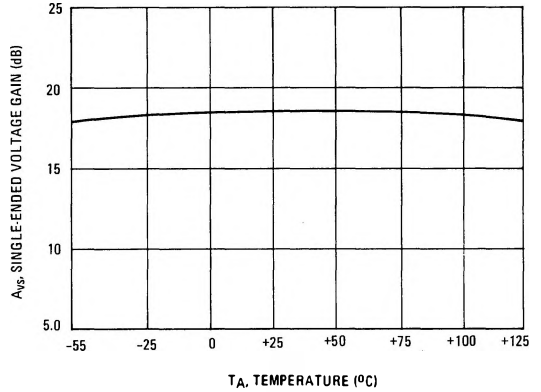


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

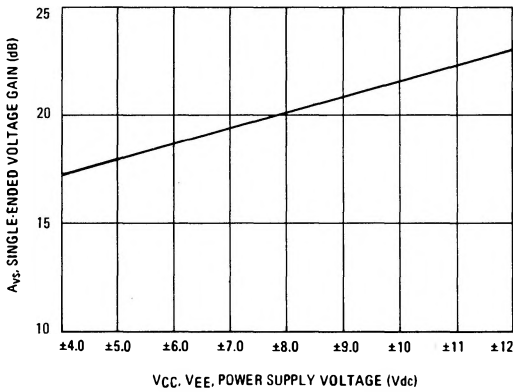


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

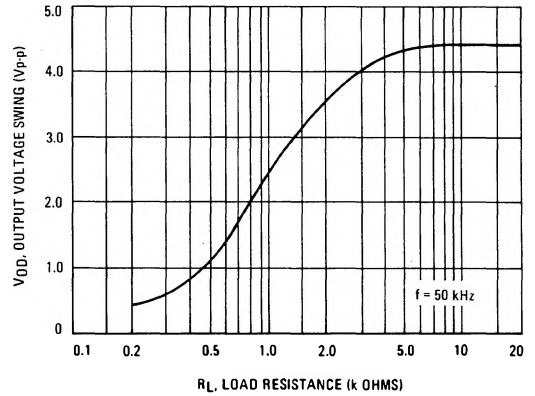


FIGURE 5 – INPUT C_p AND R_p versus FREQUENCY (BOTH CHANNELS)

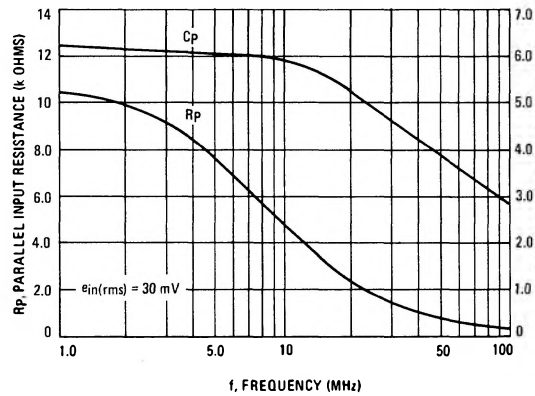
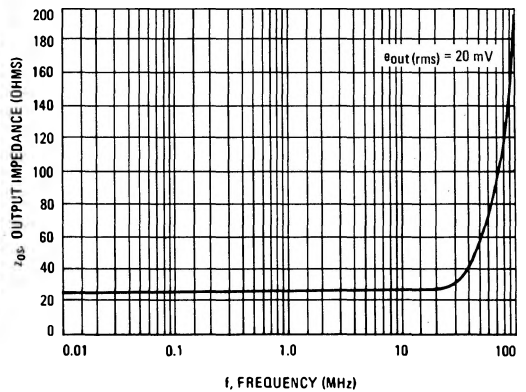


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY



MC1545, MC1445 (continued)

FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

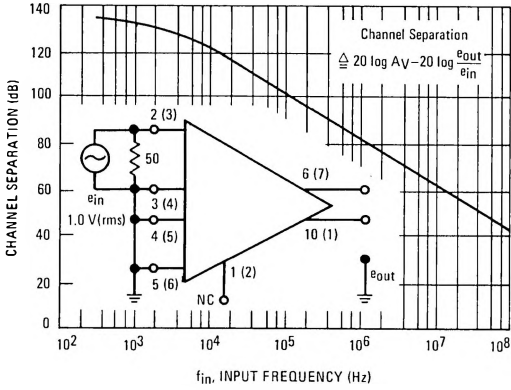


FIGURE 8 – GATE CHARACTERISTICS

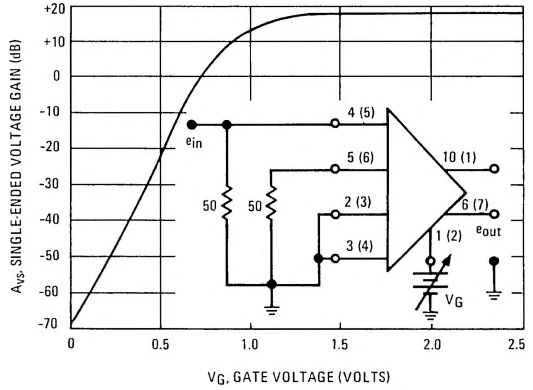


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

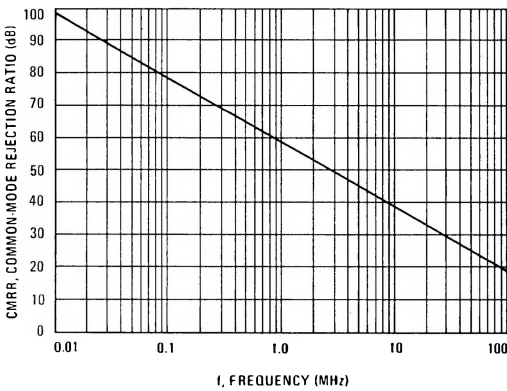


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

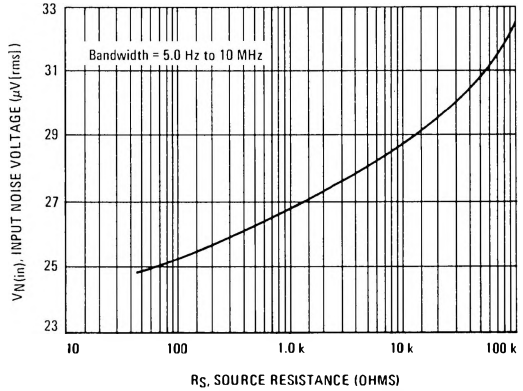


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

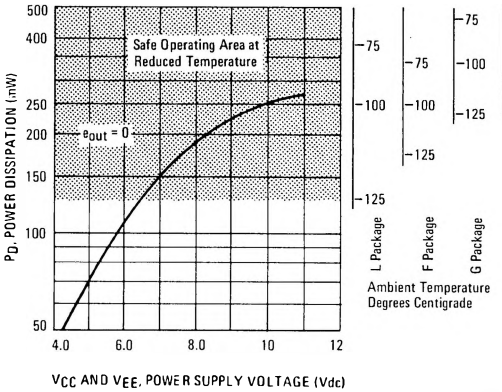
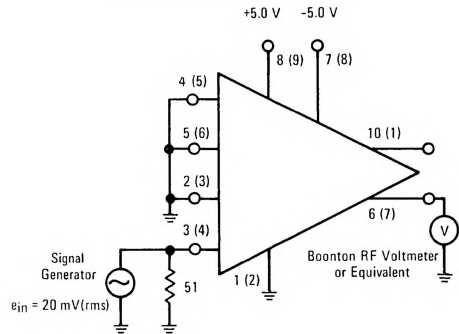


FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

MC1545, MC1445 (continued)

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

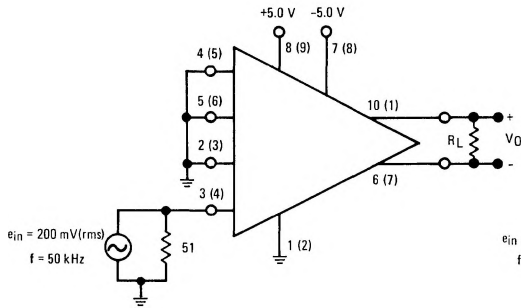


FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

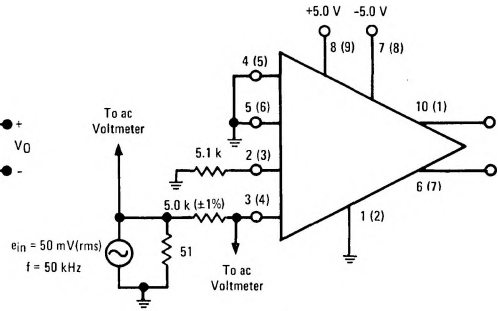


FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

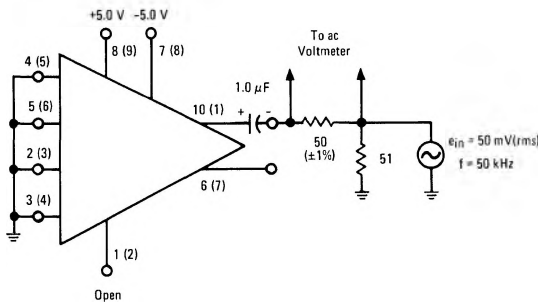


FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

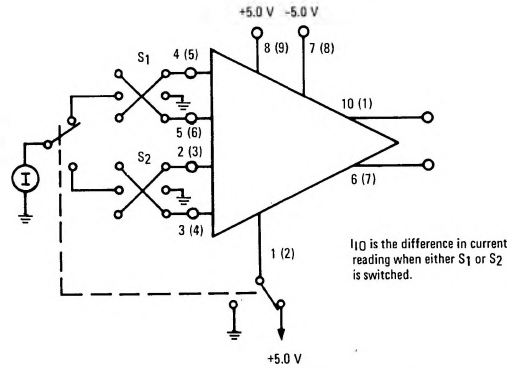


FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

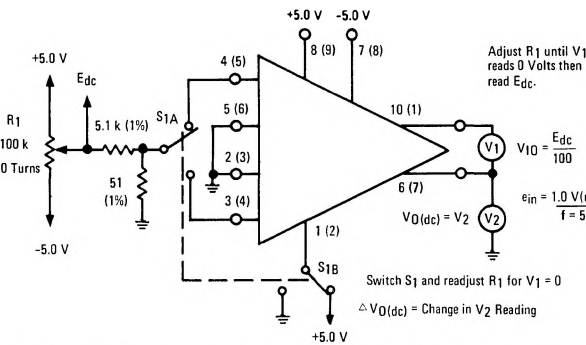
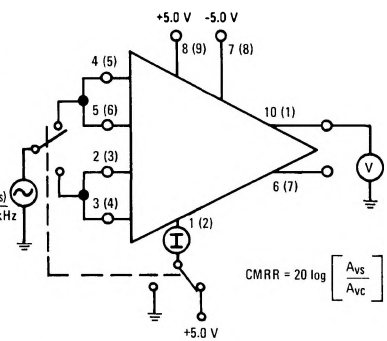


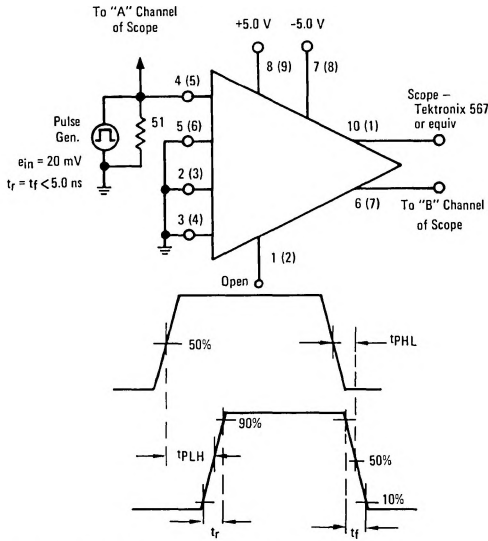
FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages, number at left in each case denotes corresponding pin for G package.

MC1545, MC1445 (continued)

FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



Number in parenthesis denotes pin for F and L packages,
number at left in each case denotes corresponding pin for G package.

FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

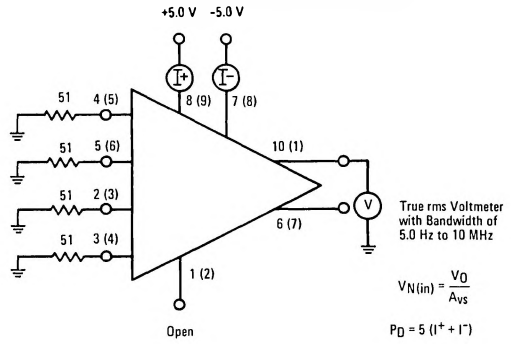


FIGURE 21 – LIMITING CHARACTERISTIC

