MC1328

DUAL CHROMA DEMODULATOR

MONOLITHIC DUAL DOUBLY BALANCED CHROMA DEMODULATOR

- Good Chroma Sensitivity (0.3 Vp-p Input Produces 5.0 Vp-p Output)
- Good dc Temperature Stability (3 mV/°C typ)
- Low Output dc Offset Voltages (0.6 V max)
- Pin Compatible with ULN-2114, ULN-2114A
- Negligible Change in Output Voltage Swing With Varying 3.58 MHz Reference Signal
- High Ripple Rejection Due To Built-In MOS Filter Capacitors
- High Output Voltage Swing (10 Vp-p Typ) – B-Y

DUAL DOUBLY BALANCED CHROMA DEMODULATOR

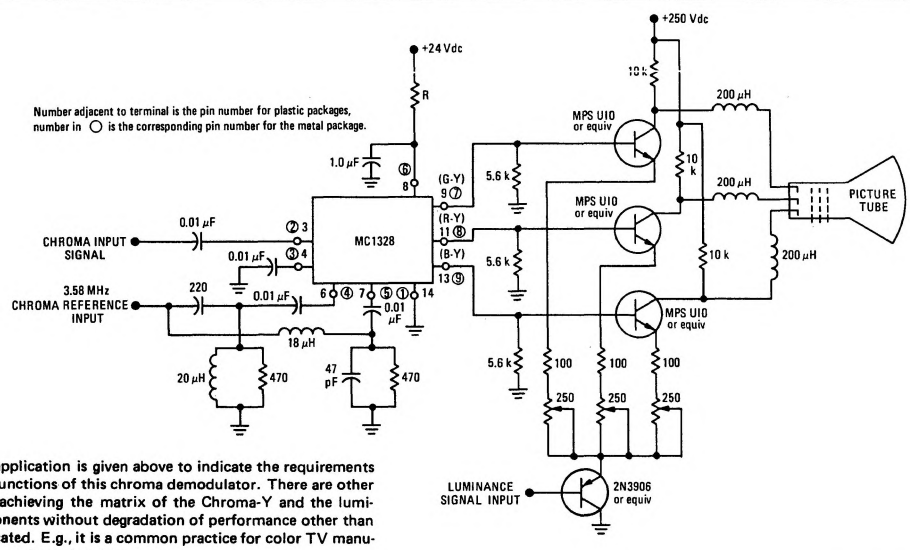
Monolithic Silicon Integrated Circuit

G SUFFIX
METAL PACKAGE
CASE 603-02
(TO-100)

P SUFFIX
PLASTIC PACKAGE
CASE 605
(TO-116)

PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – MC1328 TYPICAL APPLICATION



A practical application is given above to indicate the requirements and output functions of this chroma demodulator. There are other methods of achieving the matrix of the Chroma-Y and the luminance components without degradation of performance other than the one indicated. E.g., it is a common practice for color TV manufacturers to matrix in the picture tube.

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

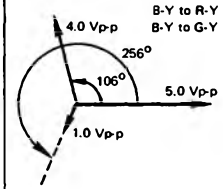
Rating	Value	Unit
Power Supply Voltage	30	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C Metal Package Derate above T_A = +25°C	 625 5.0 680 4.5	 mW mW/°C mW mW/°C
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms, Reference Input
STATIC CHARACTERISTICS Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Characteristic	Pin No. Suffix G Pkg	Pin No. Suffix P, PQ Pkgs	Min	Typ	Max	Unit
Quiescent Output Voltage See Figure 2	7,8,9	9,11,13	13	14.3	16	Vdc
Quiescent Input Current (See Figure 2) (R_L = ∞, Chroma and Reference Input Voltages = 0) (R_L = 3.3 k ohms, Chroma and Reference Input Voltages = 0)	6	8	– 16.5	6.0 19	– 25.5	mA
Reference Input DC Voltage	4,5	6,7	–	6.2	–	Vdc
Chroma Input DC Voltage	2,3	3,4	–	3.4	–	Vdc
Differential Output Voltage See Note 1 and Figure 3	7,8,9	9,11,13	–	0.3	0.6	Vdc
Output Temperature Coefficient (No Output Differential Voltage > 0.6 Vdc, +25°C to +65°C) See Note 1 and Figure 3	7,8,9	9,11,13	–	3.0	–	mV/°C

DYNAMIC CHARACTERISTICS (V^+ = 24 Vdc, R_L = 3.3 k ohms,
Referenced Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Detected Output Voltage (B-Y) See Note 2	9	13	8.0	9.0	–	Vp-p
Chroma Input Voltage (B-Y Output = 5.0 Vp-p) See Note 3	2	3	–	0.3	0.7	Vp-p
Detected Output Voltage (Adjust B-Y Output to 5.0 Vp-p) See Note 4 G-Y R-Y	 7 8	 9 11	 0.75 3.5	 1.0 3.8	 1.25 4.2	Vp-p
Relative Output Phase (B-Y Output = 5.0 Vp-p) B-Y to R-Y 4.0 Vp-p B-Y to G-Y  	 9-8 9-7	 13-11 13-9	 101 248	 106 256	 111 264	Degrees
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	7,8,9	9,11,13	–	250	500	mVp-p
B-Y Phase Shift (B-Y Reference Input to B-Y Output)	5-9	7-13	–	3	–	Degrees
Residual Carrier and Harmonics (with Input Signal Voltage, normal Reference Signal Voltage and B-Y = 5.0 Vp-p)	7,8,9	9,11,13	–	–	1.5	Vp-p
Reference Input Resistance (Chroma Input = 0)	4,5	6,7	–	2.0	–	k ohms
Reference Input Capacitance (Chroma Input = 0)	4,5	6,7	–	6.0	–	pF
Chroma Input Resistance	2,3	3,4	–	2.0	–	k ohms
Chroma Input Capacitance	2,3	3,4	–	2.0	–	pF

NOTES:

1. With Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage (1.0 Vp-p), all output voltages will be within specified limits and will not differ from each other by greater than 0.6 Vdc.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 0.6 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the B-Y Output Voltage = 5 Vp-p. The Chroma Input Voltage at this point should be equal to or less than 0.7 Vp-p.
4. With normal Reference Input Signal Voltage, adjust the Chroma Input Signal until the B-Y Output Voltage = 5 Vp-p. At this point, the R-Y and G-Y voltages will fall within the specified limits.

TEST CIRCUITS

(V^+ = 24 Vdc, R_L = 3.3 kΩ, T_A = +25°C unless otherwise noted)

FIGURE 2 – TEST CIRCUIT WITH NO REFERENCE INPUT SIGNAL

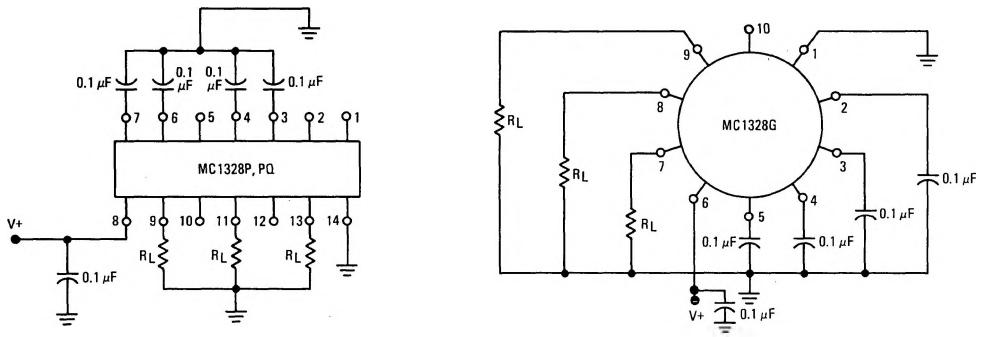
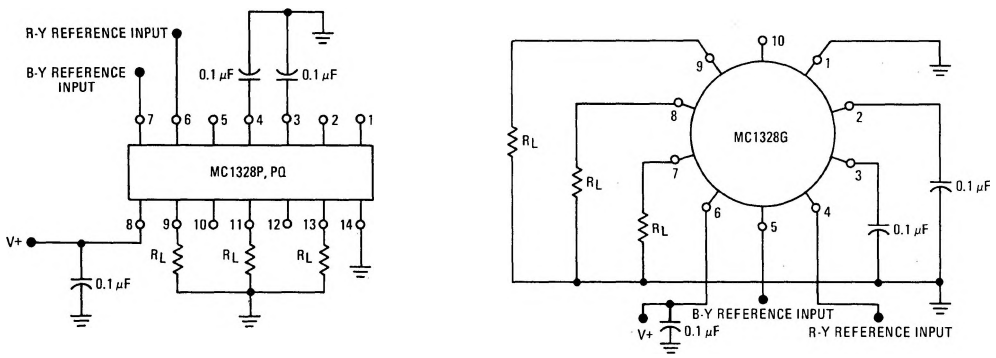


FIGURE 3 – TEST CIRCUIT WITH REFERENCE INPUT SIGNAL
(Quiescent Current, DC Output Voltage, Difference Voltage)



TYPICAL CHARACTERISTICS

FIGURE 4 – DETECTED OUTPUT

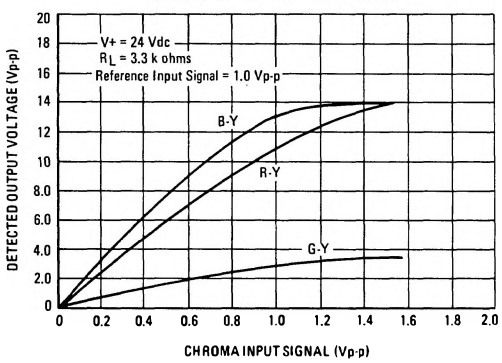
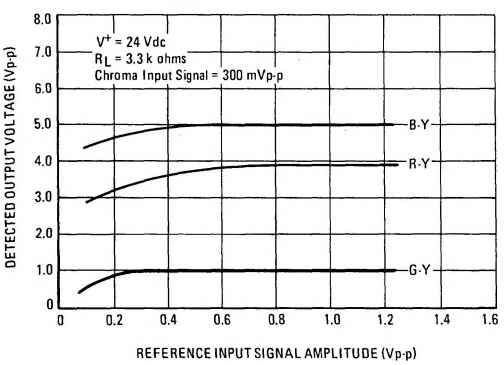


FIGURE 5 – DETECTED OUTPUT



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – DETECTED OUTPUT VOLTAGE

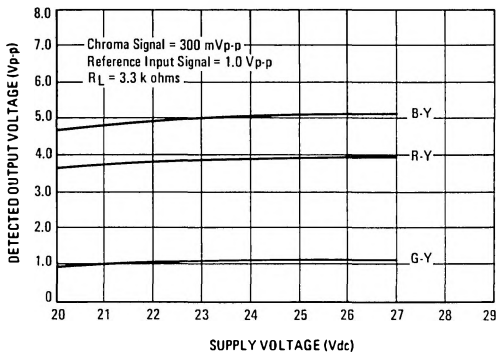


FIGURE 7 – DC OUTPUT VOLTAGE

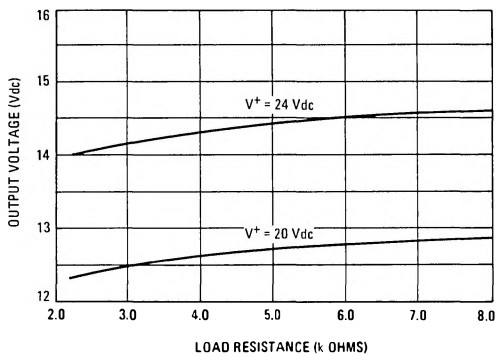


FIGURE 8 – DC OUTPUT VOLTAGE

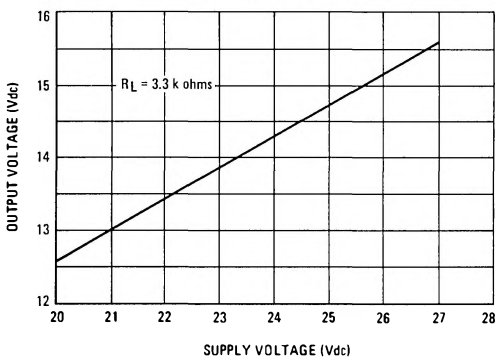


FIGURE 9 – POWER DISSIPATION

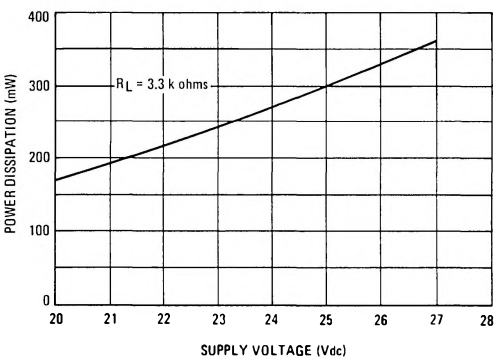


FIGURE 10 – POWER DISSIPATION

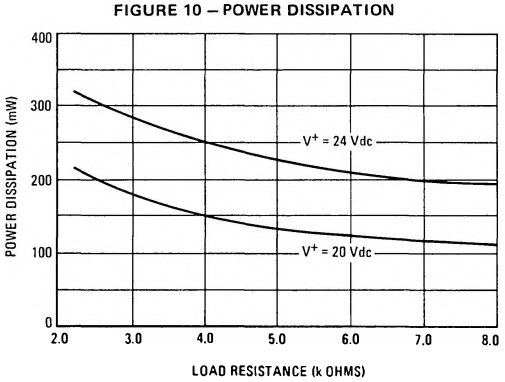
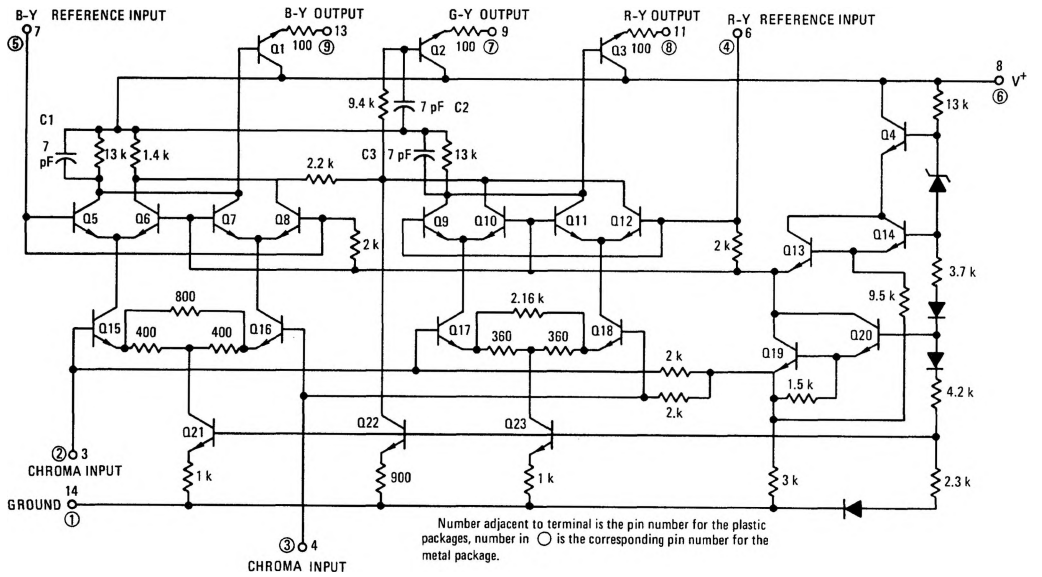


FIGURE 11 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

A double sideband suppressed carrier chroma signal flows between the bases of the two differential pairs, Q15 and Q16, Q17 and Q18. A reference signal of approximately 1 Vp-p amplitude having the same frequency as the suppressed chroma carrier with an appropriate phase relationship is supplied between the bases of the upper differential pairs Q5 and Q6, Q7 and Q8, Q9 and Q10, Q11 and Q12. The upper pairs are switched between full conduction and zero conduction at the carrier frequency rate. The collectors of the upper pairs are cross-coupled so that "doubly balanced" or "full-wave" synchronous detected chroma signals are obtained. Both positive and negative phases of the detected signal are available at opposite collector pairs.

Capacitors C1, C2 and C3 provide filtering of carrier harmonics from the detected color difference signals. This increases the available swing before clipping for the color difference signal, and reduces the high frequency components which must pass through the emitter followers (Q1, Q2, Q3) into the video output stages. Since high capacitance (>100 pF) is characteristic of the input impedance of a video output stage, the transistor emitter followers must operate at a high quiescent current (>5 mA) in order to pass large high frequency components without distortion. The filtering reduces the quiescent current required in the emitter followers and thus reduces dissipation in the integrated circuit.