

# MC1304 MC1305

## STEREO DEMODULATOR

### MONOLITHIC FM MULTIPLEX STEREO DEMODULATORS

... derive the left and right audio information from the detected composite signal. The MC1304 eliminates the need for an external stereo-channel separation control. The MC1305 is similar to the MC1304 but permits the use of an external stereo-channel separation control for maximum separation.

- Operation Practicable Over Wide Power-Supply Range, 8-14 Vdc
- Built-in Stereo-Indicator Lamp Driver
- Total Audio Muting Capability
- Automatic Switching – Stereo-Monaural
- Monaural Squelch Capability

### FM MULTIPLEX STEREO DEMODULATOR

#### SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX  
PLASTIC PACKAGE  
CASE 605  
TO-116



PQ SUFFIX  
PLASTIC PACKAGE  
CASE 647

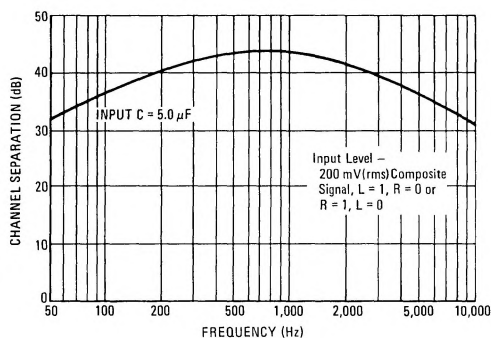
#### MAXIMUM RATINGS ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage (Pins 1, 6, 9, 11, 12) (Pin 7 is grounded)	+22	Vdc
Lamp Driver Current	40	mAdc
Power Dissipation (Package Limitation) (Both Packages)	625	mW
Derate above $T_A = 25^\circ\text{C}$	5.0	mW/ $^\circ\text{C}$
Operating Temperature Range (Ambient)	0 to +75	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$

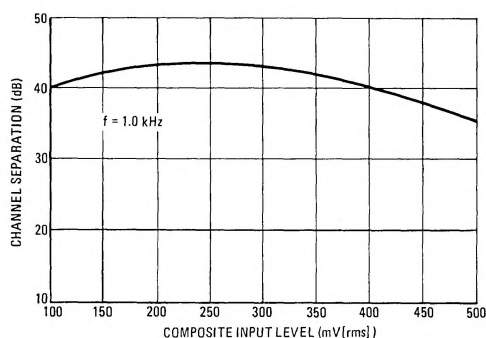
\* Pin 8 for MC1305

\*\*Maximum Ratings\*\* as defined in MIL-S-19500, Appendix A.

CHANNEL SEPARATION versus FREQUENCY



CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL



MC1304,MC1305 (continued)

**ELECTRICAL CHARACTERISTICS** ( $V+ = 12$  Vdc,  $T_A = +25^\circ\text{C}$  unless otherwise noted. Test made with 75  $\mu\text{s}$  de-emphasis network (3.9 k $\Omega$ , 0.02  $\mu\text{F}$ ) unless otherwise noted).

Characteristics	Min	Typ	Max	Unit
Input Impedance ( $f = 20$ Hz)	12	20	—	k $\Omega$
Stereo Channel Separation (See Notes 1 and 2) ( $f = 100$ Hz) ( $f = 1.0$ kHz) ( $f = 10$ kHz)	— — —	35 45 30	— — —	dB
Channel Balance (Monaural Input = 200 mV(rms)), (Monaural, Left and Right Outputs)	—	0.5	—	dB
Total Harmonic Distortion (See Notes 1 and 3) (Modulation frequency - 1.0 kHz)	—	0.5	1.0	%
Ultrasonic Frequency Rejection (See Note 4) (19 kHz) (38 kHz)	— —	25 20	— —	dB
Inherent SCA Rejection (without filter) @ 60 kHz, 67 kHz and 74 kHz	—	50	—	dB
Lamp Indicator ( $R_A = 120\Omega$ ) Minimum 19 kHz Input Level for lamp on Maximum 19 kHz Input Level for lamp off	— 5.0	16 14	25 —	mV(rms)
Audio Muting Mute on (Voltage required at pin 5) Mute off (Voltage required at pin 5) Attenuation in Mute Mode (Note 5)	0.6 1.3 —	— — 55	1.0 2.0 —	Vdc Vdc dB
Stereo-Monaural Switching Stereo (Voltage required at pin 4) Monaural (Voltage required at pin 4)	1.3 —	— —	2.0 1.0	Vdc
Power Dissipation ( $V+ = 10$ V) (Without lamp) (With lamp)	— —	150 180	300 300	mW

Note 1 — Measurement made with 200 mV(rms) Standard Multiplex Composite Signal and  $L = 1$ ,  $R = 0$  or  $R = 1$ ,  $L = 0$ . Standard Multiplex Composite signal is here defined as a signal containing left and/or right audio information with a 10% (19 kHz) pilot signal in accordance with FCC regulations.

Note 2 — Stereo channel separation is adjustable for the MC1305 with a resistor from pin 9 to ground.

Note 3 — Distortion specification also applies to Monaural Signal.

Note 4 — Referenced to 1 kHz output signal with Standard Multiplex Composite Input Signal.

Note 5 — This is referenced to 1.0 kHz output signal with either Standard Multiplex Composite Signal or Monaural Input Signal.

FIGURE 1 — DISTORTION COMPONENTS IN AUDIO SIGNAL

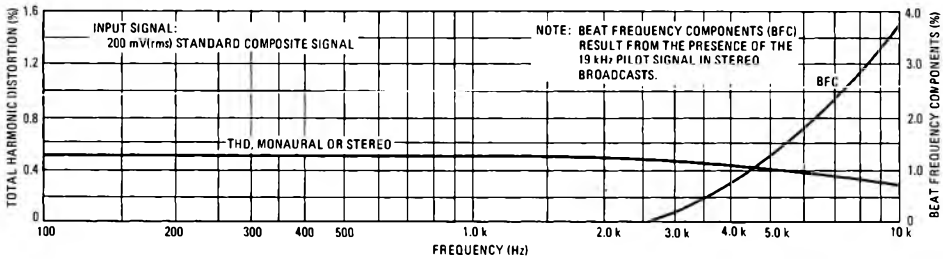


FIGURE 2 — TOTAL HARMONIC DISTORTION

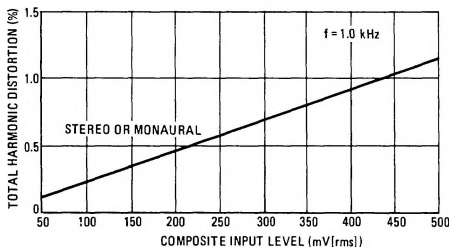
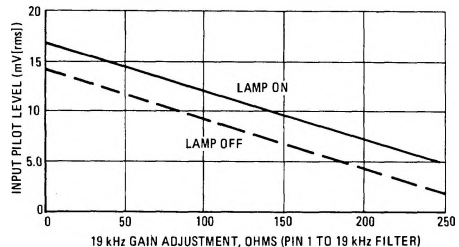


FIGURE 3 — MULTIPLEX SENSITIVITY



MC1304,MC1305 (continued)

FIGURE 4 - MC1304 CIRCUIT SCHEMATIC

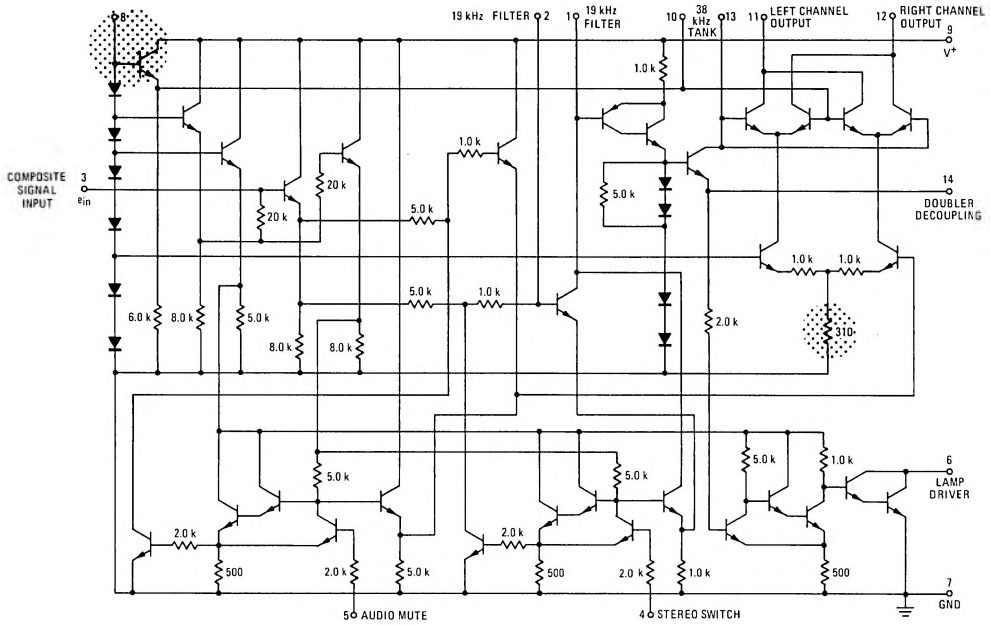
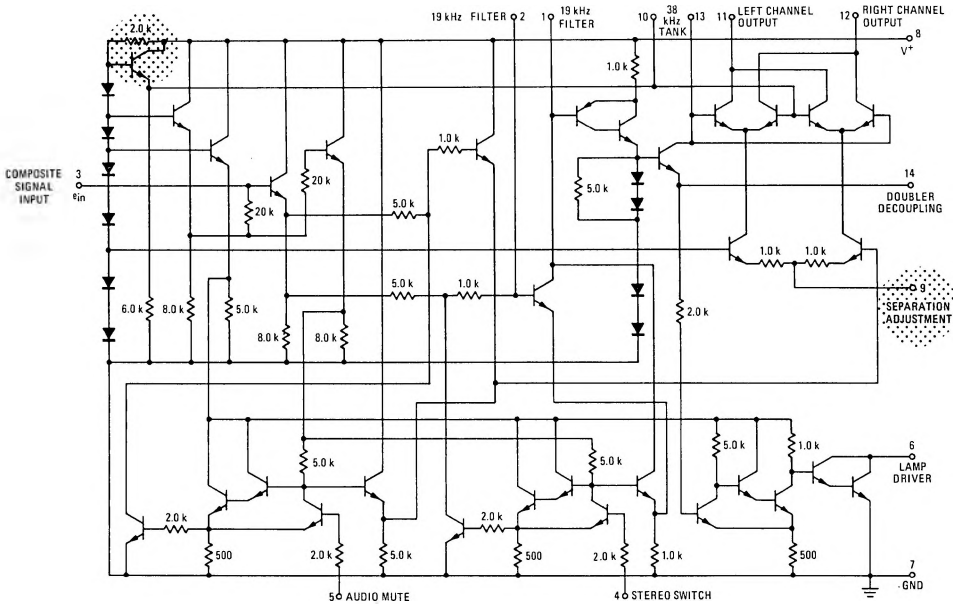


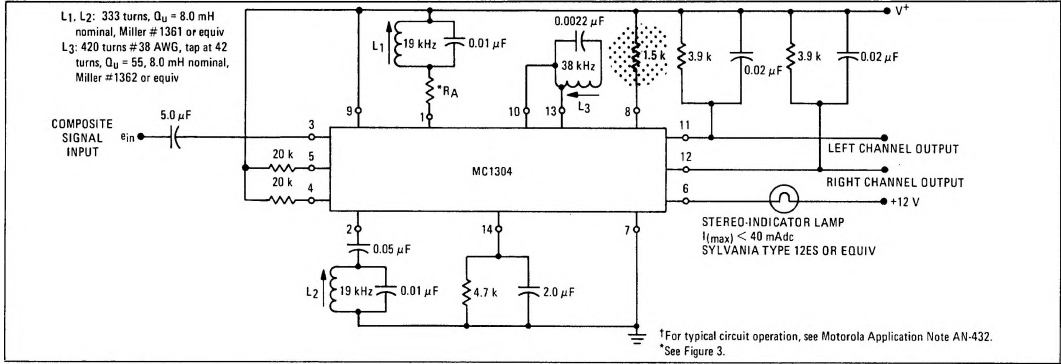
FIGURE 5 - MC1305 CIRCUIT SCHEMATIC



Portions of the circuits shown within the dotted areas pertain to the MC1304 or MC1305 as indicated by the titles of the circuits.

# MC1304, MC1305 (continued)

**FIGURE 6 – MC1304 TYPICAL CIRCUIT CONFIGURATION†**



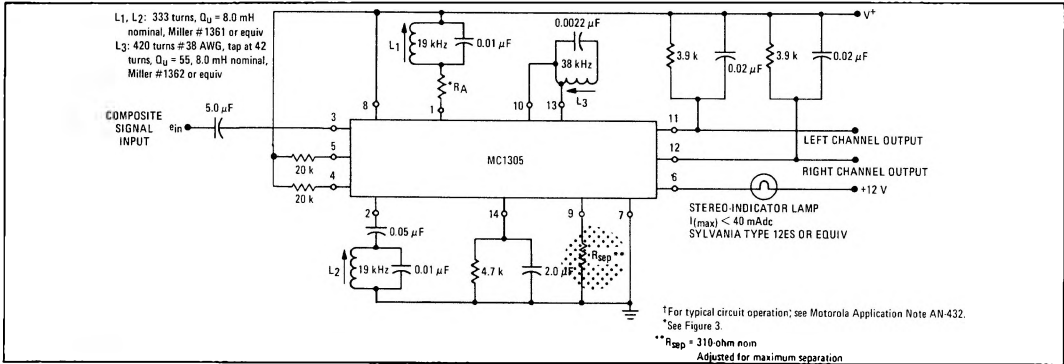
Typical dc voltages (All voltages measured with respect to ground, Pin 7,  $R_A = 0$ )

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$V_{CC} = 8.5$ Vdc	8.5	2.0	2.8	1.6	1.6	0.8	0	4.6*	8.5	3.9	6.3	6.3	3.9	1.9
$V_{CC} = 12$ Vdc	12	2.0	2.8	1.9	1.9	0.8	0	4.6**	12	3.9	9.7	9.7	3.9	1.9

\* 1.5 k $\Omega$  in series with pin 8

\*\* 2.7 k $\Omega$  in series with pin 8

**FIGURE 7 – MC1305 TYPICAL CIRCUIT CONFIGURATION†**



Typical dc voltages (All voltages measured with respect to ground Pin 7)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$V_{CC} = 8.5$ Vdc	8.5	2.0	2.8	1.6	1.6	0.8	0	8.5	0.32	3.9	6.3	6.3	3.9	1.9
$V_{CC} = 12$ Vdc	12	2.0	2.8	1.9	1.9	0.8	0	12	0.36	3.9	9.7	9.7	3.9	1.9

Portions of the circuits shown within the dotted areas pertain to the MC1304 or MC1305 as indicated by the titles of the circuits.