EMITTER COUPLED AMPLIFIER

MC1110

CASE 89

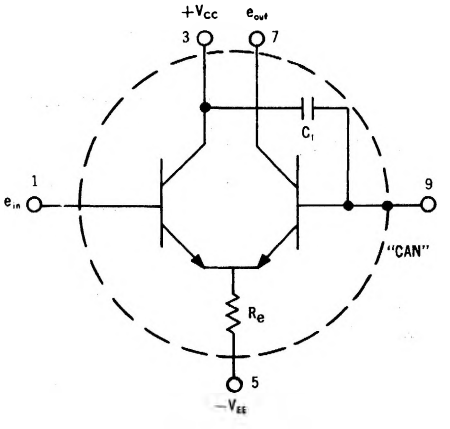
Typical Amplifier Features:

- DC – 300 MHz Performance
- Intended for IF and RF Applications
- 26 dB typ. Gain at 100 MHz
- High Stability Through Low Internal Feedback

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Power Supply Voltage	V_{EE}	14	Vdc
Total Power Dissipation (Derate 5 mW/°C above T_A = 25°C)	P_D	0.5	Watt
Operating Temperature Range	T_j	-55 to+125	°C
Storage Temperature Range	T_{stg}	-65 to+200	°C
Maximum Input Level (RMS)	V_{in}	2	V (RMS)

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

CIRCUIT OPERATION

The input terminal (Pin 1) of the device should be DC ground for optimum DC operating point. Pin 3 is to be supplied with a positive voltage (V_{CC}) for transistor collector and Pin 5 with a negative voltage (V_{EE}) to supply emitter bias current. AGC may be accomplished by variation of V_{EE}. The output of the circuit (Pin 7) should be operated at the same DC potential as is Pin 3. Pin 9 should be AC and DC grounded. Resistor R_e is a diffused silicon resistor, and C_1 is a silicon oxide capacitor.

ELECTRICAL CHARACTERISTICS (at $T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS						
Input Leakage Current (V_3 = 5 Vdc; I_5, I_7, I_9 = 0)		I_1	---	---	10	nAdc
Output Leakage Current (V_7 = 5 Vdc; I_1, I_3, I_5 = 0)		I_9	---	---	10	nAdc
Operating Current (V_{CC} = 5 Vdc, V_{EE} = -4.7 Vdc, V_{in} = 0)	Figure 1	I_{CT}	3.8	4	4.2	mAdc
Input Operating Current V_{CC} = 5 Vdc, (V_{EE} = -10 Vdc, V_{in} = 0)	Figure 1	I_1	---	---	250	μAdc
Reference Operating Current V_{CC} = 5 Vdc, (V_{EE} = -10 Vdc, V_{in} = 0)	Figure 1	I_9	---	---	250	μAdc
Current Balance V_{CC} = 5 Vdc, (V_{EE} = -10 Vdc, V_{in} = 0) V_{CC} = 5 Vdc, V_{EE} = -4.7 Vdc, V_{in} = 0)	 Figure 1 Figure 1	I_3/I_7	 0.90 0.90	 --- ---	 1.10 1.10	---
Large Signal Transconductance (V_{CC} = 5 Vdc, V_{EE} = -4 Vdc, ΔV_{in} = 50 mV)		G_{21}	26	28	---	m-mhos
SMALL-SIGNAL CHARACTERISTICS						
Small Signal Current Gain (V_{CC} = 5 V, I_E = -4 mA, f = 100 MHz)		h_{21}	6.0	9.0	---	---
Short Circuit Admittances (V_{CC} = 5 V, V_{EE} = -4V, f = 100 MHz)	Figure 2	---				m-mhos
Input Admittance		$\|y_{11}\|$	---	2.0	---	
Reverse Transfer Admittance		$\|y_{12}\|$	---	0.064	---	
Forward Transfer Admittance		$\|y_{21}\|$	---	16.3	---	
Output Admittance		$\|y_{22}\|$	---	1.2	---	
Transducer Power Gain (V_{CC} = 5V, V_{EE} = -4V, f = 100 MHz, BW = 3 MHz) (V_{CC} = 5V, V_{EE} = -4V, f = 200 MHz, BW = 6 MHz)	 Figure 20 Figure 21	G_T	 22 15	 26 18	 --- ---	dB
Noise Figure (V_{CC} = 5V, V_{EE} = -4V, f = 100 MHz, $R_g = R_{SO}$)		NF	---	4	6	dB

FIGURE 1 — DC CHARACTERISTICS TEST CIRCUIT

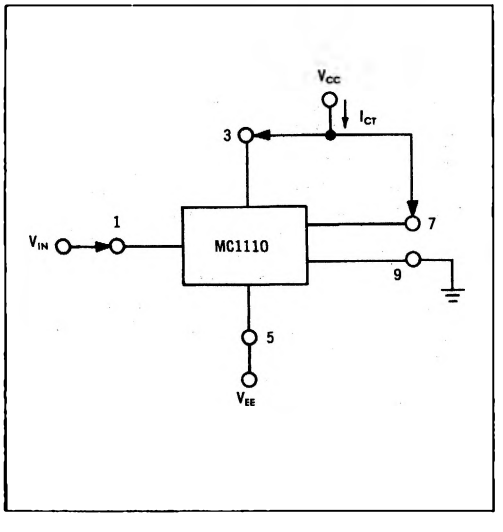
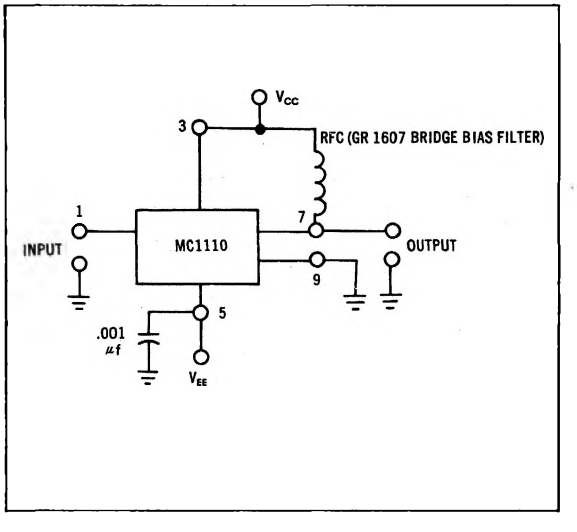
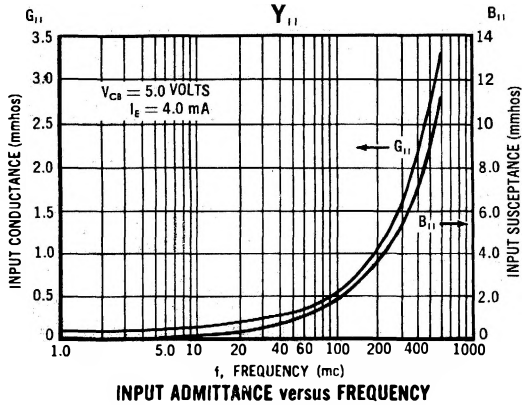


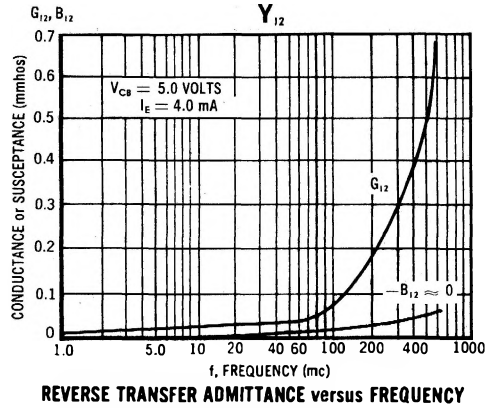
FIGURE 2 — SHORT CIRCUIT ADMITTANCE TEST CIRCUIT
(GENERAL RADIO 1607 A BRIDGE)





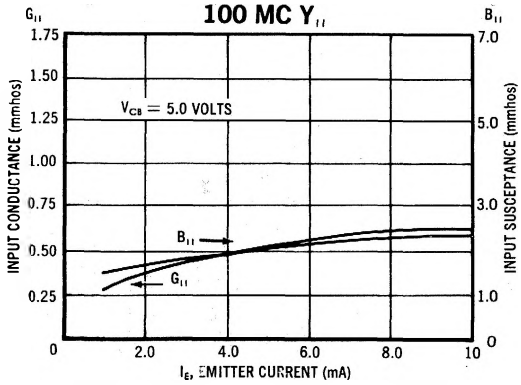
INPUT ADMITTANCE versus FREQUENCY

FIGURE 3



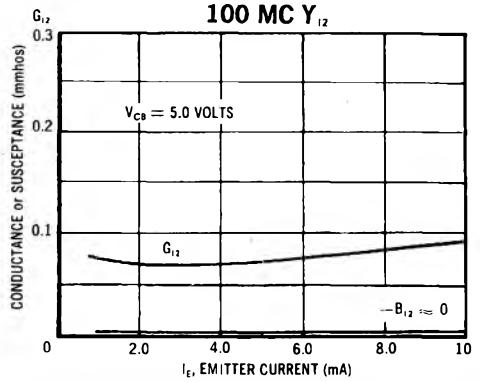
REVERSE TRANSFER ADMITTANCE versus FREQUENCY

FIGURE 6



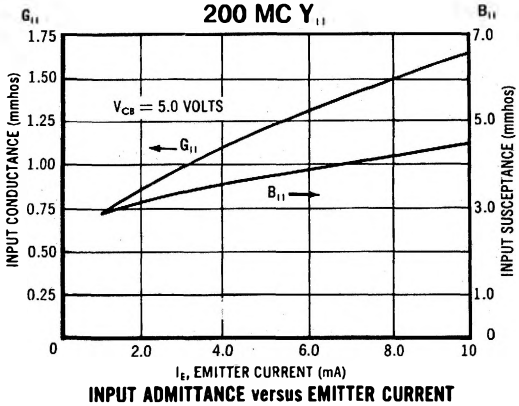
INPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 4



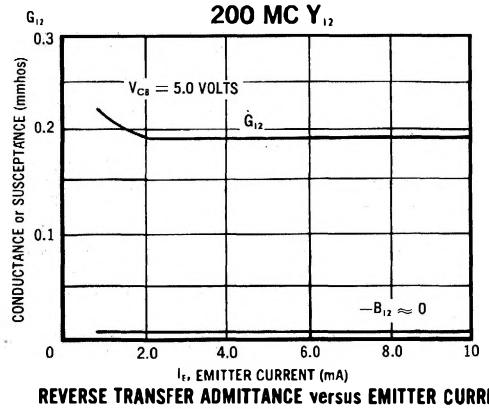
REVERSE TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 7



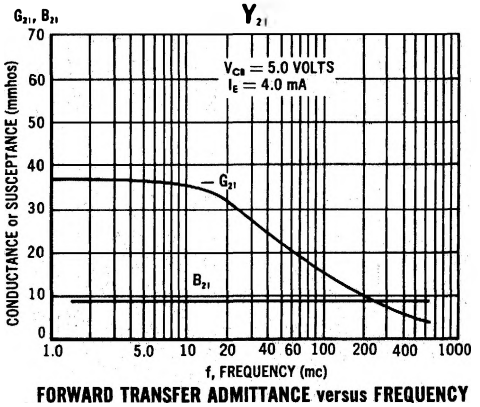
INPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 5



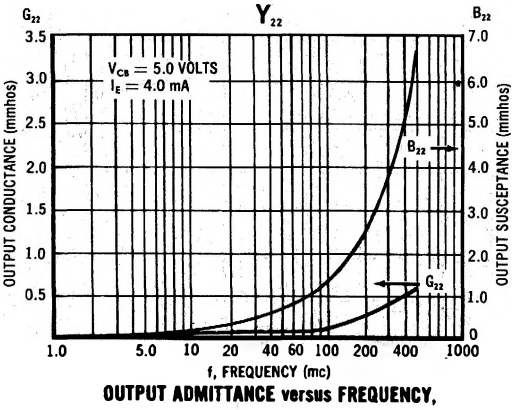
REVERSE TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 8



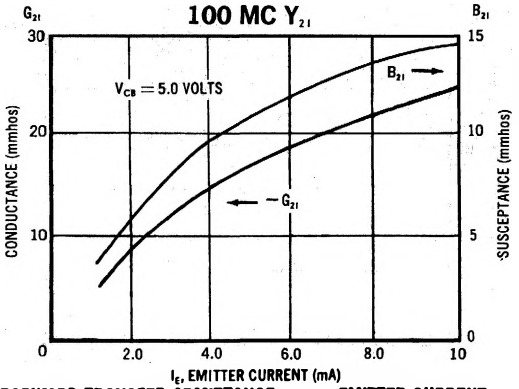
FORWARD TRANSFER ADMITTANCE versus FREQUENCY

FIGURE 9



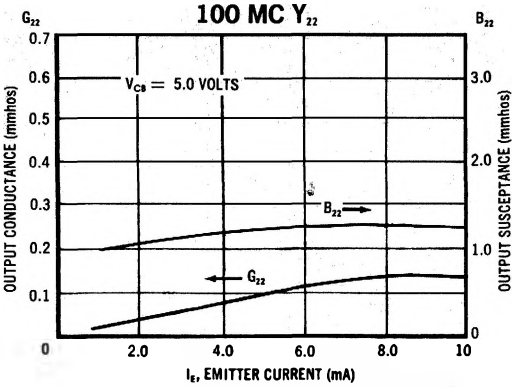
OUTPUT ADMITTANCE versus FREQUENCY,

FIGURE 12



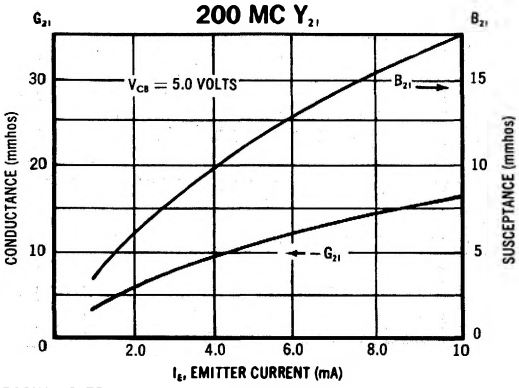
FORWARD TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 10



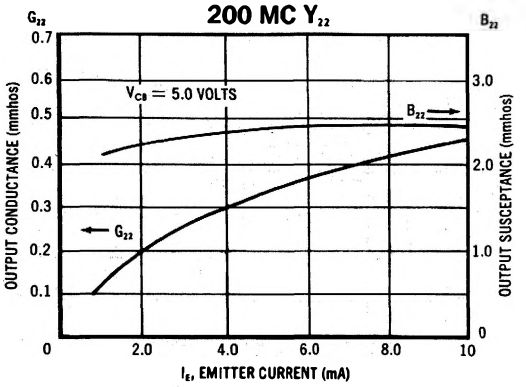
OUTPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 13



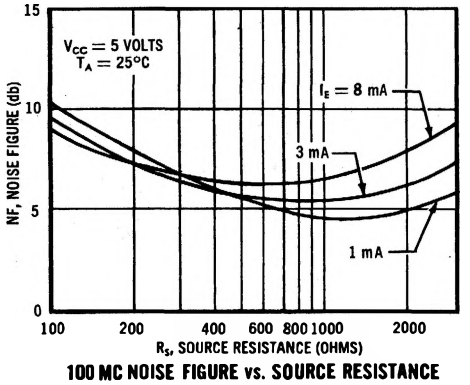
FORWARD TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 11



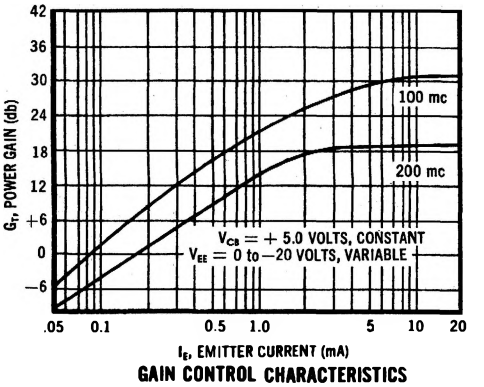
OUTPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 14



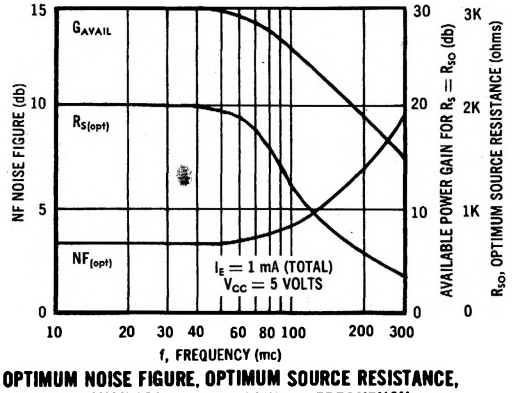
100 MC NOISE FIGURE vs. SOURCE RESISTANCE

FIGURE 15



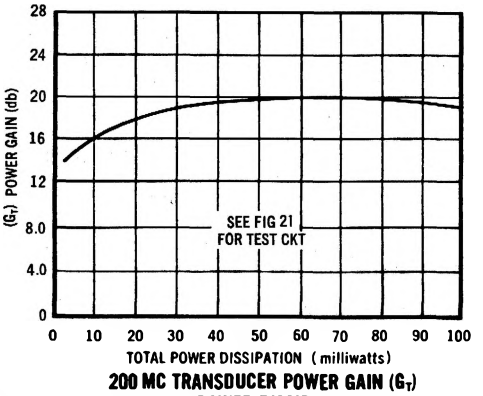
GAIN CONTROL CHARACTERISTICS

FIGURE 16



OPTIMUM NOISE FIGURE, OPTIMUM SOURCE RESISTANCE, AND AVAILABLE POWER GAIN vs. FREQUENCY

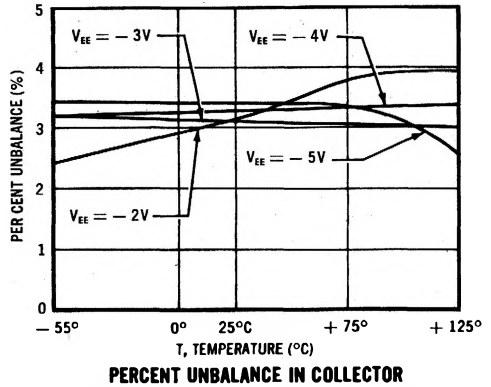
FIGURE 17



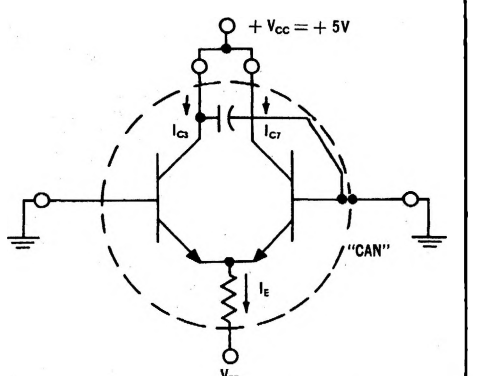
200 MC TRANSDUCER POWER GAIN (G_T) vs. POWER DISSIPATION

FIGURE 18

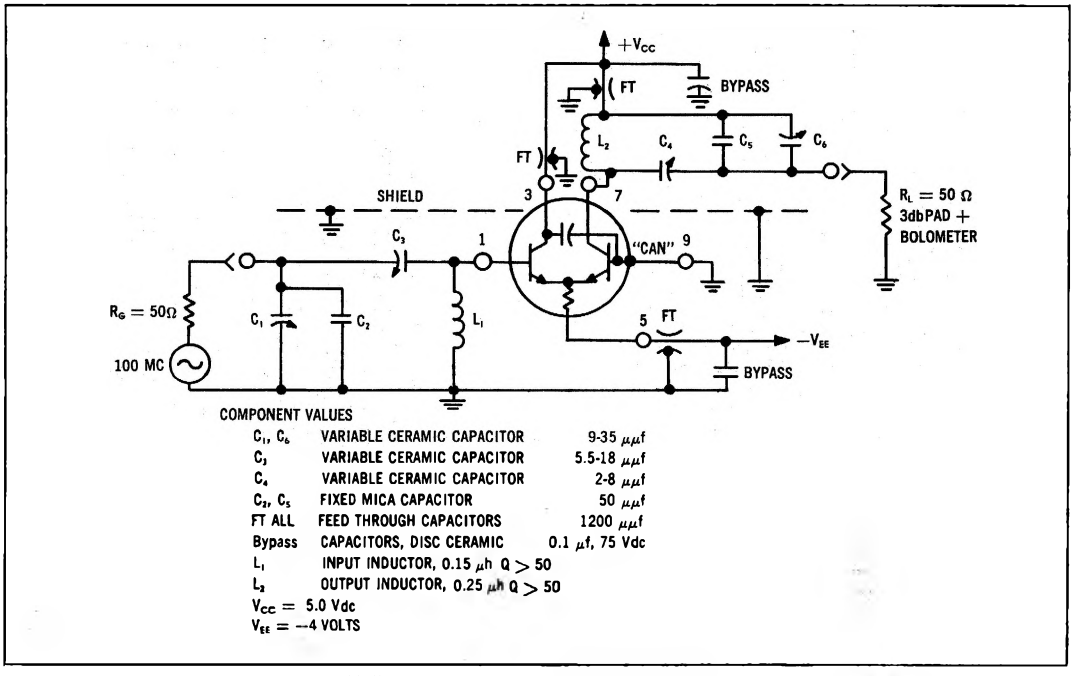
FIGURE 19



PERCENT UNBALANCE IN COLLECTOR CURRENTS (I_{C_3}/I_{C_7}) vs. TEMPERATURE



TEST CIRCUIT

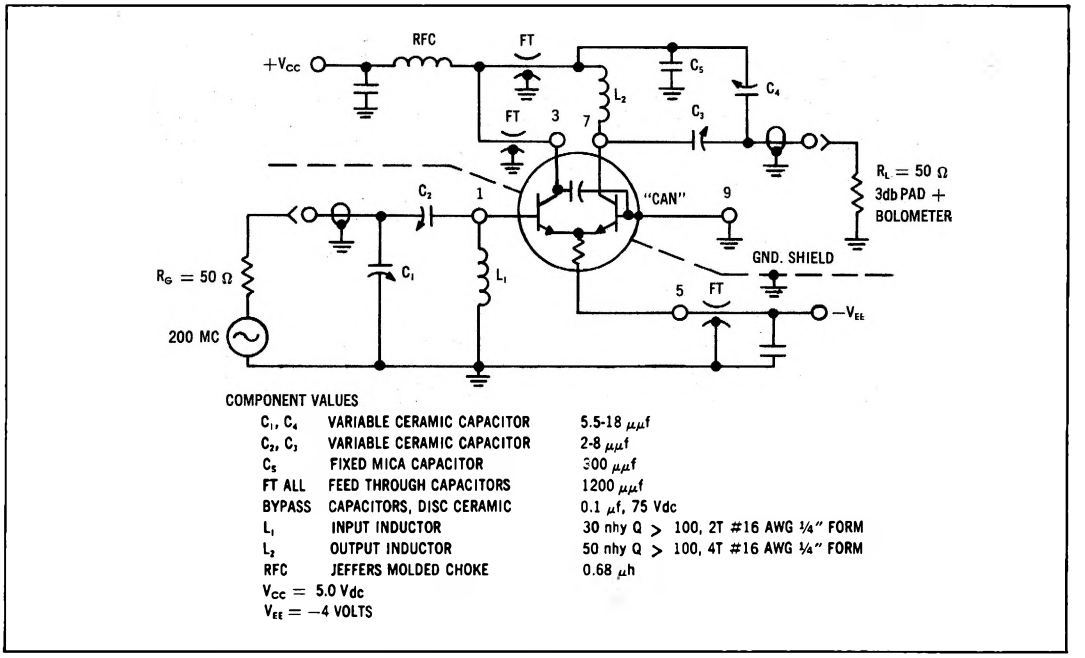


COMPONENT VALUES

C_1, C_6	VARIABLE CERAMIC CAPACITOR	9-35 μμf
C_3	VARIABLE CERAMIC CAPACITOR	5.5-18 μμf
C_4	VARIABLE CERAMIC CAPACITOR	2-8 μμf
C_2, C_5	FIXED MICA CAPACITOR	50 μμf
FT ALL	FEED THROUGH CAPACITORS	1200 μμf
Bypass	CAPACITORS, DISC CERAMIC	0.1 μf, 75 Vdc
L_1	INPUT INDUCTOR, 0.15 μh Q > 50	
L_2	OUTPUT INDUCTOR, 0.25 μh Q > 50	

V_{CC} = 5.0 Vdc
V_{EE} = –4 VOLTS

FIGURE 20 — 100 MC POWER GAIN TEST SET



COMPONENT VALUES

C_1, C_4	VARIABLE CERAMIC CAPACITOR	5.5-18 μμf
C_2, C_3	VARIABLE CERAMIC CAPACITOR	2-8 μμf
C_5	FIXED MICA CAPACITOR	300 μμf
FT ALL	FEED THROUGH CAPACITORS	1200 μμf
BYPASS	CAPACITORS, DISC CERAMIC	0.1 μf, 75 Vdc
L_1	INPUT INDUCTOR	30 nhy Q > 100, 2T #16 AWG ¼" FORM
L_2	OUTPUT INDUCTOR	50 nhy Q > 100, 4T #16 AWG ¼" FORM
RFC	JEFFERS MOLDED CHOKE	0.68 μh

V_{CC} = 5.0 Vdc
V_{EE} = –4 VOLTS

FIGURE 21 — 200 MC POWER GAIN TEST SET