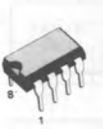
SGS-THOMSON MICROELECTRONICS

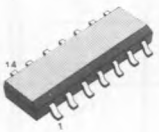
M9346

1024 BIT (64 x 16) SERIAL NMOS EEPROM

- SINGLE SUPPLY READ/WRITE/ERASE OPERATIONS (5V ± 10%)
- TTL COMPATIBLE
- 64 x 16 READ/WRITE MEMORY
- LOW STANDBY CURRENT
- LOW COST SOLUTION FOR NON VOLATILE ERASE AND WRITE MEMORY
- RELIABLE FLOTOX PROCESS
- SELF-TIMED PROGRAMMING CYCLE
- DEVICE STATUS SIGNAL DURING PROGRAMMING
- POWER-ON/OFF DATA PROTECTION CIRCUITRY
- AUTOERASE
- BULK PROGRAMMING ENABLE OR DISABLE FOR ENHANCED DATA PROTECTION



B
DIP-8
(Plastic Package)



M
SO14
(Plastic Micropackage)

(Ordering Information at the end of the datasheet)

DESCRIPTION

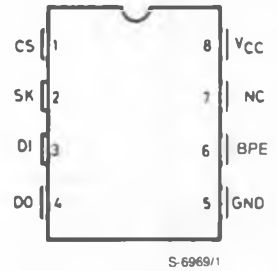
The M9346 is a 1024 bit non-volatile sequential access memory manufactured using SGS-THOMSON FLOATING GATE process. It is a peripheral memory designed for data storage and/or timing and is accessed via a simple serial interface. The device contains 1024 bits organized as 64x16. Written information is stored in a floating gate cell until updated by an erase and write cycle.

Bulk programming instructions (Chip Erase, Chip Write) can be enabled or disabled by the user for enhanced data protection. The M9346 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power down mode allows a consumption decrease by 75%.

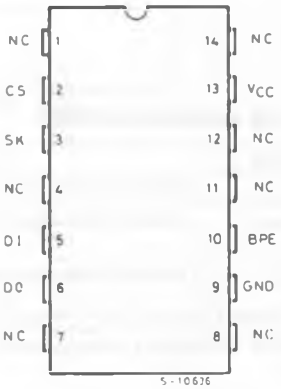
PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND
BPE	BULK PROGRAMMING ENABLE
NC	NO CONNECT

PIN CONNECTIONS

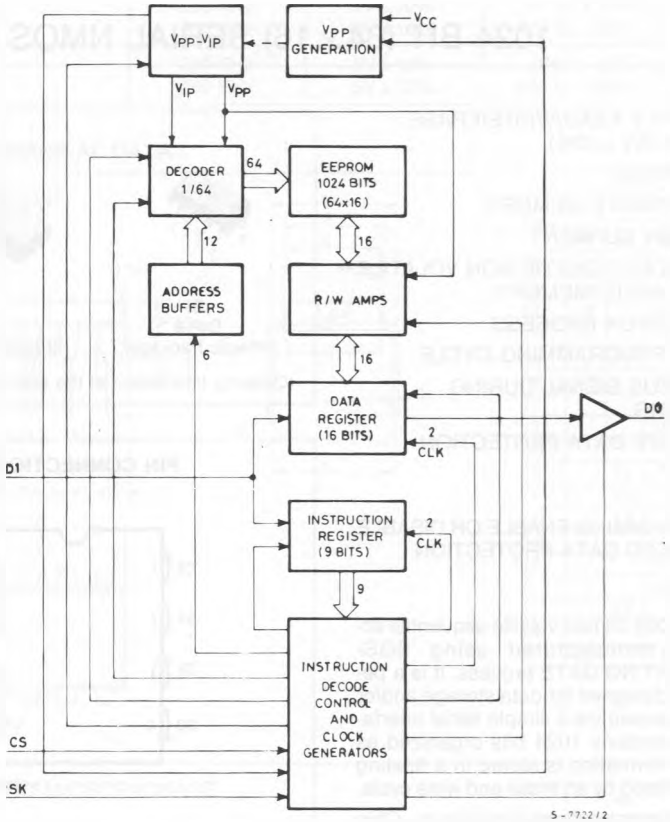


S-6969/1



S-10636

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	Voltage Relative to GND	+ 6V to − 0.3	V
T_{amb}	Ambient Operating Temperature: standard extended	0 to + 70 − 40 to + 85	°C
T_{stg}	Ambient Storage temperature	− 65 to + 125	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (except for T_{amb}).

ELECTRICAL CHARACTERISTICS (0° to +70°C, for standard Temperarure/−40° to +85°C for extended Temperarure, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
I_{CC1}	Operating Current	$V_{CC} = 5.5V$, CS = 1		1.5	12	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		1.2	3	mA
I_{CC3}	E/W Operating Current	$V_{CC} = 5.5V$, SK = 1		2.5	12	mA
V_{IL} V_{IH}	Input Voltage Levels		−0.1 2.0		0.8 $V_{CC}+1$	V
V_{OL} V_{OH}	Output Voltage Levels	$I_{OL} = 2.1$ mA $I_{OH} = -400\ \mu A$	 2.4		0.4	V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	µA
	SK Frequency		0		250	kHz
	SK Duty Cycle		25		75	%
	Input Set-Up and Hold Times:					
t_{CSAE} t_{CSS} t_{CSH}	CS (Note 2)		0.4 0.2 0			µs
t_{DIS} t_{DIH}	DI		0.4 0.4			
t_{PD1} t_{PD0}	Output DO	CL = 100 pF $V_{OL} = 0.8V$, $V_{OH} = 2V$ $V_{IL} = 0.45V$, $V_{IH} = 2.40V$			2 2	µs
$t_{E/W}$	Self-Timed Program Cycle				10	ms
t_{CS}	Min CS Low Time (Note 1)		1			µs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF			1	µs
t_{0H}, t_{1H}	Falling Edge of CS to DO tri-state				0.4	µs

Note: 1. CS must be brought low for a minimum of 1µs (t_{CS}) between consecutive instruction cycles.
2. t_{CSAE} condition has to be fullfilled in "WRITE WITH AUTOERASE" mode.

FUNCTIONAL DESCRIPTION

The input and output pins are controlled by separate serial formats. Eight 9-bit instructions can be executed. The instruction format has a logical "1" as a start bit, two bits as an op code, and six bits of address. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip-erase, chip-write) to prevent spurious programming during other modes.

The programming cycle is self timed, with the data out (DO) pin indicating the ready/busy state of the chip. The serial output (DO) pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in high impedance state eliminating bus contention. The Bulk programming instructions (ERAL, WRAL) are enabled or disabled by the BPE pin. This pin connected to V_{IH} enables the executions of previous mentioned instructions. The BPE pin connected to V_{IL} causes the same instructions to be ignored. If the BPE pin is not connected, it is pulled-up to V_{CC} by an on-chip pull-up and the Bulk programming instructions are enabled. Execution of the EWEN, EWDS, WRITE and ERASE instructions are independent from the state of the BPE pin.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16 bit serial out shift register. A dummy bit (logical "0") precedes the 16 bit data output string. The output data changes during the high state of the system clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 2)

Like most EEPROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an ERASE instruction is input, CS is dropped low.

This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 2)

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specifed in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

WRITE WITH AUTOERASE (Note 2)

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (DO) is put on the data in (DI) pin CS must be brought low before the next falling edge of the SK clock.

This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specifed in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

FUNCTIONAL DESCRIPTION (Continued)

CHIP ERASE (Note 2)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a WRITE instruction. The chip erase cycle is identical to the erase cycle except for the different op code. The Chip Erase (ERAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

CHIP WRITE (Note 2)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction. The Chip Write (WRAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedance of Data Out and the signal source driving A_0. The higher current sourcing capability of A_0, the higher voltage at the Data Out pin. To solve this problem the DI pin must be in high impedance after the last rising edge of the SK clock.

POWER ON DATA PROTECTION CIRCUITRY

During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

Note 1: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 2: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e. start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

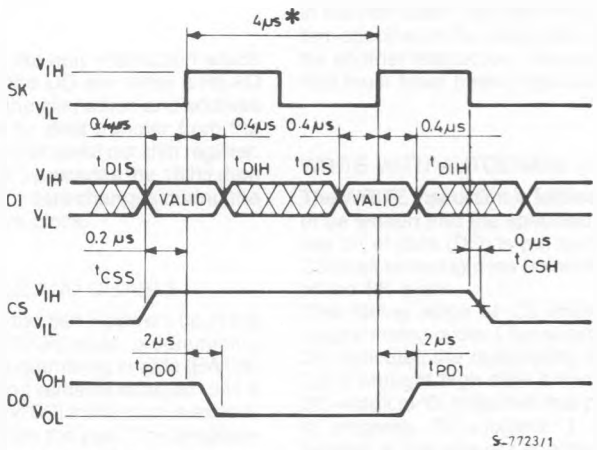
INSTRUCTION SET

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
WR. AUTOERASE	1	01	A5A4A3A2A1A0	D15-D0	Erase/write register A5A4A3A2A1A0
EWEN	1	00	11 x x x x		Erase/write enable
EWDS	1	00	00 x x x x		Erase/write disable
ERAL	1	00	10 x x x x		Erase all registers
WRAL	1	00	01 x x x x	D15-D0	Write all registers

M9346 has 8 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

TIMING DIAGRAMS

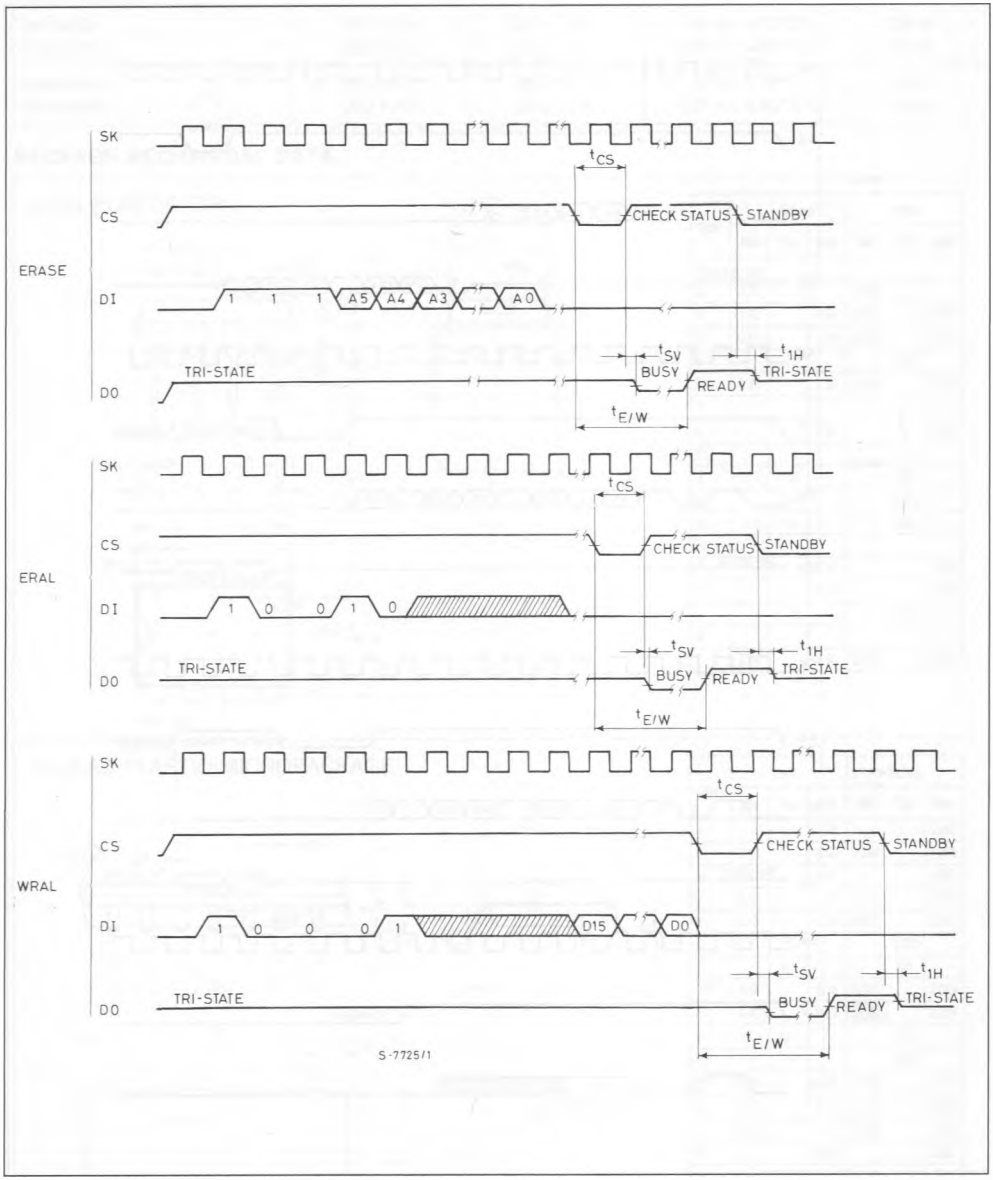
SYNCHRONOUS DATA TIMING



* THIS IS THE MINIMUM SK PERIOD

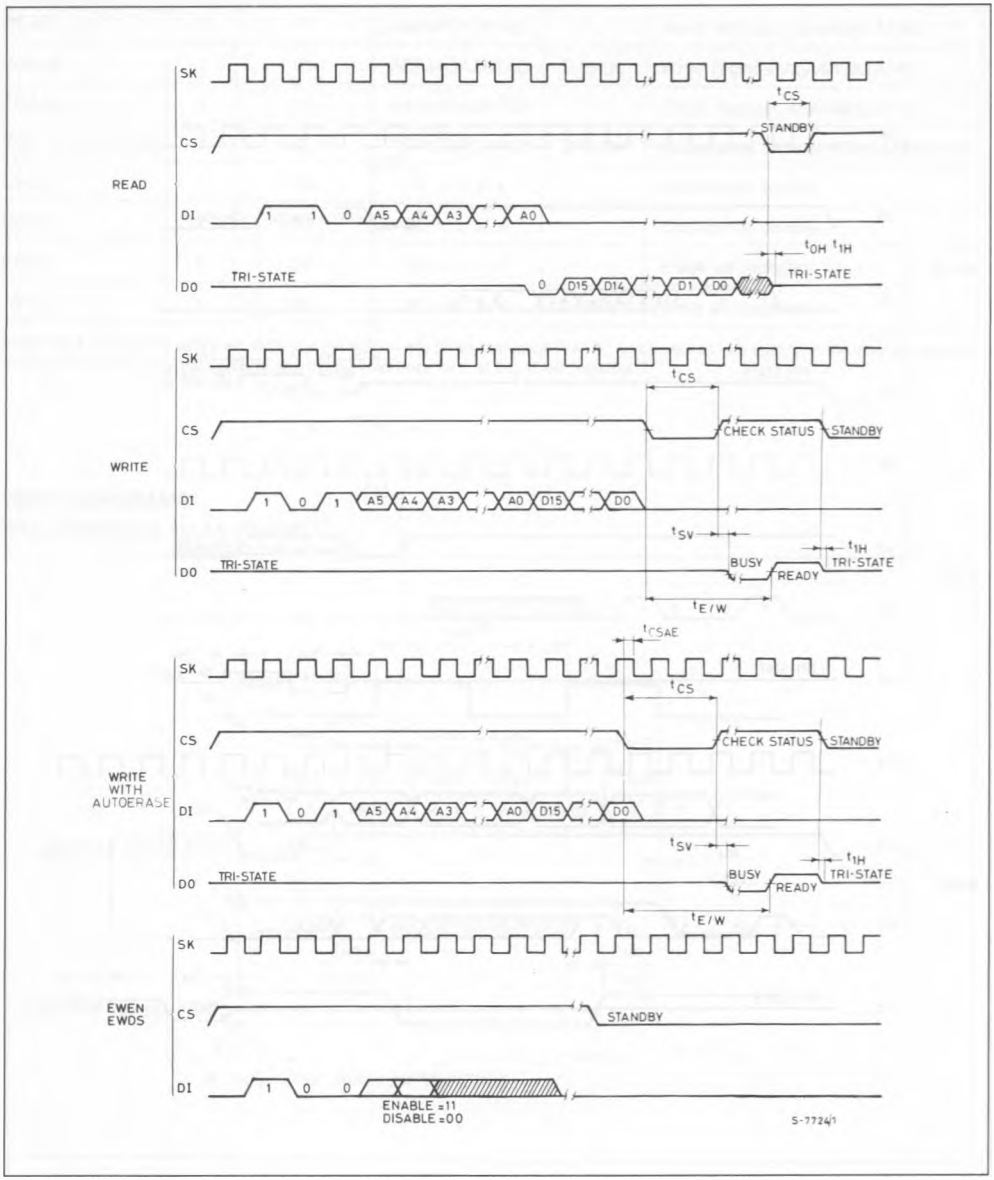
TIMING DIAGRAMS

INSTRUCTION TIMING



TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING

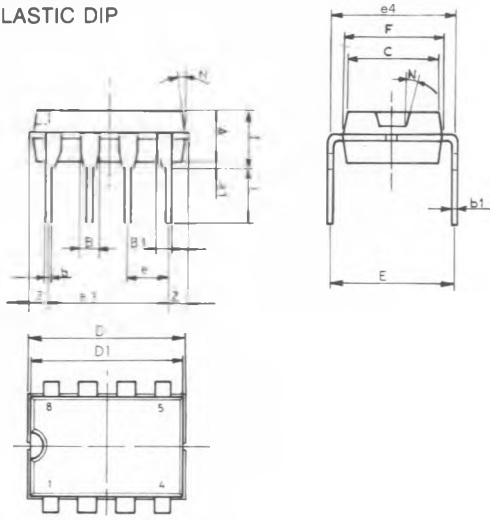


ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
M9346B1	250 KHz	5V ± 10%	0° to +70°C	DIP-8
M9346B6	250 KHz	5V ± 10%	−40° to +85°C	DIP-8
M9346M1	250 KHz	5V ± 10%	0° to +70°C	SO14
M9346M6	250 KHz	5V ± 10%	−40° to +85°C	SO14

PACKAGE MECHANICAL DATA

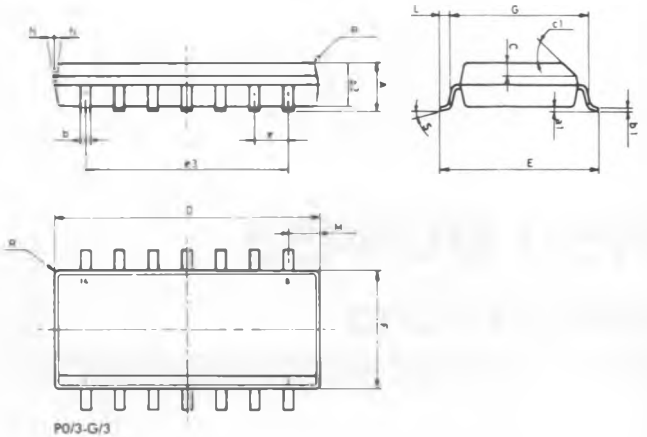
8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

14-LEAD PLASTIC MICROPACKAGE



P0/3-G/3

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.069
a1	0.10		0.20	0.004		0.008
a2			1.60			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.50			0.020	
c1		45°			45°	
D(1)	8.55		8.75	0.337		0.344
E	5.80		6.20	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F(1)	3.80		4.00	0.150		0.157
G	4.60		5.30	0.181		0.209
L	0.50		1.27	0.020		0.050
M			0.68			0.027
N						
R						
S			8°			8°

Note: 1. D and F do not include mold flash or protusions. They should not exceed 0.15 mm/.006 inches.