MILITARY TEMP.

M8228/M8238
SYSTEM CONTROLLER AND BUS DRIVER FOR M8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **M8238 has Advanced $\overline{IOW}$/ $\overline{MEMW}$ for Large System Timing Control**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Full Military Temperature Range -55° C to +125° C**
- **±10% Power Supply Tolerance**

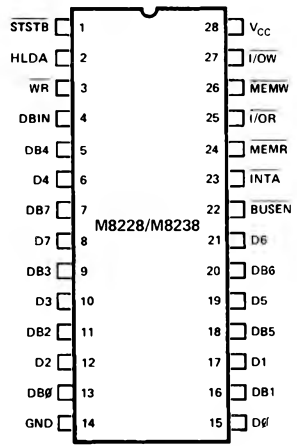
The M8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

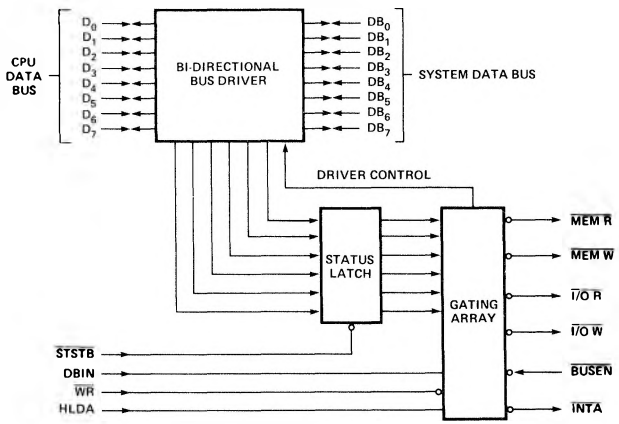
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The M8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the M8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The M8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



M8228/M8238 BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	$\overline{INTA}$	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{I/OR}$	I/O READ	$\overline{WR}$	WR (FROM 8080)
$\overline{I/OW}$	I/O WRITE	$\overline{BUSEN}$	BUS ENAPLE INPUT
$\overline{MEMR}$	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
$\overline{MEMW}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Supply Voltage, V_{CC} . . . . . -0.5V to +7V
Input Voltage . . . . . -1.0V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to 125°C; V_{CC} = 5V ±10%.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		-1.2	V	I_C = -5mA
I_F	Input Load Current, $\overline{STSTB}$		500	μA	V_F = 0.4V
	D_2, D_6		750	μA	
	D_0, D_1, D_4, D_5, D_7		250	μA	
	All Other Inputs		250	μA	
I_R	Input Leakage Current DB_0 - D_7		20	μA	V_R = 5.5V
	All Other Inputs		100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8	2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		210	mA	
V_{OL}	Output Low Voltage, D_0 - D_7		.5	V	I_{OL} = 2mA
	All Other Outputs		.5	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0 - D_7	3.3		V	I_{OH} = -10μA
	All Other Outputs	2.4		V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15	90	mA	V_{CC} = 5V
$I_{O\ (Off)}$	Off State Output Current, All Controls Outputs		100	μA	V_O = 5.5V
			-100	μA	V_O = .45V
I_{INT}	$\overline{INTA}$ Current		5	mA	(See Figure on page 3)

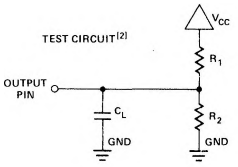
Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

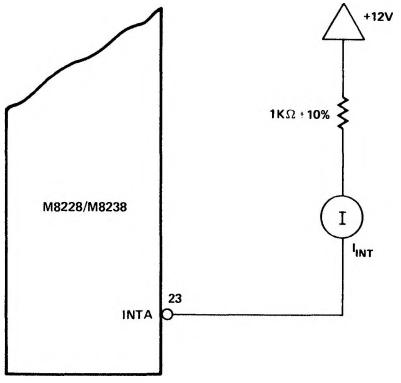
CAPACITANCE This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



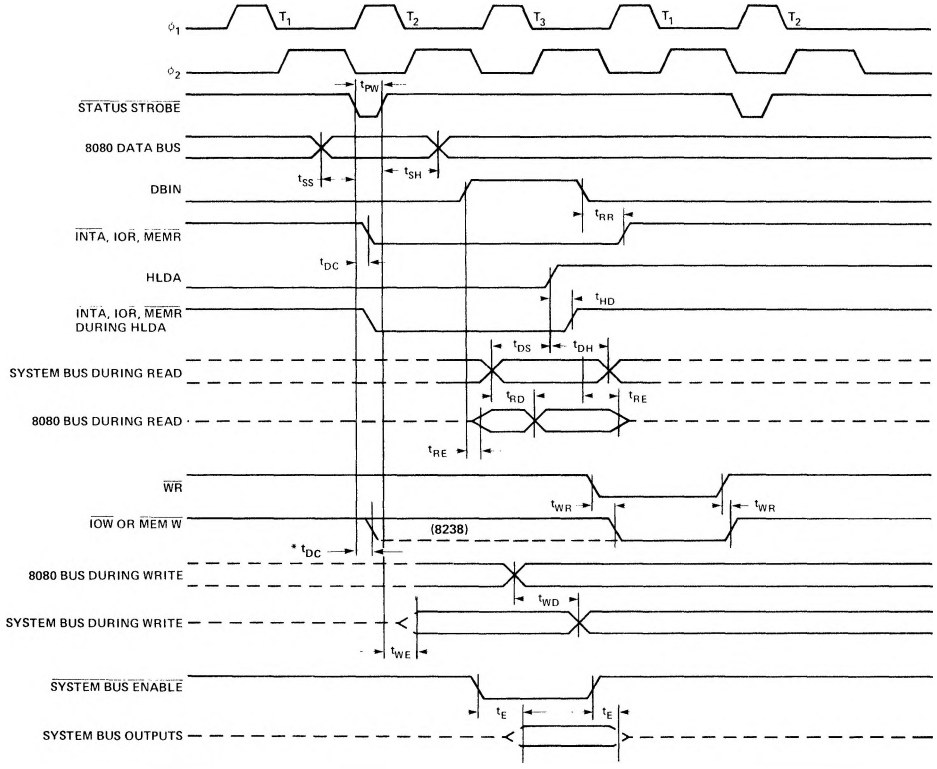


INTA Test Circuit (for RST 7)

A.C. CHARACTERISTICS $T_A = -55°C$ to $125°C$; $V_{CC} = 5V \pm 10\%$.

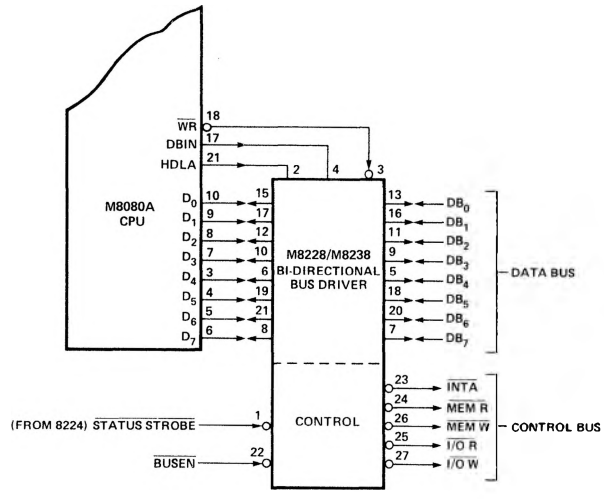
Symbol	Parameter	Limits Min.	Max.	Units	Condition
t_{PW}	Width of Status Strobe	25		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	75	ns	$C_L = 100pF$
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100pF$
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25pF$
t_{RD}	Delay from System Bus to 8080 Bus during Read		45	ns	$C_L = 25pF$
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	60	ns	$C_L = 100pF$
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100pF$
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	$C_L = 100pF$
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7		30	ns	$C_L = 100pF$
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100pF$
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

WAVEFORMS

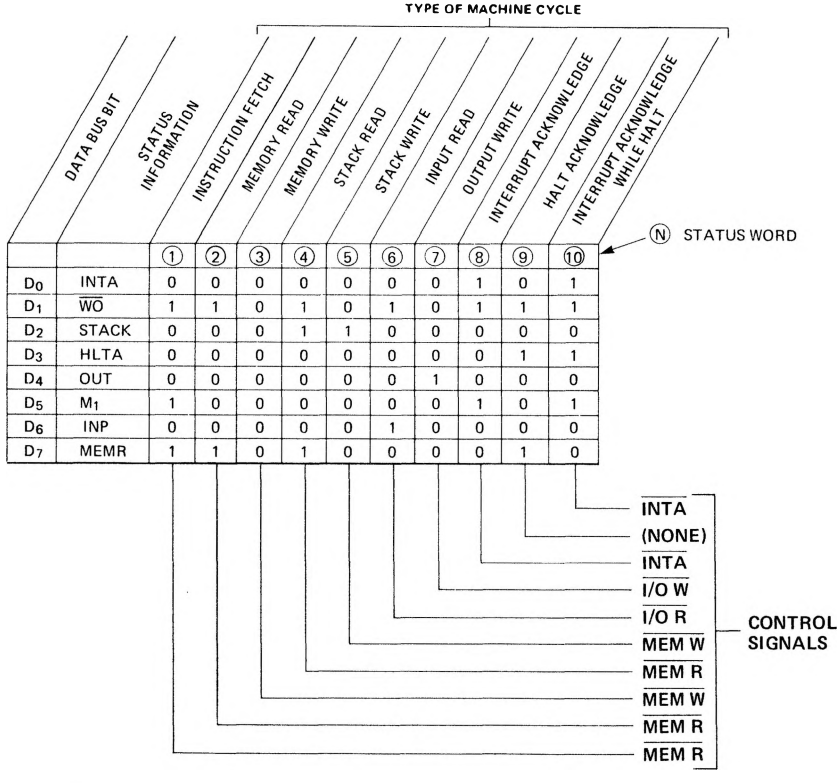


VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*Advanced $\overline{IOW}/\overline{MEMW}$ for M8238 only.



M8080A CPU Interface



Status Word Chart