SINGLE CHIP PCM CODEC AND FILTER

- A-LAW, 2.048MHz MASTER CLOCK
- 300MIL 16-PIN PACKAGE FOR HIGHER LINE-CARD DENSITY
- AT&T D3/D4 AND CCITT COMPATIBLE
- VARIABLE TIMING MODE FOR FLEXIBLE DIGITAL INTERFACE : SUPPORTS DATA RATES FROM 64KB TO 4.096MB
- FIXED TIMING MODE FOR STANDARD 32-CHANNEL SYSTEMS : 2.048MHz MASTER CLOCK
- FULLY DIFFERENTIAL ARCHITECTURE ENHANCES NOISE IMMUNITY
- LOW POWER CMOS TECHNOLOGY
- 0.5mW TYPICAL POWER DOWN
- 70mW TYPICAL OPERATING
- ON CHIP AUTO ZERO, SAMPLE AND HOLD, AND PRECISION VOLTAGE REFERENCES

DESCRIPTION

The M5917 is a limited feature version of Intel's 2913 and 2914 combination codec/filter chips. They are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven silicon gate technology.

The primary applications for the M5917 is in telephone systems :

- Switching - Digital PBX's and Central Office Switching Systems
- Subscriber Instruments - Digital Handsets and Office Workstations

Other possible applications can be found where the wide dynamic range (78dB) and minimum conversion time (125µs) are required for analog to digital interface functions :

- High Speed Modems
- Voice Store and Forward
- Secure Communications
- Digital Echo Cancellation

Figure 1 : Pin Connection.

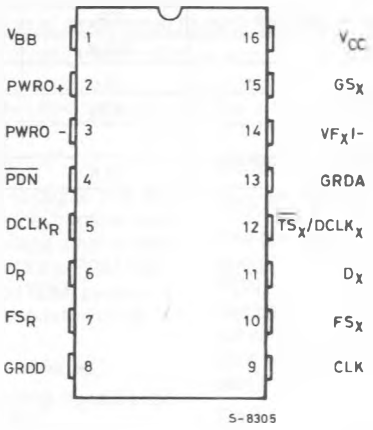


Figure 2 : Block Diagram.

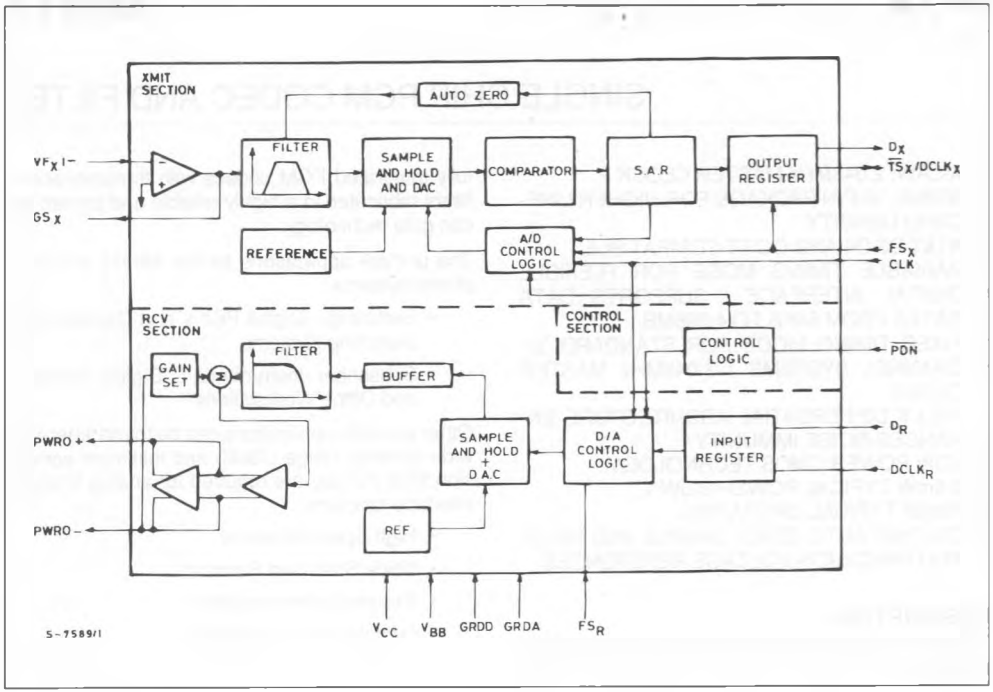


Table 1 : Pin Names.

V_{BB}	Power (– 5V)	GS_X	Transmit Gain Control
PWRO+, PWRO–	Power Amplifier Outputs	$VF_XI–$	Analog Input
$\overline{PDN}$	Power Down Select	GRDA	Analog Ground
$DCLK_R$	Receive Variable Data Clock	$\overline{TS_X}$	Timeslot Strobe/buffer Enable
D_R	Receive PCM Input	$DCLK_X$	Transmit Variable Data Clock
FS_R	Receive Frame	D_X	Transmit PCM Output
	Synchronization Clock	FS_X	Transmit Frame
GRDD	Digital Ground		Synchronization Clock
V_{CC}	Power (+ 5V)	CLK	Master Clock

Table 2 : Pin Description.

Symbol	Function
V_{BB}	Most Negative Supply. Input voltage is – 5 volts ± 5%.
PWRO+	Non-inverting Output of Power Amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO–	Inverting Output of Power Amplifier. Functionally identical and complementary to PWRO+.
$\overline{PDN}$	Power Down Select. When $\overline{PDN}$ is TTL high, the device is active.When low, the device is powered down.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock wich operates at TTL levels from 64kB to 4096MB data rates.
D_R	Receive PCM Input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock ; CLK in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/timeslot enable, receive channel. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 30 miliseconds.
GRDD	Digital Ground for all Internal Logic Circuits. Not internally tied to GRDA.
CLK	Master and data clock for the fixed data rate mode ; master clock only in variable data rate mode.
FS_X	8KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 30 milliseconds.
D_X	Transmit PCM Output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock : CLK in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 2.048MB data rates.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply ; input voltage is + 5 volts ± 5%.

FUNCTIONAL DESCRIPTION

The M5917 provides the analog-to-digital and the digital-to-analog conversion and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highway of a time division multiplexed (TDM) system. It is intended to be used at the analog termination of a PCM line.

The following major functions are provided :

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information

GENERAL OPERATION

SYSTEM RELIABILITY FEATURES

The combochip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The M5917 has internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs DX and $\overline{TS_X}$ are held in a high impedance state for approximately four frames (500µs) after power up or application

of V_{BB} or V_{CC}. After this delay, D_X and $\overline{TS}_X$ will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 35 milliseconds to reach their equilibrium value due to the autozero circuit settling time.

To enhance system reliability, $\overline{TS}_X$ and D_X will be placed in a high impedance state approximately 20µs after an interruption of CLK.

POWER DOWN AND STANDBY MODES

To minimize power consumption, two power down modes are provided in which most M5917 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 0.5mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 1mW. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Table 3 : Power-down Methods.

Device Status	Power-downMethod	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state within 10µs.
Standby Mode	FS_X and FS_R are TTL low.	$\overline{TS}_X$ and D_X are placed in a high impedance state within 30 milliseconds.
Only transmit is on standby.	FS_X is TTL low.	$\overline{TS}_X$ and DX are placed in a high impedance state within 30 milliseconds.
Only receive is on standby.	FS_R is TTL low.	

FIXED DATA RATE MODE

Fixed data rate timing, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clock CLK, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK serves as the master clock to operate the codec and filter sections and as the bit clock to clock the data in and out from the PCM highway. FS_X and FS_R are 8kHz inputs which set the sampling frequency. $\overline{TS}_X$ is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK. The frequency of CLK must be 2.048MHz. No other frequency of operation is allowed in the fixed data rate mode.

VARIABLE DATA RATE MODE

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clock CLK, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64kHz to 4096MHz. The master clock is still restricted to 2.048MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125s frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desi-red, and is only available in the variable data rate mode.

PRECISION VOLTAGE REFERENCES

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique use the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive section are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ± 0.04dB in absolute gain for each half channel. providing the user a significant margin for error in other board components.

TRANSMIT OPERATION

TRANSMIT FILTER

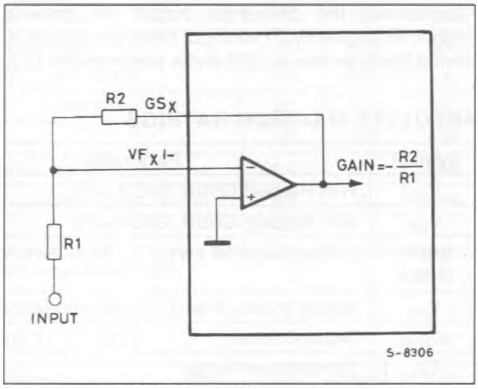
The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1MHz. Gain of up to 20dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel high less than 50pF. The input signal on lead VF_XI can be either AC or DC coupled. The input op amp can only be used in the inverting mode as shown in figure 3.

A low pass anti-aliasing section is included on-chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The M5917 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in figure 4.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60Hz power lines, 17Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200Hz. This feature allows the use of low-cost transformer hybrids without external components.

Figure 3 : Transmit Filter Gain Adjustment.



ENCODING

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

DECODING

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

RECEIVE FILTER

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders. The receive filter characteristics and specifications will be within the limits shown in figure 5.

RECEIVE OUTPUT POWER AMPLIFIERS

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12dBm or 600 ohms differentially to a level of 15dBm.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	With Respect GRDD, GRDA = 0V	– 0.6 to 7	V
V_{BB}	With Respect GRDD, GRDA = 0V	+ 0.6 to – 7	V
GRDD, GRDA	In Such Case : $0 \leq V_{CC} \leq +7V$, $-7V \leq V_{BB} \leq 0V$	± 0.3	V
$V_{I/O}$	Analog Inputs, Analog Outputs and Digital Inputs	$V_{BB} - 0.3 \leq V_{IN}/V_{OUT} \leq V_{CC} + 0.3$	V
V_{ODIG}	Digital Outputs	$GRDD - 0.3 \leq V_{OUT} \leq V_{CC} + 0.3$	V
T_{op}	Temperature Range	– 10 to + 80	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C
P_{tot}	Power Dissipation	1	W

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{BB} = – 5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)
Typical values are for T_A = 25°C and nominal power supply values.

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	$GRDD \leq V_{IN} \leq V_{IL}$ (note 1)			10	µA
I_{IH}	High Level Input Current	$V_{IH} \leq V_{IN} \leq V_{CC}$			10	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA at D_X, $\overline{TS_X}$			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 9.6mA at D_X	2.4			V
C_{OX}	Digital Output Capacitance[2]			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

POWER DISSIPATION All measurements made at f_{DCLK} = 2.048MHz, outputs unloaded.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} Operating Current			6	10	mA
I_{BB1}	V_{BB} Operating Current			6	9	mA
I_{CC0}	V_{CC} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{BB0}	V_{BB} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		300	600	µA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		40	300	µA
P_{D1}	Operating Power Dissipation			60	100	mW
P_{D0}	Power Down Dissipation	PDN ≤ V_{IL} ; after 10µs		0.4	3	mW
P_{ST}	Standby Power Dissipation	FS_X, FS_R ≤ V_{IL} ; after 30ms		1.7	5	mW

Notes : 1. V_{IN} is the voltage on any digital pin.
2. Timing parameters are guaranteed based on a 100pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60pf.
3. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{BX1}	Input Leakage Current, VF_XI-	– 2.17V ≤ V_{IN} ≤ 2.17V			100	nA
R_{IXI}	Input Resistance, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI-				25	mV
A_{VOL}	DC Open Loop Voltage Gain, GS_X	R_L = 10K	5000	20.000		
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	R_L ≥ 10kΩ	– 2.17		2.17	V
C_{LXI}	Load Capacitance, GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			kΩ

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{ORA}	Output Resistance, PWRO+, PWRO–			1		Ω
V_{OSRA}	Single-ended Output DC Offset, PWRO+, PWRO–	Relative to GRDA	– 150	75	150	mV
C_{LRA}	Load Capacitance, PWRO+, PWRO–				100	pF

A.C. CHARACTERISTICS - TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0dBm0, 1020Hz sine wave. Input amplifier is set for unity gain,[2] inverting. The digital input is a PCM bit stream generated by passing a 0dBm0, 1020Hz sine wave through an ideal encoder. Receive output is measured single ended. All output levels are (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EmW	Encoder Milliwatt Response (transmit gain tolerance)	Signal Input of 1.068Vrms T_A = 25°C, V_{BB} = – 5V, V_{CC} = + 5V	– 0.15	± 0.04	+ 0.15	dBm0
EmW_{TS}	EmW Variation with Temperature and Supplies	± 5% Supplies, 0 to 70°C Relative to Nominal Conditions	– 0.1		+ 0.1	dB
DmW	Digital Milliwatt Response (receive gain tolerance)	Measure Relative to $0TLP_R$. Signal Input per CCITT Recommendation G.711. Output Signal of 1000Hz. T_A = 25°C ; V_{BB} = – 5V ; V_{CC} = + 5V	– 0.15	± 0.04	+ 0.15	dBm0
DmW_{TS}	DmW Variation with Temperature and Supplies	± 5% Supplies, 0 to 70°C	– 0.1		+ 0.1	dB
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0dBm0)	Referenced to 600Ω Referenced to 900Ω		+ 2.79 + 1.03		dBm dBm
$0TLP2_R$	Zero Receive Level Point Receive Channel (0dBm0)	Referenced to 600Ω Referenced to 900Ω		+ 5.79 + 4.03		dBm dBm

Notes : 1. 0dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.068 volts rms or an output of 1.516 volts rms.
2. Unity gain input amplifier, signal input VF_{XI} –.

GAIN TRACKING Reference Level = – 10dBm0

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input.	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input.	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB

NOISE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, Psophometrically Weighted	VF_XI+ = GRDA, VF_XI- = GS_X		(1)*	– 80	dBm0p
N_{RP}	Receive Noise, Psophometrically Weighted	D_R = Lowest Positive Decode Level		+ 9	– 81	dBm0p
N_{SF}	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			– 50	dBm0
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
$PSRR_4$	V_{BB} Power Supply Rejection, Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs	VF_XI+ = 0dBm0, 1.02kHz, D_R = Lowest Positive Decode Level. Measure at PWRO+			– 80	dB
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs	D_B = 0dBm0, 1.02kHz, VF_XI+ = GRDA, Measure at D_X			– 80	d

(1) * Noise free : DXPCM Code stable at 01010101.

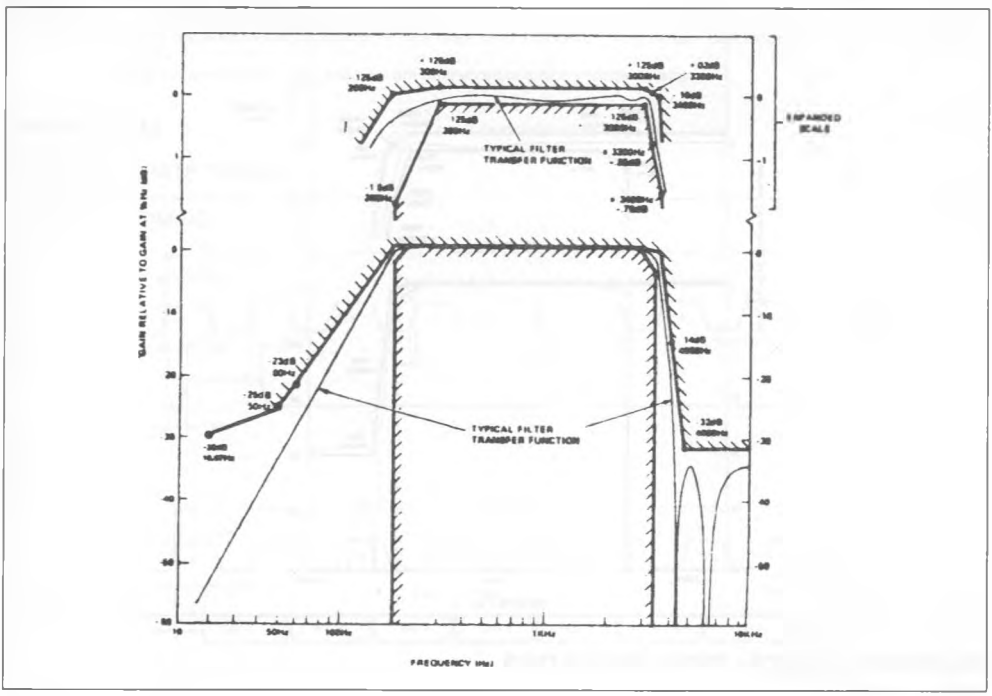
DISTORTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$SD2_X$	Transmit Signal to Distortion, Sinusoidal Input CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30$dBm0 -40dBm0 -45dBm0	36 30 25			dB dB dB
$SD1_R$	Transmit Signal to Distortion, μ-law Sinusoidal Input ; CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30$dBm0 -40dBm0 -45dBm0	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion, Sinusoidal Input ; CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30$dBm0 -40dBm0 -45dBm0	36 30 25			dB dB dB
DP_{X1}	Transmit Single Frequency Distortion Products	AT & T Adivisory = 64 (3.8) 0dBm0 Input Signal			-46	dB
DP_{R1}	Receive Single Frequency Distortion Products	AT & T Adivisory = 64 (3.8) 0dBm0 Input Signal			-46	dB
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			-35	dB
IMD_2	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			-49	dB
SOS	Spurious Out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			-30	dBm0
SIS	Spurious in Band Signals, End to End Measurement	CCITT G.712 (9)			-40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate CLK_X = 2.048MHz ; 0dBm0, 1.02kHz Signal at VF_XI+ Measure at D_X		300		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		170 95 45 80		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed data rate, CLK_R = 2.048MHz ; digital input is DMW codes. Measure at PWRO+		190		μs
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		10 10 85 110		μs μs μs μs

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS Input amplifier is set for unity gain. inverting.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at VF_XI-				
	16.67Hz				– 30	dB
	50Hz				– 25	dB
	60Hz				– 23	dB
	200Hz		– 1.8		– 0.125	dB
	300 to 3000Hz		– 0.125		+ 0.125	dB
	3300Hz		– 0.35		+ 0.03	dB
	3400Hz		– 0.7		– 0.10	dB
	4000Hz				– 14	dB
	4600Hz and Above				– 32	dB

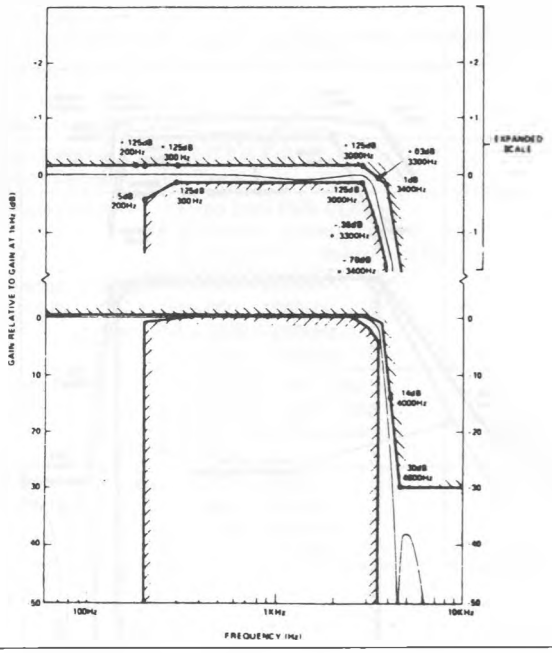
Figure 4 : Transmit Channel.



RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gain at 1.02kHz	0dBm0 Signal Input at D_R				
	below 200Hz				+ 0.125	dB
	200Hz		– 0.5		+ 0.125	dB
	300 to 3000Hz		– 0.125		+ 0.125	dB
	3300Hz		– 0.35		+ 0.03	dB
	3400Hz		– 0.7		– 0.1	dB
	4000Hz				– 14	dB
	4600Hz and Above				– 30	dB

Figure 5 : Receive Channel.



AC CHARACTERISTICS - TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{CY}	Clock Period, CLK	f_{CLK} = 2.048MHz	488			ns
t_{CLK}	Clock Pulse Width	CLK	195			ns
t_{DCLK}	Data Clock Pulse Width[1]	64kHz ≤ f_{DCLK} ≤ 2.048MHz	195			ns
t_{CDC}	Clock Duty Cycle	CLK	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns

AC CHARACTERISTICS - TIMING PARAMETERS (continued)

TRANSMIT SECTION, FIXED DATA RATE MODE[2]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DZX}	Data Enabled on TS Entry	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{DDX}	Data Delay from CLK	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{HZX}	Data Float on TS Exit	$C_{LOAD} = 0$	60		190	ns
t_{SON}	Timeslot X to Enable	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{SOFF}	Timeslot X to Disable	$C_{LOAD} = 0$	50		190	ns
t_{FSD}	Frame Sync Delay		0		120	ns

RECEIVE SECTION, FIXED DATA RATE MODE

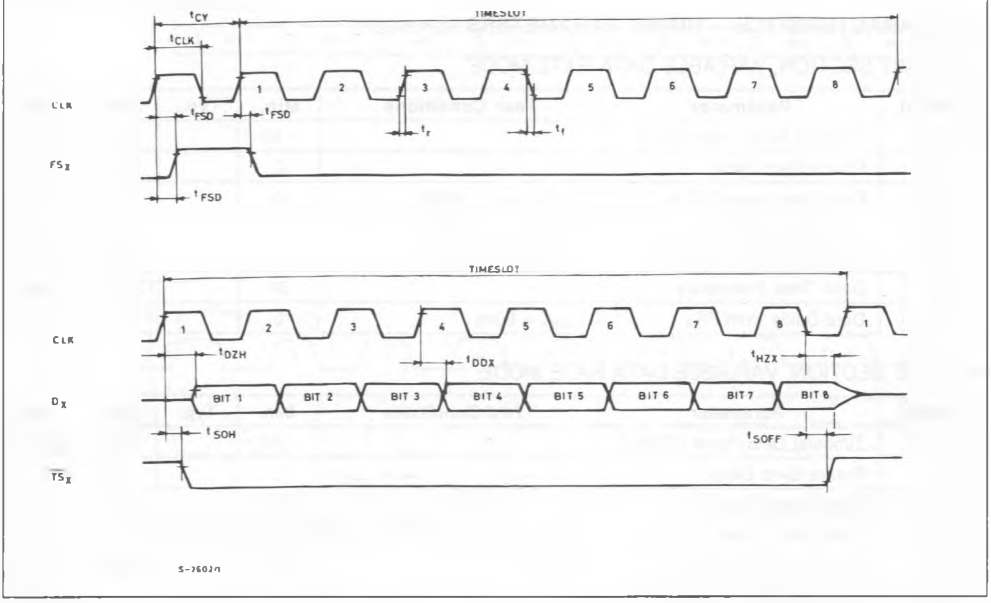
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync Delay		0		120	ns

Notes : 1. Devices are available which operate at data rates up to 4.096MHz ; the minimum data clock pulse width for these devices is 110ns.
2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

WAVEFORMS

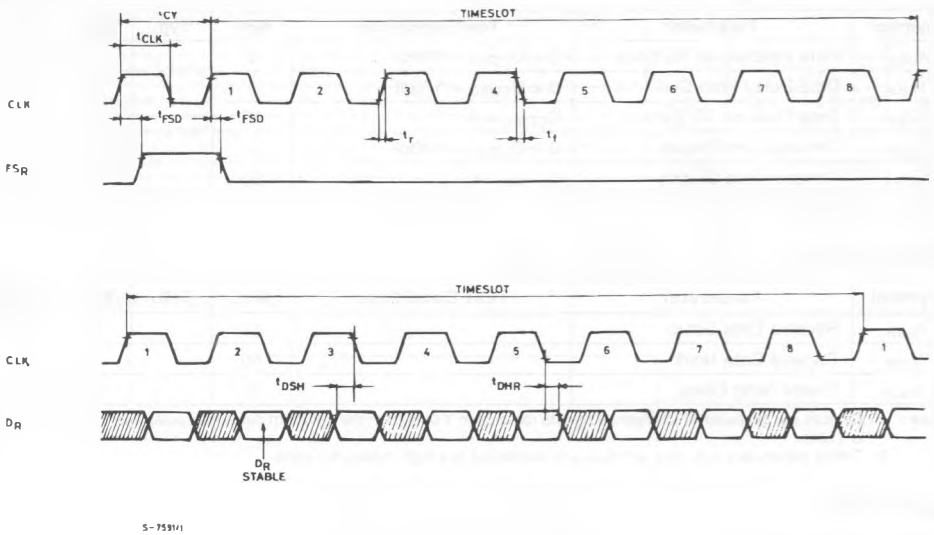
FIXED DATA RATE TIMING.

TRANSMIT TIMING



Note : All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

RECEIVE TIMING



Note : All timing parameters referenced to V_{IH} and V_{IL}.

AC CHARACTERISITCS - TIMING PARAMETERS (continued)

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDX}	Timeslot Delay from $DCLK_X$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DDX}	Data Delay from $DCLK_X$	$0 < C_{LOAD} < 100pF$	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100pF$	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100pF$	0		80	ns
f_{DX}	Data Clock Frequency		64		2048[2]	kHz
t_{DFSX}	Data Delay from FS_X	t_{TSDX} = 80ns	0		140	ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDR}	Timeslot Delay from $DCLK_R$		– 80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DSR}	Data Setup Time		10			ns
t_{DHR}	Data Hold Time		60			ns
f_{DR}	Data Clock Frequency		64		2048[2]	kHz
t_{SER}	Timeslot End Receive Time		0			ns

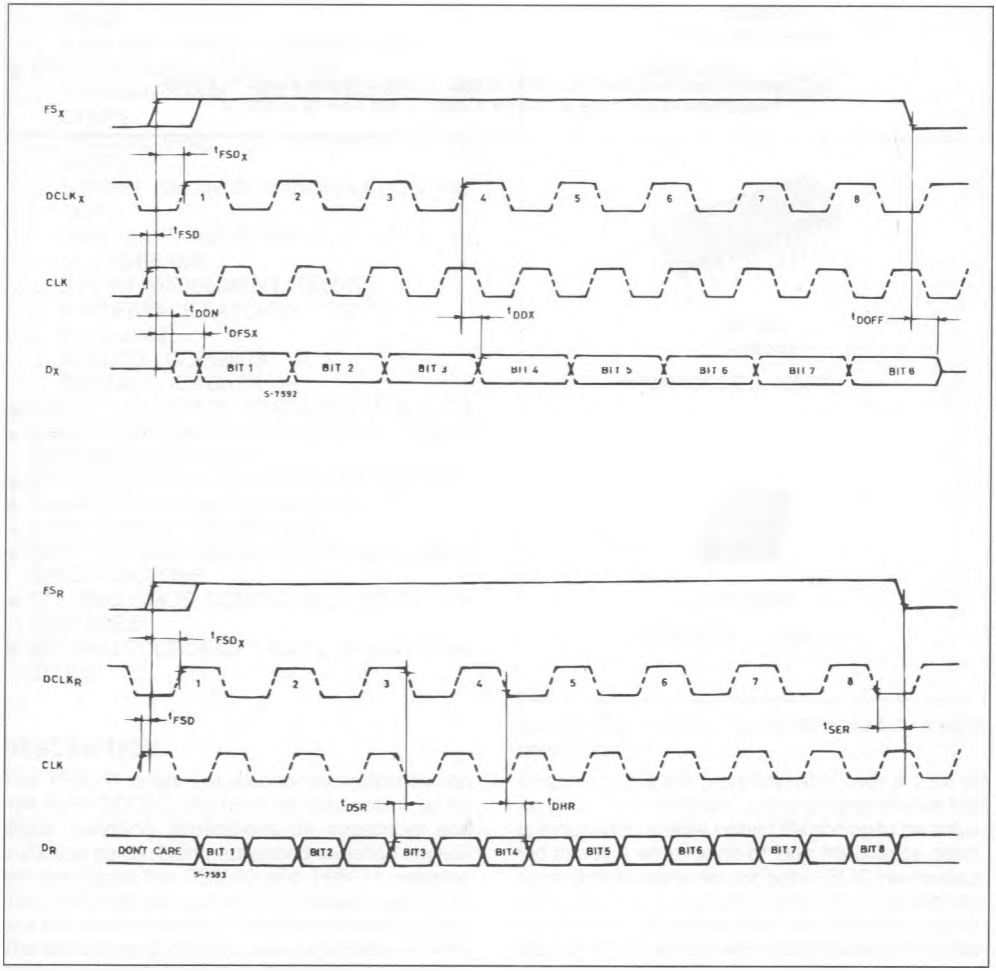
AC CHARACTERISTICS - TIMING PARAMETERS (continued)

64KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{FSLX}	Transmit Frame Sync Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync Minimum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width				10	µs

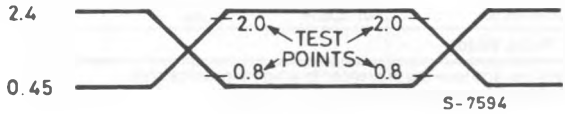
Notes : 1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. Device are available which operate at data rates up to 4.096MHz.

VARIABLE DATA RATE TIMING



Note : All timing parameters referenced to V_{IH} and V_{IL} except t_{DON} and t_{OFF} which reference a high impedance state.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0" timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".