SGS-THOMSON MICROELECTRONICS

# M5116

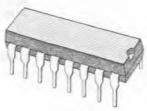
## μ-255 LAW COMPANDING CODEC

- ±5-VOLT POWER SUPPLIES
- LOW POWER DISSIPATION - 30mW (Typ)
- FOLLOWS THE μ-255 COMPANDING LAW
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TRIMMING
- SINGLE 16-PIN PACKAGE
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64kb/s-2.1Mb/s AT 8kHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDING PINS REDUCE SYSTEM NOISE PROBLEMS

### DESCRIPTION

The M5116 is a monolithic CMOS companding CODEC which contains two sections : (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

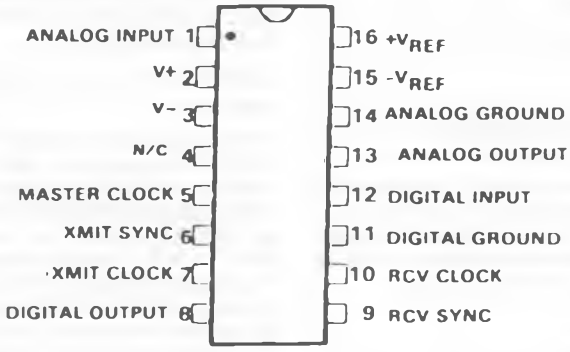
These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.



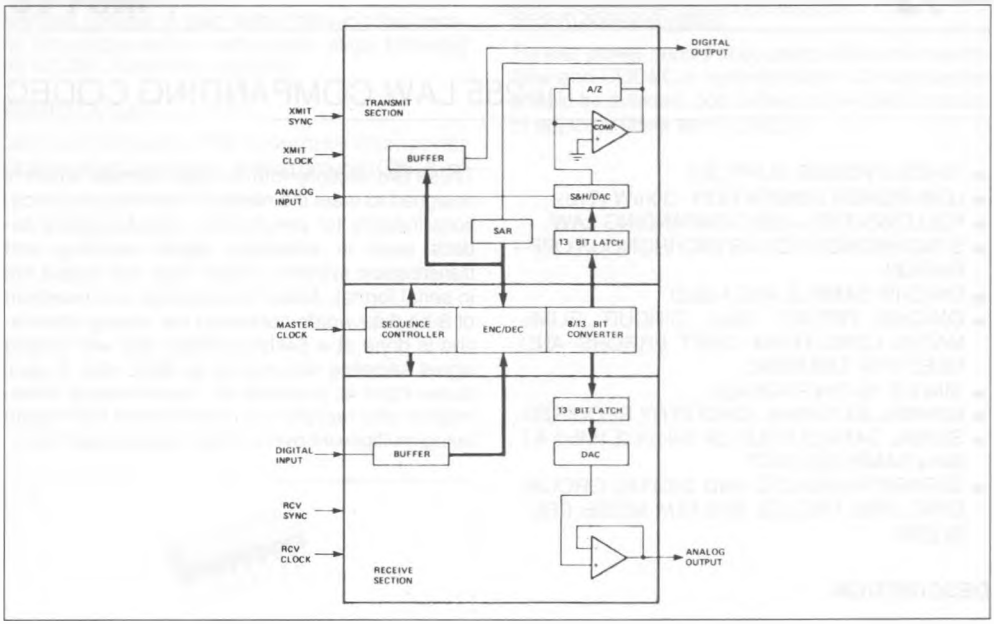
**DIP-16**

**ORDER CODES :** M5116N (Plastic)
M5116J (Ceramic)

### PIN CONNECTION (top view)

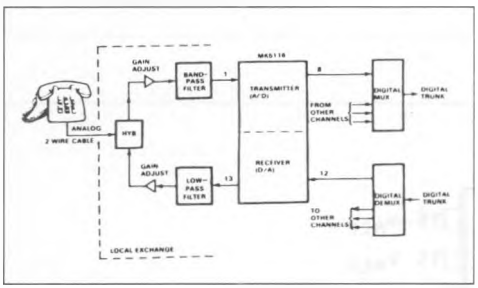


## BLOCK DIAGRAM




## FUNCTIONAL DESCRIPTION

PCM SYSTEM BLOCK DIAGRAM




POSITIVE AND NEGATIVE REFERENCE VOLTAGES (+ $V_{REF}$ and - $V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the M5116. + $V_{REF}$ and - $V_{REF}$ must maintain 100ppM/C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (refer to figure 1). The analog input must remain between + $V_{REF}$ and - $V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in figure 6.

MASTER CLOCK : Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV CLOCK, XMIT SYNC, or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (refer to figure 7 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated, and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC may remain high longer than 8 XMIT CLOCK cycles, but must go low for at least 1 master clock before the transmission of the next digital word (refer to figure 9).

XMIT CLOCK, Pin 7 (refer to figure 7 for the Timing Diagram)

The on-chip 8-bit output shift register of the M5116 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (refer to the figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RVC SYNC, Pin 9 (refer to figure 8 for the Timing Diagram)

This input is synchronized with RCV CLOCK, and serial data is clocked in by RCV CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV CLOCK periods. The conversion from digital to analog starts after the negative edge of the RCV SYNC pulse (refer to figure 1). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (refer to figure 10).

RCV CLOCK, Pin 10 (refer to figure 8 for Timing Diagram)

The on-chip 8-bit shift register for the M5116 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (refer to figure 2). This set up time, $t_{RDS}$, allows the data to be transferred into the MASTER of a master-slave flip-flop. A hold time, $t_{RDH}$, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

**Figure 1 :** A/D, D/A Conversion Timing.

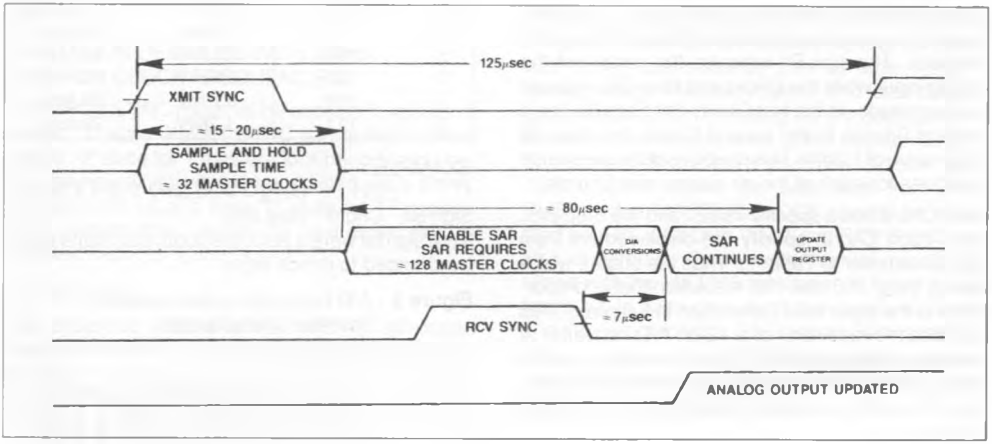
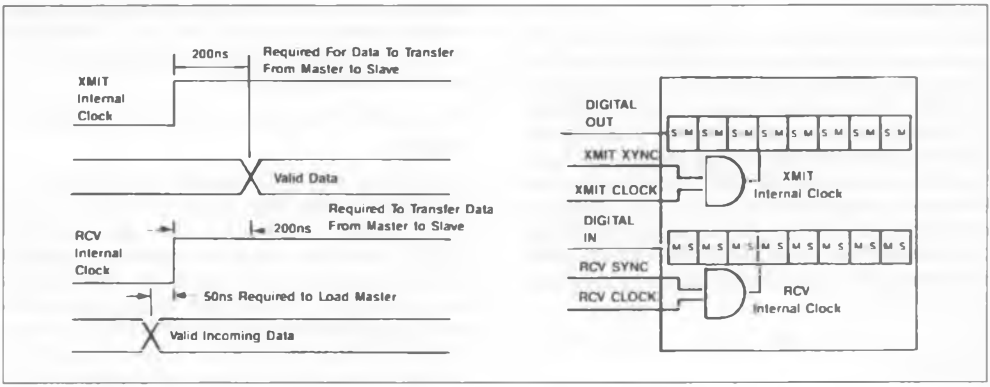


**Figure 2 :** Data Input/Output Timing.




DIGITAL OUTPUT, Pin 8

The M5116 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value ; and the Step Bits, 16 in each Chord, specify the displacement from that value (refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in figure 3.

DIGITAL INPUT, Pin 12

The M5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV CLOCK. The timing diagram is shown in figure 11. When RCV SYNC goes high, the MK5116 uses RCV CLOCK to clock the serial data into its input register. RCV SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (μ-Law Decoder) is shown in figure 4.

## DIGITAL OUTPUT CODE μ-LAW

**Table 1.**

| | Chord Code | Chord Value | Step Value |
|---|---|---|---|
| 1. | 000 | 0.0mV | 0.163mV |
| 2. | 001 | 10.11mV | 1.226mV |
| 3. | 010 | 30.3mV | 2.45mV |
| 4. | 011 | 70.8mV | 4.90mV |
| 5. | 100 | 151.7mV | 9.81mV |
| 6. | 101 | 313mV | 19.61mV |
| 7. | 110 | 637mV | 39.2mV |
| 8. | 111 | 1.284V | 78.4mV |

EXAMPLE :

1 011 0010 = + 70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

**Figure 3 :** A/D Converter (μ-law encoder) Transfer Characteristic.

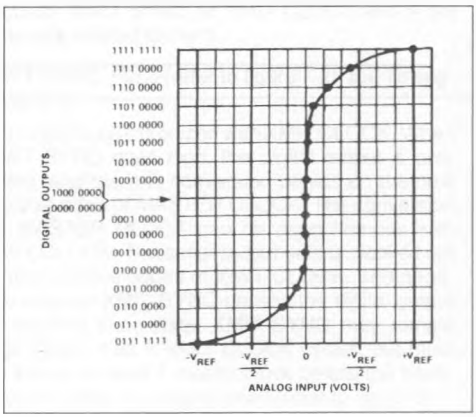
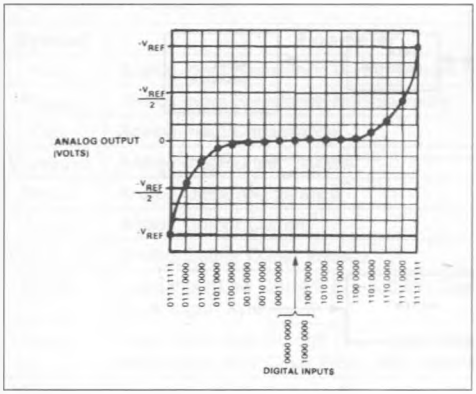


**Figure 4** : D/A Converter (μ-law encoder) Transfer Characteristic.




ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV CLOCK FREQUENCIES

XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMINT SYNC is required to be at a logic "0" state for 1 master-clock period (min.) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master-clock periods (min.) before the next digital word is received (refer to figures 9 and 10).

OFFSET NULL

The offset-null feature of the MK5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset-adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because the resultant DC error ($V_{OFFSET0}$) will have no effect, since the output is intended to be AC-coupled to the external filter. The sign is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

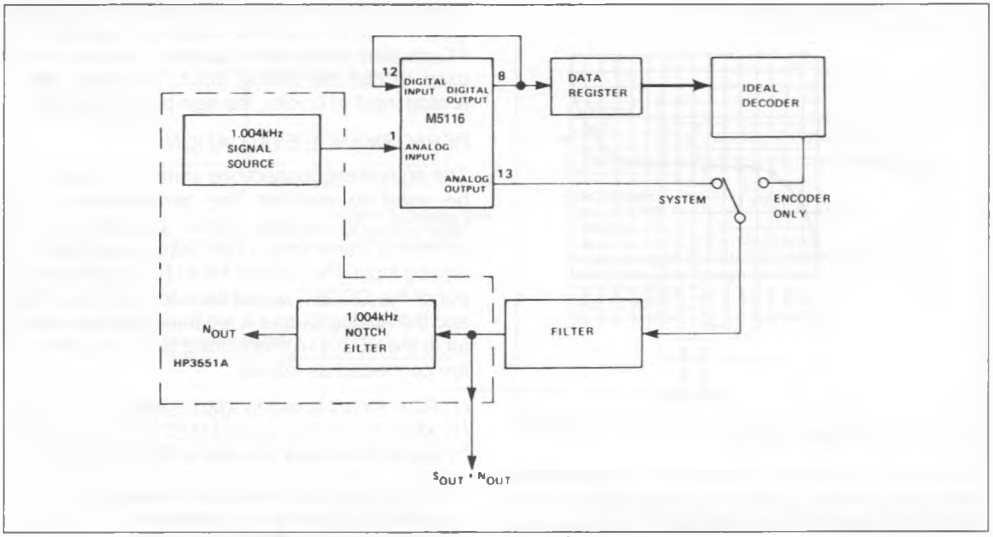
The equipment connections shown in figure 5 can be used to evaluate the performance of the MK5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5116. The Digital Output of the CODEC is tied back to the Digital Input, and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5116 are connected as follows :

(1) RCV SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV CLOCK.

The following timing signals are required :
(1) MASTER CLOCK = 1.536MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of figure 5 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5116 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK, and MASTER CLOCK should be separated from RCV CLOCK. XMIT and RCV SYNCS are also separated. Some experimental results obtained with the MK5116 are shown in figure 11 and figure 12. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5116 exceeds the requirements for Signal-to-Distortion ratio (figure 11) and for Gain Tracking (figure 12).

**Figure 5 :** System Characteristics Test Configuration.




**Note :** The ideal decoder consist of a digital decompander and a 13-bit precision DAC.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Value | Unit |
|---|---|---|
| DC Supply Voltage, V+ | + 6 | V |
| DC Supply Voltage, V– | – 6 | V |
| Ambient Operating Temperature, $T_A$ | 0 to 70 | °C |
| Storage Temperature | – 55 to + 125 | °C |
| Package Dissipation at 25 °C (derated 9mW/°C when soldered into PCB) | 500 | mW |
| Digital Input | $-0.5V \leq V_{IN} \leq V+$ | |
| Analog Input | $V- \leq V_{IN} \leq V+$ | |
| $+ V_{REF}$ | $-0.5V \leq +V_{REF} \leq V+$ | |
| $- V_{REF}$ | $V- \leq -V_{REF} \leq +0.5$ | V |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damages to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

## ELECTRICAL OPERATING CHARACTERISTICS

### POWER SUPPLY REQUIREMENTS

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| V+ | Positive Supply Voltage | 4.75 | 5.0 | 5.25 | V | |
| V– | Negative Supply Voltage | – 5.25 | – 5.0 | – 4.75 | V | |
| $+ V_{REF}$ | Positive Reference Voltage | 2.375 | 2.5 | 2.625 | V | 1 |
| $- V_{REF}$ | Negative Reference Voltage | – 2.625 | – 2.5 | – 2.375 | V | 1 |

**TEST CONDITIONS** : V+ = 5.0V, V– = – 5.0V, + $V_{REF}$ = 2.5V, – $V_{REF}$ = – 2.5V, $T_A$ = 0°C to 70°C

DC CHARACTERISTICS

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{INAS}$ | Analog Input Resistance During Sampling | | 2 | | kΩ | 2 |
| $R_{INANS}$ | Analog Input Resistance Non-Sampling | | 100 | | MΩ | |
| $C_{INA}$ | Analog Input Capacitance | | 150 | 250 | pF | 2 |
| $V_{OFFSET\ 1}$ | Analog Input Offset Voltage | | ± 1 | ± 8 | mV | 2 |
| $R_{OUTA}$ | Analog Output Resistance | | 1 | 10 | Ω | |
| $I_{OUTA}$ | Analog Output Current | 0.25 | 0.5 | | mA | |
| $V_{OFFSET\ 0}$ | Analog Output Offset Voltage | | + 20 | ± 850 | mV | |
| $I_{INLOW}$ | Logic Input Low Current ($V_{IN}$ = 0.8V) Digital Input, Clock Input, Sync Input | | ± 0.1 | ± 10 | µA | 3 |
| $I_{INHIGH}$ | Logic Input High Current ($V_{IN}$ = 2.4V) Digital Input, Master and RCV Clock Input, RCV Sync Input | | ± 0.1 | ± 10 | µA | 3 |
| $I_{INHIGH_X}$ | Logic Input High Current ($V_{IN}$ = 2.4V) TX Clock, TX Sync | | – .25 | – 0.8 | mA | 3 |
| $C_{DO}$ | Digital Output Capacitance | | 8 | 12 | pF | |
| $I_{DOL}$ | Digital Output Leakage Current | | ± 0.1 | ± 10 | µA | |
| $V_{OUTLOW}$ | Digital Output Low Voltage | | | 0.4 | V | 4 |
| $V_{OUTHIGH}$ | Digital Output High Voltage | 3.9 | | | V | 4 |
| I+ | Positive Supply Current | | 4 | 10 | mA | 5 |
| I– | Negative Supply Current | | 2 | 6 | mA | 5 |
| $I_{REF+}$ | Positive Reference Current | | 4 | 20 | µA | |
| $I_{REF-}$ | Negative Reference Current | | 4 | 20 | µA | |

**AC CHARACTERISTICS** (refer to figure 10 and figure 11)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_M$ | Master Clock Frequency | 1.5 | 1.544 | 2.1 | MHz | |
| $F_R$, $F_X$ | XMIT, RCV Clock Frequency | 0.064 | 1.544 | 2.1 | MHz | |
| $PW_{CLK}$ | Clock Pulse Width (MASTER, XMIT, RCV) | 200 | | | ns | |
| $t_{RC}$, $t_{FC}$ | Clock Rise, Fall Time (MASTER, XMIT, RCV) | | | 25% of $PW_{CLK}$ | ns | |
| $t_{RS}$, $t_{FS}$ | Sync Rise, Fall Time (XMIT, RCV) | | | 25% of $PW_{CLK}$ | ns | |
| $t_{DIR}$, $t_{DIF}$ | Data Input Rise, Fall Time | | | 25% of $PW_{CLK}$ | ns | |
| $t_{WSX}$, $t_{WSR}$ | Sync Pulse Width (XMIT RCV) | | $\frac{8}{F_X(F_R)}$ | | µs | |

## DC CHARACTERISTICS (refer to figure 7 and figure 8)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{PS}$ | Sync Pulse Perlod (XMIT. RCV) | | 125 | | µs | |
| $t_{XCS}$ | XMIT Clock-to-XMIT Sync Delay | 50% of $t_{FC}$ ($t_{RS}$) | | | ns | 6 |
| $t_{XCSN}$ | XMIT Clock-to-XMIT Sync (negative edge) Delay | 200 | | | ns | |
| $t_{XSS}$ | XMIT Sync Set-Up Time | 200 | | | ns | |
| $t_{XDD}$ | XMIT Data Delay | 0 | | 200 | ns | 4 |
| $t_{XDP}$ | XMIT Data Present | 0 | | 200 | ns | 4 |
| $t_{XDT}$ | XMIT Data Three State | | | 150 | ns | 4 |
| $t_{DOF}$ | Digital Output Fall Time | | 50 | 100 | ns | 4 |
| $t_{DOR}$ | Digital Output Rise Time | | 50 | 100 | ns | 4 |
| $t_{SRC}$ | RVC Sync-to-RCV Clock Delay | 50% of $t_{RC}$ ($t_{FS}$) | | | ns | 6 |
| $t_{RDS}$ | RCV Data Set-up Time | 50 | | | ns | 7 |
| $t_{DRH}$ | RCV Data Hold Time | 200 | | | ns | 7 |
| $t_{RCS}$ | RCV Clock-to-RCV Sync Delay | 200 | | | ns | |
| $t_{RSS}$ | RCV Sync Set-up Time | 200 | | | ns | 7 |
| $t_{SAO}$ | RCV Sync-to-Analog Output Delay | | 7 | | µs | |
| SLEW+ | Analog Output Positive Slew Rate | | 1 | | V/µs | |
| SLEW– | Analog Output Negative Slew Rate | | 1 | | V/µs | |
| DROOP | Analog Output Droop Rate | | 25 | | µV/µs | |

## AC CHARACTERISTICS (refer to figures 11 and 12)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $GT_X$ | Gain Tracking Transmit | Analog Input = + 3 to – 37dBm0<br>Analog Input = – 37 to – 50dBm0<br>Analog Input = – 50 to – 55dBm0<br>Relative to 0 dBm0 | – .2<br>– .4<br>– 1.25 | 0.0<br>± 0.1<br>± 0.2 | + .2<br>+ .4<br>+ 1.25 | dB<br>dB<br>dB |
| $GT_R$ | Gain Tracking Receive | Input Level = + 3 to – 37dBm0<br>Input Level = – 37 to – 50dBm0<br>Input Level = – 50 to – 55dBm0<br>Relative to 0 dBm0 | – .2<br>– .4<br>– 1.25 | 0.0<br>± 0.1<br>± 0.2 | + .2<br>+ .4<br>+ 1.25 | dB<br>dB<br>dB |
| $GT_{E\ E}$ | Gain Tracking End to End | Analog Input = + 3 to – 37dBm0<br>Analog Input = – 37 to – 50dBm0<br>Analog Input = – 50 to – 55dBm0<br>Relative to 0 dBm0 | – .4<br>– .8<br>– 2.50 | 0.0<br>± 0.1<br>± 0.2 | + .4<br>+ .8<br>+ 2.50 | dB<br>dB<br>dB |
| $SD_X$ | Signal to Distortion Transmit | Analog Input = 0 to – 30dBm0<br>Analog Input = – 40dBm0<br>Analog Input = – 45dBm0 | 37<br>31<br>26 | | | dB<br>dB<br>dB |
| $SD_R$ | Signal to Distortion Receive | Input Level = 0 to – 30dBm0<br>Input Level = – 40dBm0<br>Input Level = – 45dBm0 | 37<br>31<br>26 | | | dB<br>dB<br>dB |

**AC CHARACTERISTICS** (refer to figures 11 and 12)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $SD_{E-E}$ | Signal to Distortion End to End | Analog Input = 0 to – 30dBm0<br>Analog Input = – 40 dBm0<br>Analog Input = – 45 dBm0 | 35<br>29<br>24 | | | dB<br>dB<br>dB |
| $N_X$ | Idle Channel Noise Transmit | Analog Input = 0Volts | | | 17 | dBnc0 |
| $N_R$ | Idle Channel Noise Receive | Digital Input = 0 Code | | | 0 | dBnc0 |
| $N_{E-E}$ | Idle Channel Noise End to End | Analog Input = 0Volts<br>Digital Output to Digital Input | | | 18 | dBncO |
| $CT_{RX}$ | Crosstalk Receive to Transmit | Analog In = – 50dBm0 at 2600$H_Z$<br>Digital Input = 0dBm0 at 1008$H_Z$ digital | | | – 80 | dB |
| $CT_{XR}$ | Crosstalk Transmit to Receive | Analog In = 0dBm0 at 1008$H_Z$<br>Digital Input = 0 Code | | | – 80 | dB |
| TLP | Transmit Level Point | 600Ω | | + 4 | | dB |

**Notes :**
1. + $V_{REF}$ and - $V_{REF}$ must be matched within ±1 % in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor ; therefore, the designer should avoid excessive source impedance. Input-related device characteristics are derived using the Recommended Analog Input Circuit. See figure 6.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with $I_{OH}$ = 100µA, $I_{OL}$ = 500µA.
5. Results in 30mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

**Figure 6 :** Recommended Analog Input Circuit.

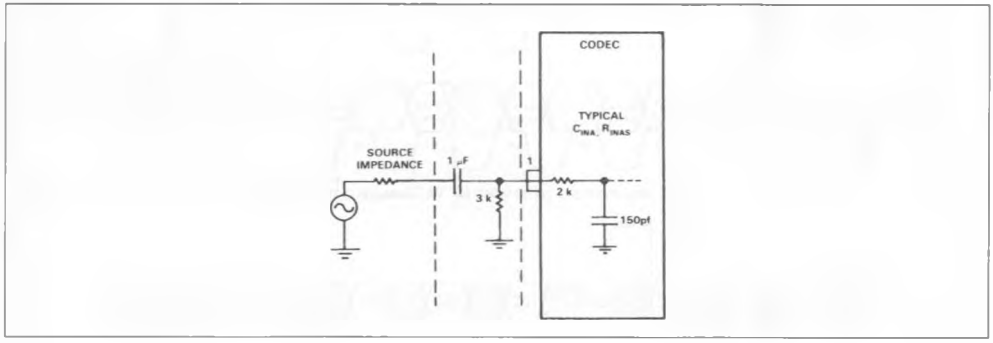
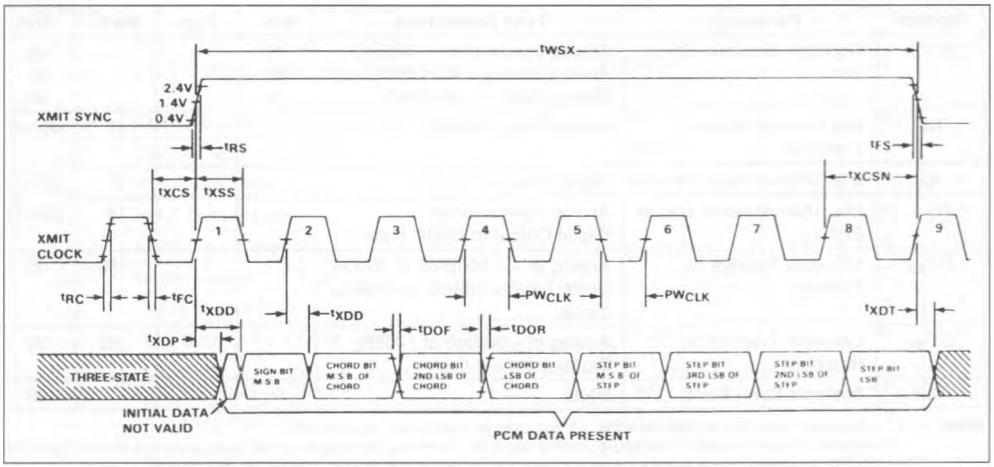
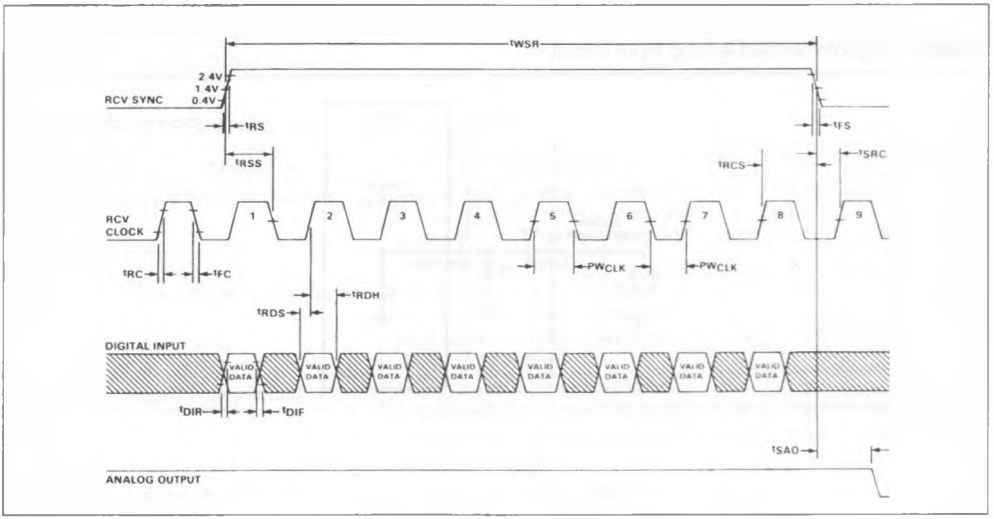


**Figure 7 :** Transmitter Section Timing.



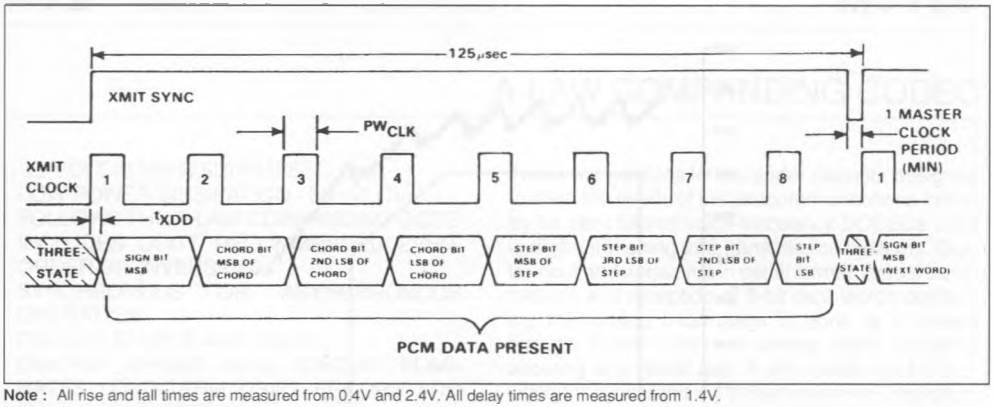

**Note :** All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

**Figure 8 :** Receiver Section Timing.



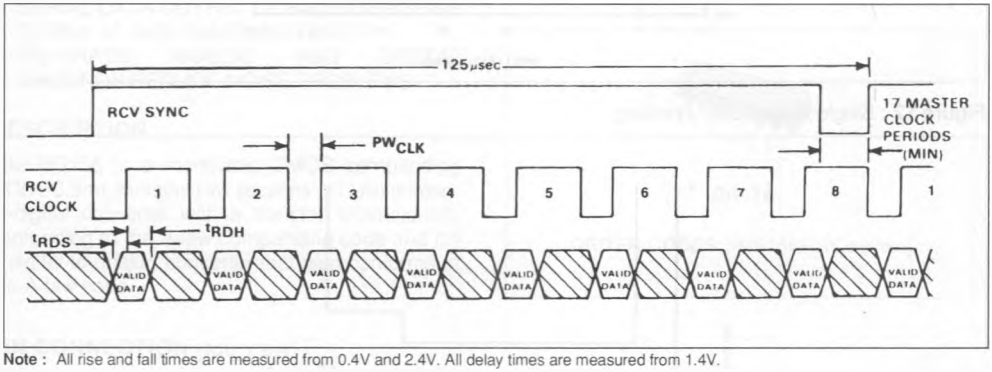

**Note :** All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V

**Figure 9 :** 64kHz Operation, Transmitter Section Timing.




**Note :** All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

**Figure 10 :** 64kHz Operation, Receiver Section Timing.




**Note :** All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

**Figure 11 :** Single-ended Signal to Distortion.

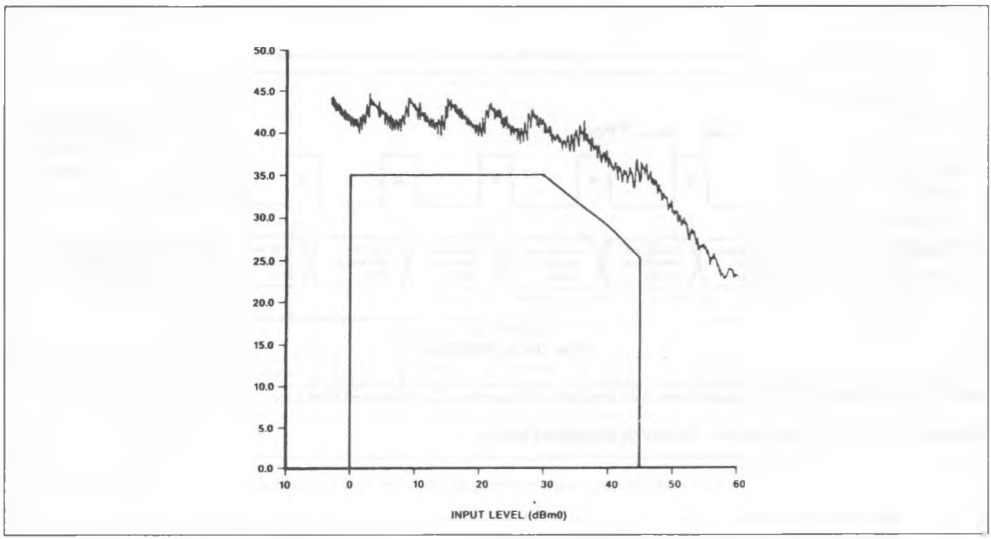



**Figure 12 :** Single-ended Gain Tracking.