MOS INTEGRATED CIRCUIT

M 4015

PRELIMINARY DATA

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

- POWER SUPPLY V_{DD}= 12V, V_{CC}= 5V, V_{BB}= -5V (ALL WITH ± 10% TOLERANCE EXCEPT V_{DD} ± 5)
- ALL INPUTS ARE LOW CAPACITANCE AND TTL COMPATIBLE
- INPUT LATCHES FOR ADDRESSES, CHIP SELECT AND DATA IN
- INPUTS PROTECTED AGAINST STATIC CHARGE
- THREE-STATE TTL COMPATIBLE OUTPUT
- OUTPUT DATA LATCHED AND VALID INTO NEXT CYCLE
- ECL. COMPATIBLE ON V_{BB} POWER SUPPLY (-5.7V)
- LOW POWER CONSUMPTION: ACTIVE POWER UNDER 470 mW
  STANDBY POWER UNDER 27 mW
- ORGANIZATION 4096 x 1 BIT IN 16-PIN STD PACKAGE
- FUNCTIONAL AND PIN COMPATIBLE WITH MK4027
- ACCESS TIME: TYPE M4015 250 ns

The M4015 is a 4096 word by 1 bit dynamic N-channel silicon gate MOS RAM. The M4015 uses a single transistor cell utilizing a dynamic storage technique and dynamic control circuitry with low power dissipation. A unique multiplexing and latching technique for the address inputs permits the M4015 to be mounted in a standard 16-pin package. The M4015 incorporates several flexible operating modes. In addition to the usual read and write cycles, read modify write, page mode and RAS-only refresh cycles are available with the M4015. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA). The device is available in 16-lead dual in-line plastic or ceramic package (metal-seal), and ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS*

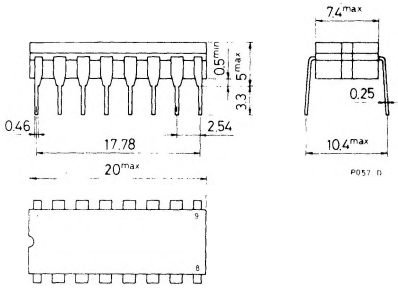
	Voltage on any pin relative to V_{BB}	-0.5 to +20	V
	Voltage on V_{DD}, V_{CC} relative to V_{SS}	-1 to +15	V
	V_{BB}-V_{SS} (V_{DD}-$V_{SS} > 0$)	0	V
T_{op}	Operating temperature	0 to +55	°C
T_{stg}	Storage temperature for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
I_o	Short circuit output current	50	mA
P_{tot}	Total power dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

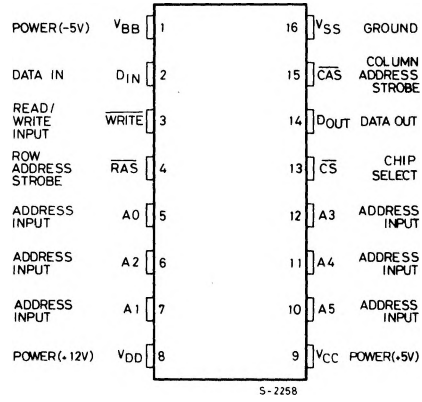
ORDERING NUMBER: M4015 F1 for dual in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

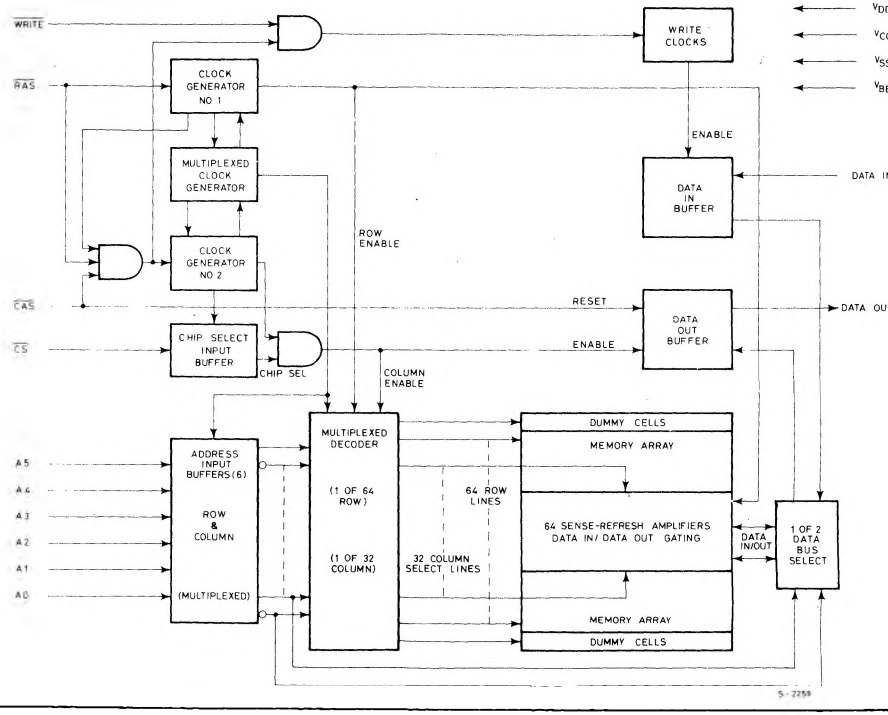
Dual in-line ceramic package frit-seal
for M4015 F1



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb} = 0 to 55°C)[4]

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	11.4	12	12.6	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2, 3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	-4.5	-5	-5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3		7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3		7	V	2
V_{IL}	Input low voltage, all inputs	-1		0.65	V	2

DC ELECTRICAL CHARACTERISTICS[1] (T_{amb} = 0 to 55°C)[4] (V_{DD} = 12V ± 5% , V_{CC} = 5V ± 10% , V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
I_{DD1}	Average V_{DD} power supply current			35	mA	5
I_{DD2}	Standby V_{DD} power supply current		3		mA	8
I_{DD3}	Average V_{DD} power supply current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} power supply current				mA	6
I_{BB}	Average V_{BB} power supply current			150	µA	
$I_{I(L)}$	Input leakage current (any input)			10	µA	7
$I_{O(L)}$	Output leakage current			10	µA	8, 9
V_{OH}	Output high voltage (I_{SOURCE} = -5 mA)	2.4			V	
V_{OL}	Output low voltage (I_{SINK} = 3.2 mA)			0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[1,10,15]

(T_{amb} = 0 to 55°C)[4], (V_{DD} = 12V ± 5% , V_{CC} = 5V ± 10% , V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

Parameter		M4015			Unit	Notes
		Min.	Typ.	Max.		
t_{RC}	Random read or write cycle time	380			ns	
t_{RWC}	Read write cycle time	395			ns	
t_{RMW}	Read modify write cycle time	470			ns	
t_{RAC}	Access time from row address strobe			250	ns	11-13
t_{CAC}	Access time from column address strobe			165	ns	12-13
t_{OFF}	Output buffer turn-off delay			60	ns	
t_{RP}	Row address strobe precharge time	120			ns	
t_{RAS}	Row address strobe pulse width	250		4000	ns	
t_{RSH}	Row address strobe hold time	165			ns	
t_{CAS}	Column address strobe pulse width	165			ns	
t_{CSH}	Column address strobe hold time	250			ns	
t_{RCD}	Row to column strobe delay	35		85	ns	14
t_{ASR}	Row address set-up time	0			ns	
t_{RAH}	Row address hold time	35			ns	
t_{ASC}	Column address set-up time	0			ns	
t_{CAH}	Column address hold time	75			ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	160			ns	
t_{CSC}	Chip select set-up time	0			ns	
t_{CH}	Chip select hold time	75			ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	160			ns	
t_T	Transition time (rise and fall)	5		50	ns	15
t_{RCS}	Read command set-up time	0			ns	
t_{RCH}	Read command hold time	0			ns	
t_{WCH}	Write command hold time	75			ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	160			ns	
t_{WP}	Write command pulse width	75			ns	
t_{RWL}	Write command to row strobe lead time	100			ns	
t_{CWL}	Write command to column strobe lead time	100			ns	
t_{DS}	Data in set-up time	0			ns	16
t_{DH}	Data in hold-time	75			ns	16

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (cont.)

Parameter		M4015			Unit	Notes
		Min.	Typ.	Max.		
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	160			ns	
t_{CRP}	Column to row strobe precharge time	0			ns	
t_{CP}	Column precharge time	110			ns	
t_{RFSH}	Refresh period			1	ms	
t_{WCS}	Write command set-up time	0			ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	90			ns	17
t_{RWD}	RAS to WRITE delay	175			ns	17
t_{DOH}	Data out hold time	4			µs	

CAPACITANCES (T_{amb} = 0 to 55°C, V_{DD} = 12V ± 5% ; V_{SS} = 0V; V_{BB} = -5.7 to -4.5V)

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
C_{I1}	Input capacitance (A_0-A_5), D_{IN}, $\overline{CS}$		4	5	pF	18
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		8	10	pF	18
C_O	Output capacitance (D_{OUT})		5	7	pF	8-18

1. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2. All voltage referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. T_{amb} is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).
6. I_{CC} depends on output loading. The V_{CC} supply is connected to the output buffer only.
7. All device pins at 0 volts except V_{BB} which is at -5V and the pin under test which is at +10V.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{out} \leq +10V$.
10. AC measurements assume t_T = 5 ns.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
13. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
18. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts.