SGS-THOMSON MICROELECTRONICS

M3493

CMOS 12 X 8 CROSSPOINT WITH CONTROL MEMORY

- LOW ON RESISTANCE (typ. 40 Ω at V_{DD} = 10 V)
- INTERNAL CONTROL LATCHES
- ANALOG SIGNAL SWING CAPABILITY EQUAL TO POWER SUPPLY VOLTAGE APPLIED
- LESS THAN 1 % TOTAL DISTORT. AT 0 dBm
- LESS THAN – 95 dB CROSS-TALK AT 1 KHz 1 V_{PP}
- VERY LOW POWER CONSUMPTION
- PIN-TO-PIN COMPATIBLE WITH M093

DIP40
(Plastic)

PLCC44

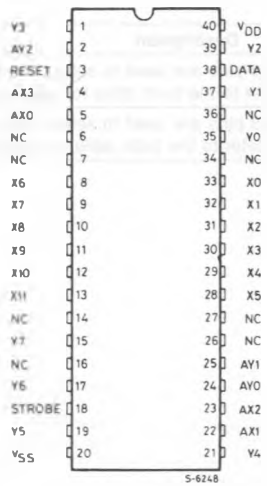
ORDER CODES : M3493B1 (DIP40)
M3493C1 (PLCC44)

DESCRIPTION

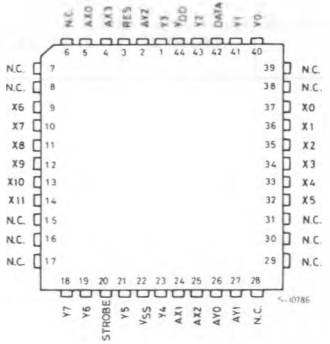
The M3493 contains a 12 x 8 array of crosspoint together with a 7 to 96 line decoder and latch circuits. Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one.

M3493 is available in 40 lead dual in-line plastic, or 44 lead plastic chip carrier packages.

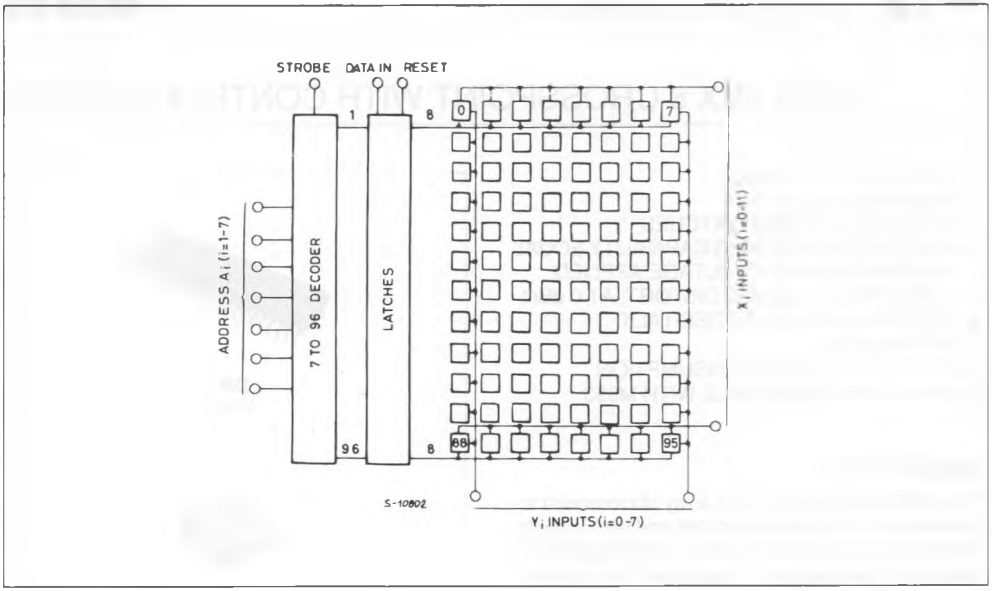
PIN CONNECTIONS (top view)



CHIP CARRIER



BLOCK DIAGRAM



INPUT/OUTPUT DESCRIPTION

POWER

I/O	Symbol	Pin	Description
I	V_{DD}	40	Positive Power Supply
I	V_{SS}	20	Negative Power Supply

ADDRESS

I/O	Symbol	Pin	Description
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 16 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.

CONTROL

I/O	Symbol	Pin	Description
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 128 switches. The states of the above control lines are irrelevant. This pin is active high.

DATA

I/O	Symbol	Pin	Description
I/O	X0-X11	8-13, 28-33	Analog Input/Outputs. These pins are connected to the Y0-Y7 pins in according to the truth table.
I/O	Y0-Y7	1,15,17,19,21 35,37,39	Analog Input/Outputs. These pins are connected to the X0-X15 pins in according to the truth table.

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	No connection
1	1	1	0	0	0	0	No connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	No connection
1	1	1	1	0	0	0	No connection
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	0	X11 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	0	X11 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	0	X11 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	0	1	X11 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	1	X11 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	1	X11 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	1	X11 - Y7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 14	V
V_{IN}	Input Voltage Range	– 0.5 to V_{DD} + 0.5	V
P_{tot}	Power Dissipation	1	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 50 to 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	10	V
T_{op}	Operating Temperature	0 to 70	°C
V_{IN}	(logic signal)	0 to V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C, V_{DD} = 10 V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	Reset = V_{DD}			1	mA

CROSSPOINT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	On Resistance	V_{IDC} = 4.75 V V_{ODC} = 4.5 V (see fig. 1)		60	100	Ω
	On Resistance Variation			6	10	Ω
	Off Leakage*	All switches off V_{OS} = V_{IS} = 0 to V_{DD}			± 3	µA

CONTROLS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}					0.8	V
V_{IH}			2.4			V
	Input Leakage*	V_{IN} = 0 to V_{DD}			± 3	µA

* The device is guaranteed with such limits up to 70°C. At 25°C these limits become ± 100nA.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, C_L = 50 pF all input square wave rise and fall times = 10 ns, V_{DD} = 10 V)

CROSSPOINTS

Symbol	Parameter	Test Conditions				Value			Unit
		Note	f_q (KHz)	R_h (KΩ)	V_{Is} (Vpp)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay Time (switch ON) Signal Input to Output	Fig. 2		1	2		30	100	ns
	Frequency Response (any switch ON) 20 log (V_{OS}/V_{IS}) = – 3 dB	C_L = 3 pF		0.081	2		50		MHz
	Sine Wave Distortion		1	0.6	8			1	%
	Feed Through (any switches OFF)	Fig. 3	10	1	2	– 80			dB
	Frequency For Signal Crosstalk Attenuation of 40 dB Attenuation of 110 dB	Fig. 4		1	2	1 5			MHz KHz
C	Capacitance Xn to Ground						15		pF
	V_n to Ground		1000		0.1		15		
	Feed Through						0.4		
C	Capacitance Logic Input to Ground		1000		0.1		5		pF

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

CONTROLS

Symbol	Parameter	Test Conditions	See Fig.	Value			Unit
		V_{DD} = 10 V		Min.	Typ.	Max.	
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-ON to high level)	R_L = 1 KΩ C_L = 50 pF t_r, t_f = 10 ns	5		150	200	ns
t_{PZH}	Data-in to Output (turn-ON to high level)		6		150	200	ns
t_{PAN}	Address to Output (turn-ON to high level)		7		150	200	ns
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-OFF)		5		150	200	ns
t_{PZL}	Data-in to Output (turn-ON to low level)		6		150	200	ns
t_{PAF}	Address to Output (turn-OFF)		7		150	200	ns
t_S	Set-UP Time Data-in to Strobe		5, 10	20			ns
t_H	Hold time Data-in to Strobe		5, 10	120			ns
t_o	Switching Frequency				1		MHz
t_W	Strobe Pulse Width		10	100			ns
t_{WR}	Reset Pulse Width		9	150			ns
t_{PHZ}	Reset Turn-OFF to Output Delay		9		150	200	ns
t_{AS}	Address Set-UP Time Address to Strobe		10	20			ns
t_{AH}	Address Hold Time Address to Strobe		10	20			ns
	Control Crosstalk Data-in, Address, or Strobe to Output	Square Wave V_{IN} = 3 V Input t_r, t_f = 10 ns R_L = 10 kΩ	8		75		mV

TEST CIRCUITS

Figure 1 : R_{ON} Measurement.

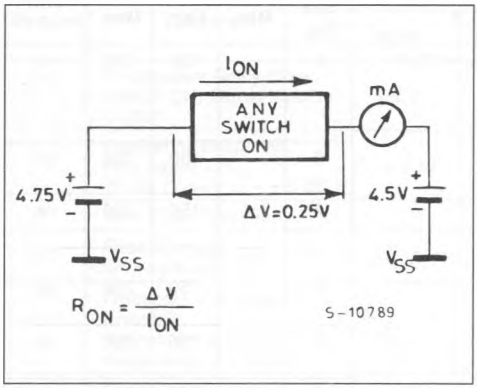


Figure 2 : Propagation Delay Time and Waveforms (signal input to signal output switch ON).

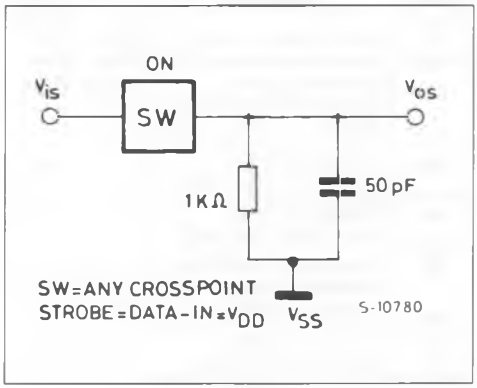
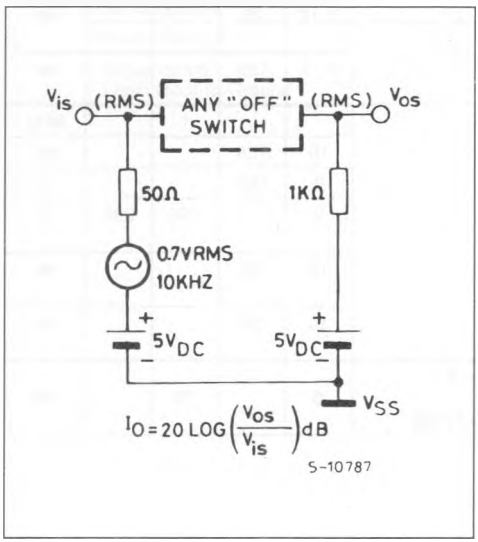


Figure 3 : Off Isolation Measurement (Feed through).



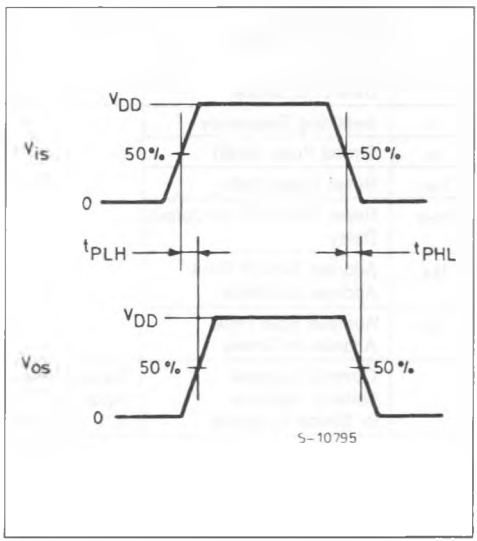


Figure 4 : Crosstalk Measurements.

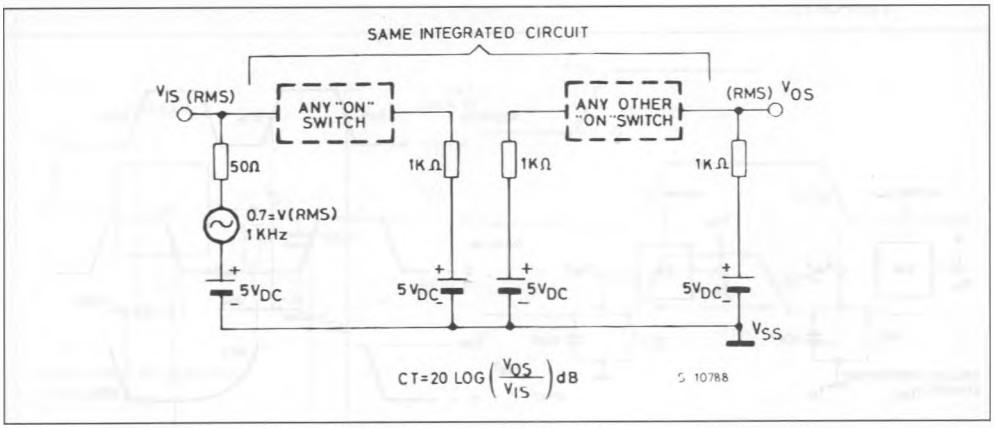


Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output switch Turn-ON or Turn-OFF).

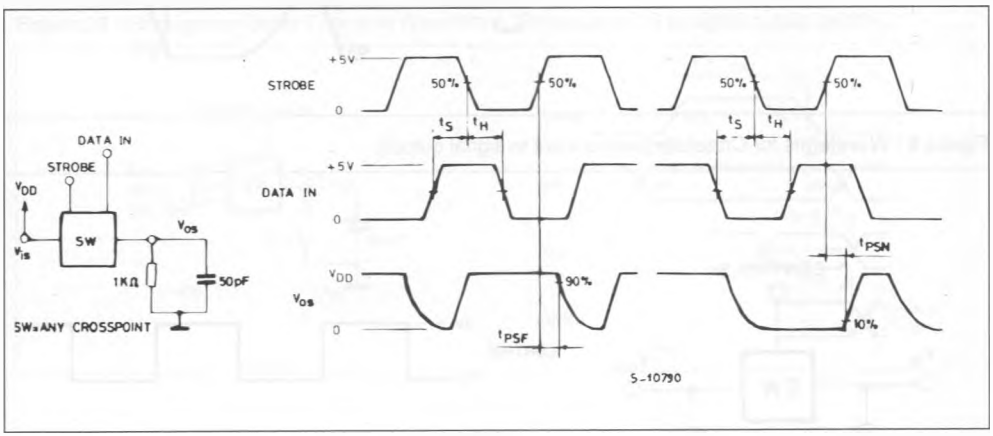


Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).

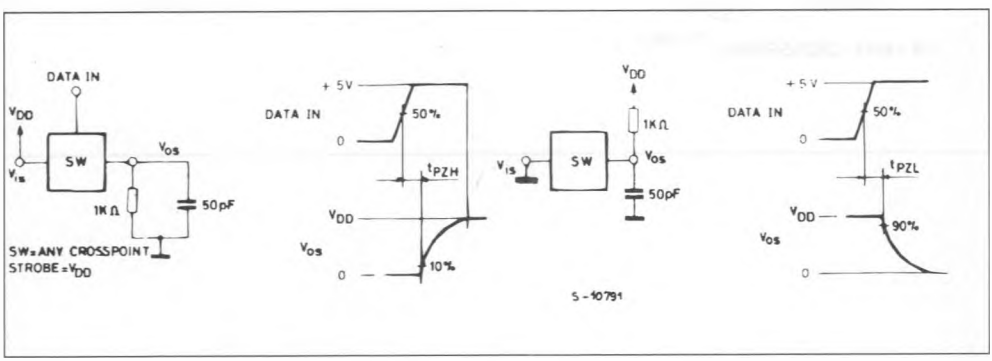


Figure 7 : Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).

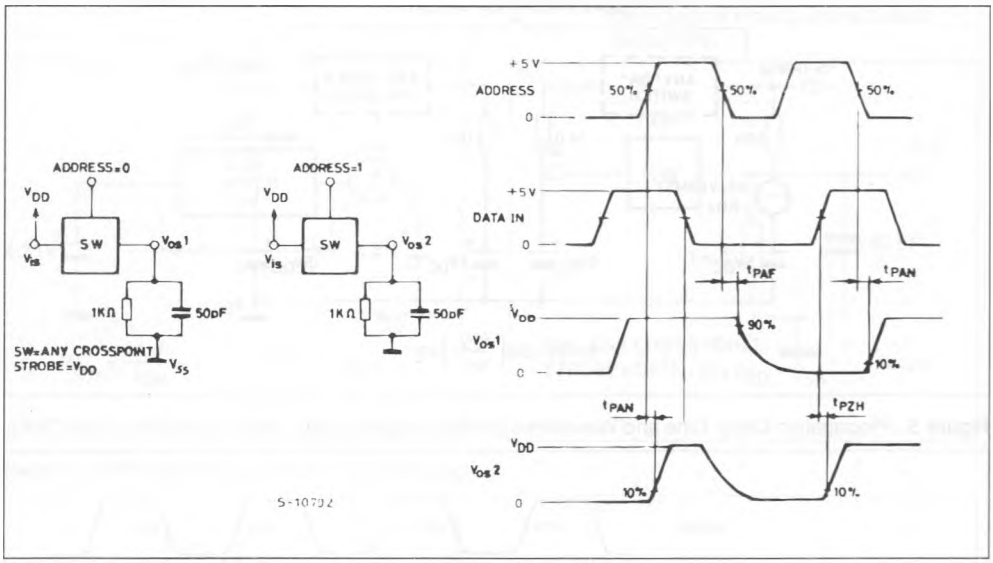


Figure 8 : Waveforms for Crosstalk (control input to signal output).

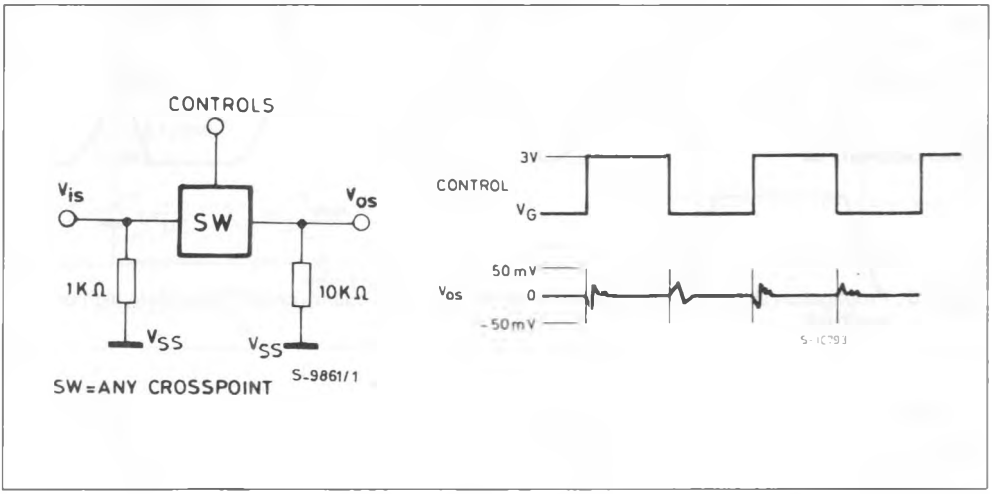


Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).

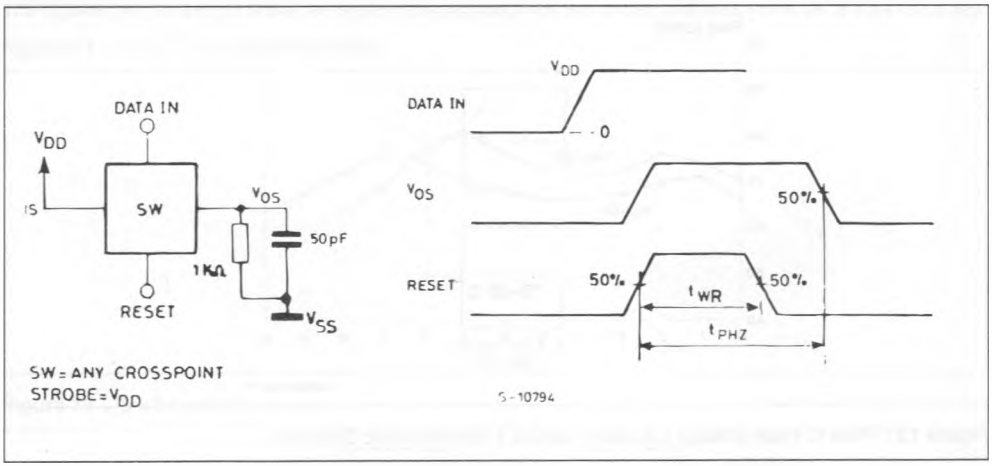


Figure 10 : Propagation Delay Time and Waveforms (Strobe and C/S to signal output switch).

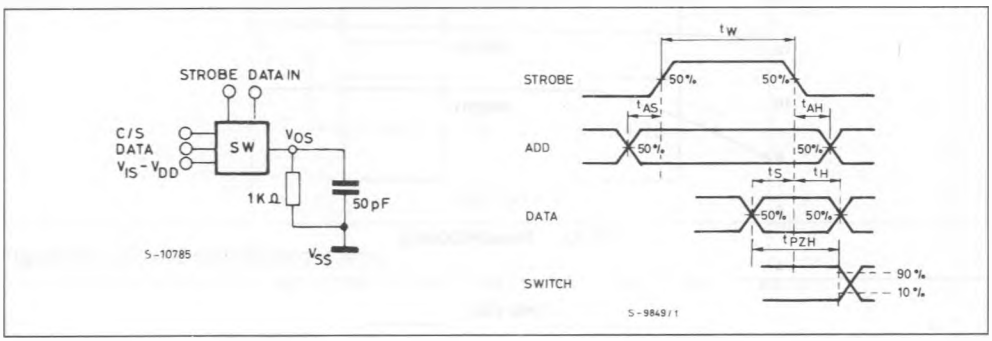


Figure 11 : Typical R_{ON} versus V_{IS}.

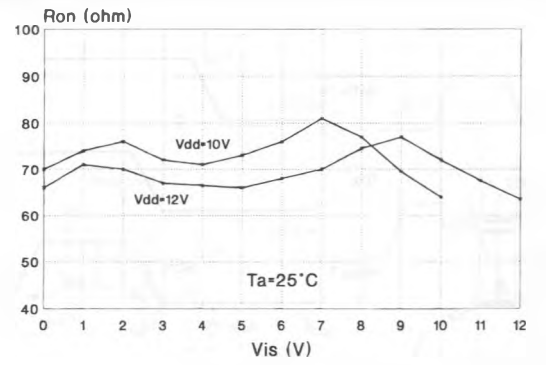


Figure 12 : Peak to Peak Voltage Capability versus Total Harmonic Distortion.

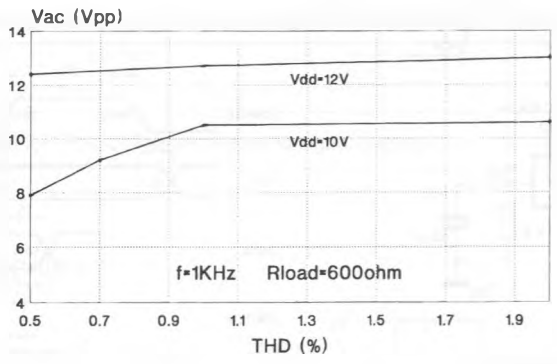
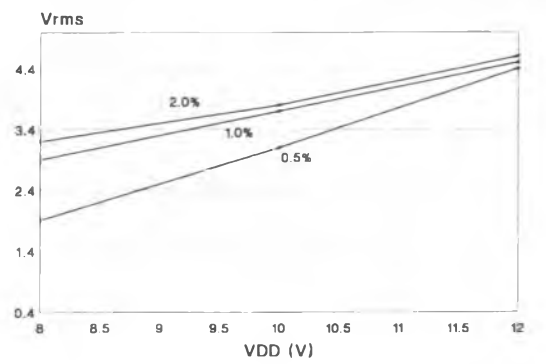


Figure 13 : V_{RMS} Capability versus V_{DD}.



TYPICAL APPLICATIONS

The figures 14, 15 and 16 show the system configuration for expanded matrices (16 x 16, 8 x 64, 32 x 32).

Figure 14 : (16 x 16 non blocking matrix).

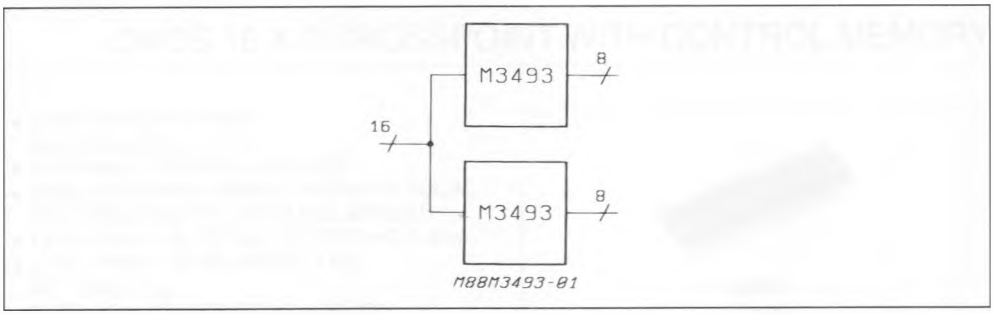


Figure 15 : (8 x 64 matrix).

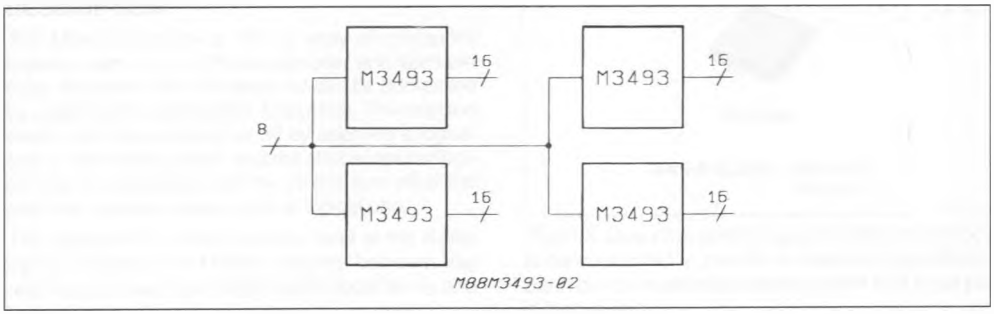


Figure 16 : (32 x 32 non blocking matrix).