REMOTE CONTROL TRANSMITTERS
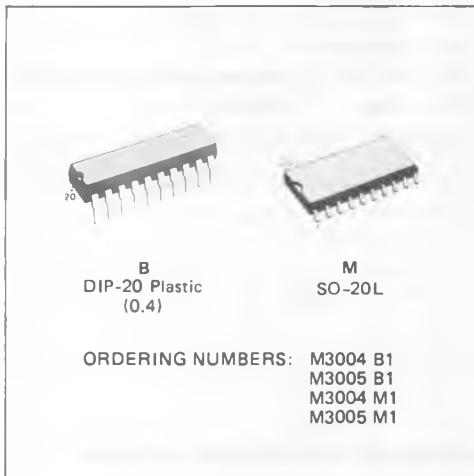
- FLASHED OR MODULATED TRANSMISSIONS (M3004 = $f_{osc/12}$, M3005 = f_{osc})
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (I_{OH} = -40mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- "LOCK-UP" PROTECTION TO PREVENT BATTERY DISCHARGE
- VERY LOW STAND-BY CURRENT ($< 2\mu A$)
- OPERATIONAL CURRENT < 2mA AT 6V SUPPLY
- WIDE SUPPLY VOLTAGE RANGE (4 TO 10.5V)
- CERAMIC RESONATOR CONTROLLED FREQUENCY (400 TO 600KHz)
- CMOS SI-GATE TECHNOLOGY
- PACKAGES: 20-LEAD PLASTIC DIL OR 20-LEAD PLASTIC SMALL OUTLINE (SO-20)

B
DIP-20 Plastic
(0.4)

M
SO-20L

ORDERING NUMBERS: M3004 B1
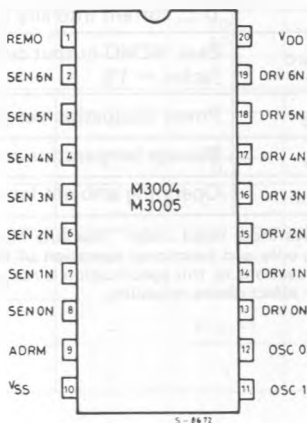M3005 B1
M3004 M1
M3005 M1

DESCRIPTION

The M3004/M3005 transmitter ICs are designed for infrared remote control systems. They have a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004/M3005 generate the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated.

Modulated pulses allow receivers with narrowband preamplifier for improved noise rejection to be used. In the M3004 the modulation frequency is $f_{osc/12}$ about 38KHz with (f_{osc} = 455KHz) while in the M3005 the modulation frequency corresponds to f_{osc}. In flash mode the M3004 and M3005 are identical. Flashed pulses require a wideband preamplifier within the receiver.

PIN CONNECTION

	M3004 M3005	
REMO 1		20 V_{DD}
SEN 6N 2		19 DRV 6N
SEN 5N 3		18 DRV 5N
SEN 4N 4		17 DRV 4N
SEN 3N 5		16 DRV 3N
SEN 2N 6		15 DRV 2N
SEN 1N 7		14 DRV 1N
SEN 0N 8		13 DRV 0N
ADRM 9		12 OSC 0
V_{SS} 10		11 OSC 1

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PIN NAMES

1	REMO	Remote data output	11	OSCI	Oscillator input
2	SEN6N		12	OSCO	Oscillator output
3	SEN5N		13	DRV0N	
4	SEN4N		14	DRV1N	
5	SEN3N	Key matrix sense inputs	15	DRV2N	
6	SEN2N		16	DRV3N	Key matrix drive outputs
7	SEN1N		17	DRV4N	
8	SEN0N		18	DRV5N	
9	ADRM	Address mode control inputs	19	DRV6N	
10	V_{SS}	Ground	20	V_{DD}	Positive supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage range	-0.3 to + 12	V
V_I	Input voltage range	-0.3 to V_{DD} + 0.3	V
V_O	Output voltage range	-0.3 to V_{DD} + 0.3	V
$\pm I$	D.C. current into any input or output	max.　　10	mA
I_{REMO}	Peak REMO output current during 10μs; duty factor = 1%	max.　　-300	mA
P_{tot}	Power dissipation per package for T_{amb} = 0 to 70°C	max.　　200	mW
T_{stg}	Storage temperature range	-55 to 150	°C
T_{amb}	Operating ambient temperature range	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $(V_{SS} = 0V; T_{amb} = 25°C;$ unless otherwise specified)

Symbol	V_{DD} (V)	Parameter	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	—	Supply voltage $T_{amb} = 0$ to +70°C	4	—	10.5	V
I_{DD}	6	Supply current; active $f_{osc} = 455KHz$; REMO output unloaded	—	0.4	—	mA
	9		—	0.8	—	
I_{DD}	6	Supply current; inactive (stand-by mode) $T_{amb} = 25°C$	—	—	2	μA
	9		—	—	2	
f_{osc}	4 to 11	Oscillator frequency (ceramic resonator)	400	—	600	KHz

KEYBOARD MATRIX

		Inputs SEN0N to SEN6N				
V_{IL}	4 to 11	Input voltage LOW	—	—	$0.2 \times V_{DD}$	V
V_{IH}	4 to 11	Input voltage HIGH	$0.8 \times V_{DD}$	—	—	V
I_I	4	Input current $V_I = 0V$	-10	—	-100	μA
	11		-30	—	-300	
I_I	11	Input leakage current $V_I = V_{DD}$	—	—	1	μA
		Outputs DRV0N to DRV6N				
V_{OL}	4	Output voltage "ON" $I_O = 0.1mA$	—	—	0.3	V
	11	$I_O = 1.0mA$	—	—	0.5	
I_O	11	Output current "OFF" $V_O = 11V$	—	—	10	μA

CONTROL INPUT ADRM

V_{IL}	—	Input voltage LOW	—	—	$0.2 \times V_{DD}$	V
V_{IH}	—	Input voltage HIGH	$0.8 \times V_{DD}$	—	—	V
		Input current (switched P and N-channel pull-pu/pull-down)				
I_{IL}	4	Pull-up active stand-by voltage: 0V	-10	—	-100	μA
	11		-30	—	-300	
I_{IH}	4	Pull-down active stand-by voltage: V_{DD}	10	—	100	μA
	11		30	—	300	

DATA OUTPUT REMO

V_{OH}	6	Output voltage HIGH $-I_{OH} = 40mA$	3	—	—	V
	9		6	—	—	
V_{OL}	6	Output voltage LOW $I_{OL} = 0.3mA$	—	—	0.2	V
	9		—	—	0.1	
t_{OH}	6	Pulse length oscillator stopped	—	—	1	ms

OSCILLATOR

I_I	6	Input current OSCI at V_{DD}	0.8	—	2.7	μA
V_{OH}	6	Output voltage HIGH $-I_{OL} = 0.1mA$	—	—	V_{DD} -1	V
V_{OL}	6	Output voltage LOW $I_{OH} = 0.1mA$	—	—	1	V

Fig. 1 - Transmitter with M3004/M3005
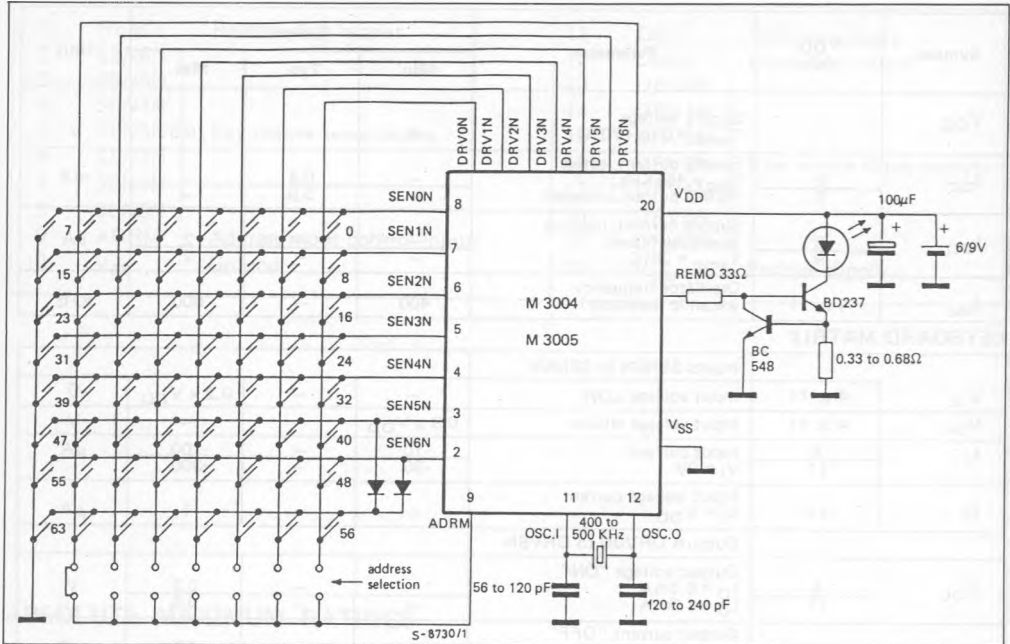
INPUTS AND OUTPUTS

KEY MATRIX INPUTS AND OUTPUTS (DRV0N TO DRV6N AND SEN0N TO SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE AND TRANSMISSION MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 5. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or con-

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INPUTS AND OUTPUTS (continued)

nected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format are listed in Table 1 and 2 (M3004), 3 and 4 (M3005).

The information is defined by the distance t_B between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2, 3 and 4. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Table 5 and 6.

The REMO output is protected against "lock-up", i.e. the lenght of an output pulse is limited to < 1ms even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (OSCI AND OSCO)

The external components must be connected to these pin when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400KHz and 600KHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

KEYBOARD OPERATION

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 5) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 6) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 6). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

FUNCTIONAL DESCRIPTION (continued)

There are two restrictions caused by the special structure of the keyboard matrix:

— The keys switching to ground (code numbers 7, 15. 23. 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.

— SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line because this condition has been used for the definition of additional codes (code numbers 50 to 63).

OUTPUT SEQUENCY (DATA FORMAT)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed.

The format of the output pulse train is given in Figs. 2, 3 and 4. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 5). The toggle bits remain unchanged within a multiple key-stroke sequence.

Fig. 2 – Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = sub-system address; A, B, C, D, E and F = command bits.
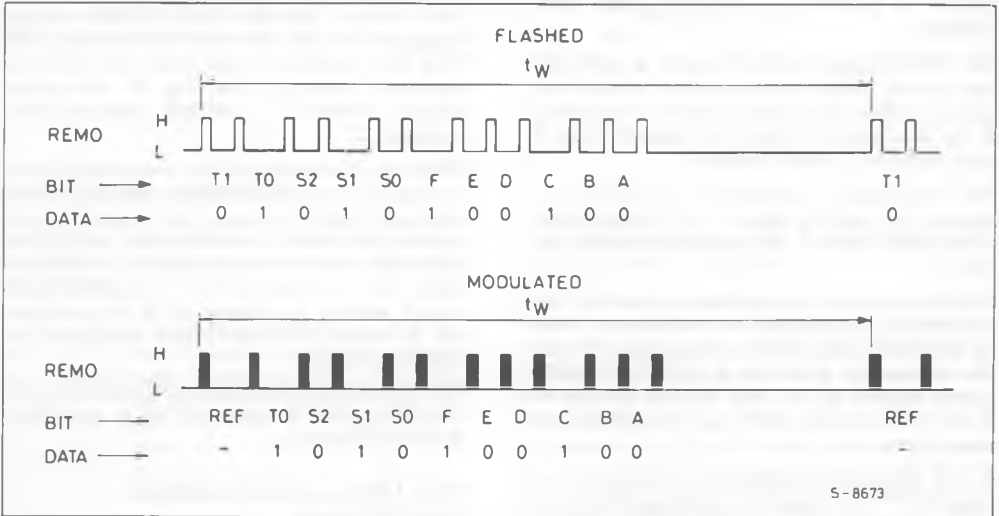
— Flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).

— Modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

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FUNCTIONAL DESCRIPTION (continued)

Fig. 3 – REMO output waveforms (M3004)
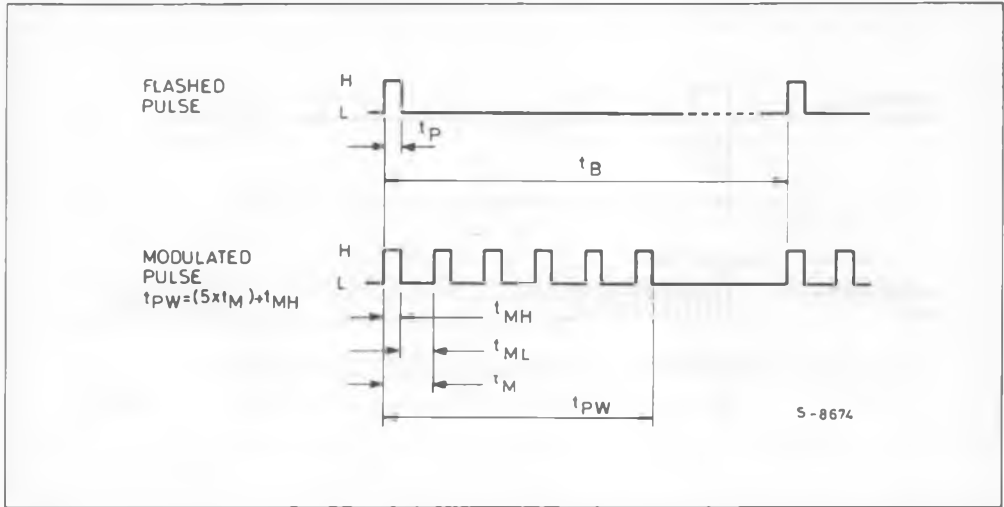
Table 1 – Pulse train timing (M3004); f_{osc} = 455KHz

Mode	T_o ms	t_P μs	t_M μs	t_{ML} μs	t_{MH} μs	t_W ms
Flashed (f_{osc} = 455KHz)	2.53	8.8	—	—	—	121
Modulated (f_{osc} = 455KHz)	2.53	–	26.4	17.6	8.8	121

Table 2 – Pulse train separation (t_B) (M3004)

Code	t_B
Logic "0"	$2 \times T_o$
Logic "1"	$3 \times T_o$
Reference time	$3 \times T_o$
Toggle bit time	$2 \times T_o$ or $3 \times T_o$

f_{osc}	455KHz	t_{osc} = 2.2μs
t_P	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\ 196 \times t_{osc}$	word distance

FUNCTIONAL DESCRIPTION (continued)
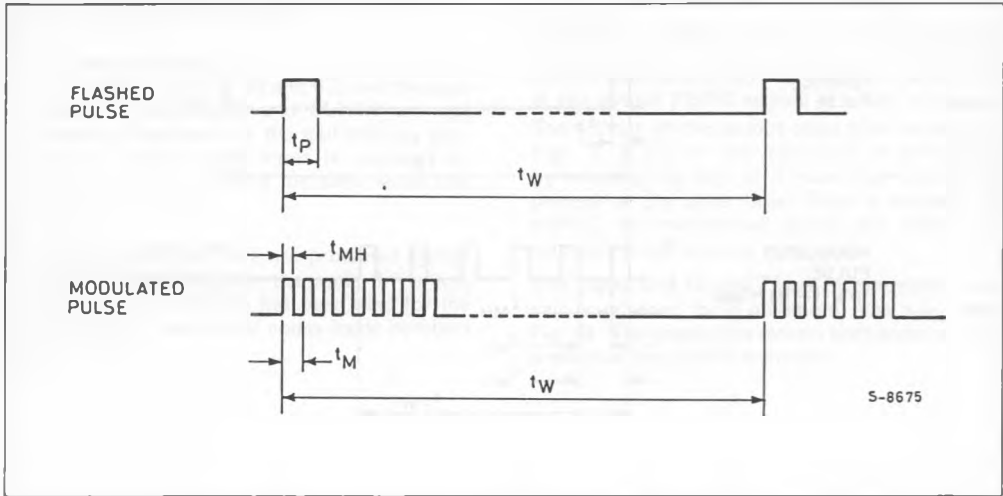
Fig. 4 - REMO output waveforms (M3005)

Table 3 - Pulse train timing (M3005)

Mode	T_O ms	t_P μs	t_M μs	t_W ms
Flashed (f_{osc} = 455KHz)	2.53	8.8	—	121
Modulated (f_{osc} = 600KHz)	2.53	—	1.66	121

Table 4 - Pulse train separation (t_B) (M3005)

Code	t_B
Logic "0"	$2 \times T_O$
Logic "1"	$3 \times T_O$
Reference time	$3 \times T_O$
Toggle bit time	$2 \times T_O$ or $3 \times T_O$

	Flashed mode (455 KHz)	Modulated mode (600KHz)	
t_{osc}	2.2μs	1.66μs	
t_P	$4 \times t_{osc}$	—	flashed pulse width
t_M	—	t_{osc}	modulation period
N	—	8	number of modulation pulses
T_O	$1152 \times t_{osc}$	$1536 \times t_{osc}$	basic unit of pulse distance
t_W	$55296 \times t_{osc}$	$73728 \times t_{osc}$	word distance
t_{MH}/t_M	—	0.4 to 0.6	pulse duty cycle during carrier mode

NOTE — The different dividing ratio for I_O and t_W between fashed mode and modulated mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during modulated mode. This allows the use of a 600KHz ceramic resonator during modulated mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W.

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FUNCTIONAL DESCRIPTION (continued)

Fig. 5 – Single key-stroke sequence. Debounce time: $t_{DB} = 4$ to $9 \times T_o$. Start time: $t_{ST} = 5$ to $10 \times T_o$. Minimum release time: $t_{REL} = T_o$. Word distance: t_W.
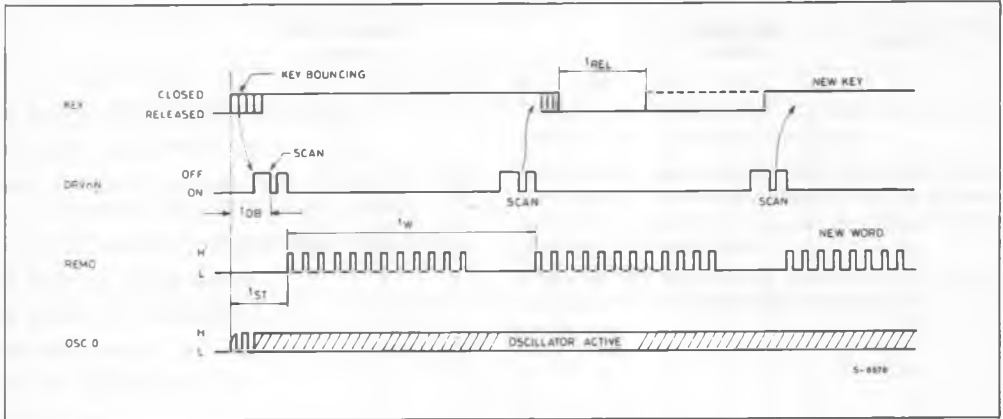

Fig. 6 – Multiple key-stroke sequence. Scan rate multiple key-stroke: $t_{SM} = 8$ to $10 \times T_o$. For t_{DB}, t_{ST} and t_W see Fig. 5.
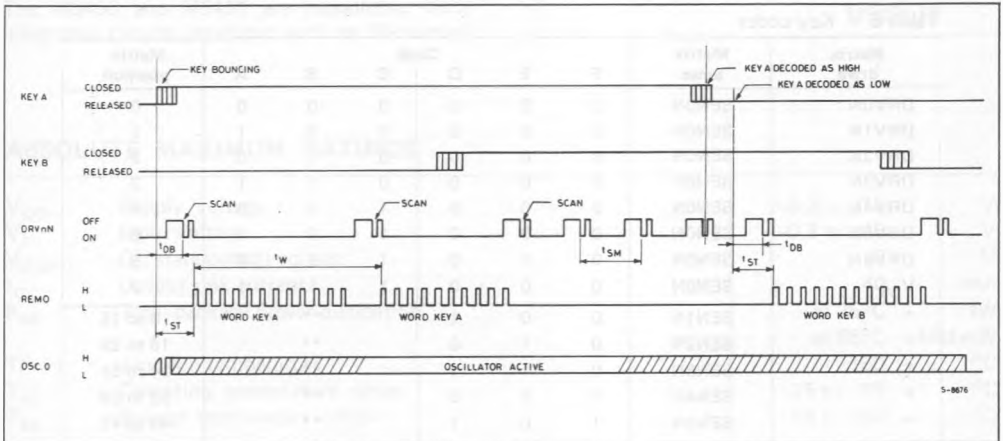
Table 5 – Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

Mode	Sub-system address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM   blank = not connected to ADRM   X = don't care

Table 6 – Key codes

Matrix drive	Matrix sense	Code						Matrix position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V$_{SS}$	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

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