MOS INTEGRATED CIRCUIT

M 2114

PRELIMINARY DATA

1024 x 4 BIT STATIC RAM

- SINGLE +5V SUPPLY
- IDENTICAL CYCLE AND ACCESS TIMES
- COMPLETELY STATIC MEMORY-NO CLOCK OR TIMING STROBE REQUIRED
- DIRECTLY TTL COMPATIBLE: ALL INPUTS AND OUTPUTS
- COMMON DATA INPUT AND OUTPUT USING THREE-STATE OUTPUTS
- HIGH DENSITY 18 PIN PACKAGE

M2114	M2114-2	M2114-3	M2114	M2114L2	M2114L3	M2114L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Current (mA)	100	100	100	70	70	70

The M2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided. The M2114 is designed for memory applications where high performance and high reliability, low cost, large bit storage, and simple interfacing are important design objectives. The M2114 is placed in an 18-pin package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

ABSOLUTE MAXIMUM RATINGS*

V_i	Voltage on any pin with respect to ground	3.5 to +7	V
P_{tot}	Total power dissipation	1	W
I_{out}	D.C. output current	5	mA
T_{amb}	Ambient temperature under bias	-10 to 80	°C
T_{stg}	Storage temperature range	-65 to 150	°C

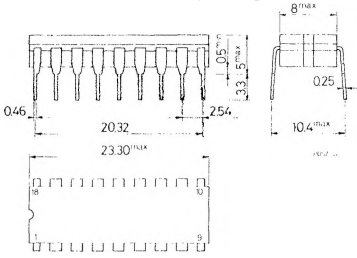
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS: M2114
M2114-2
M2114-3
M2114L
M2114L2
M2114L3
add suffix F1 for frit-seal ceramic DIP or B1 for plastic DIP.

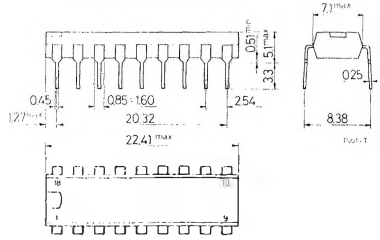
M 2114

MECHANICAL DATA (dimensions in mm)

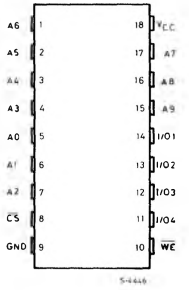
Dual in-line ceramic package, frit seal



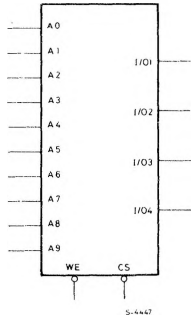
Dual in-line plastic package



PIN CONNECTIONS



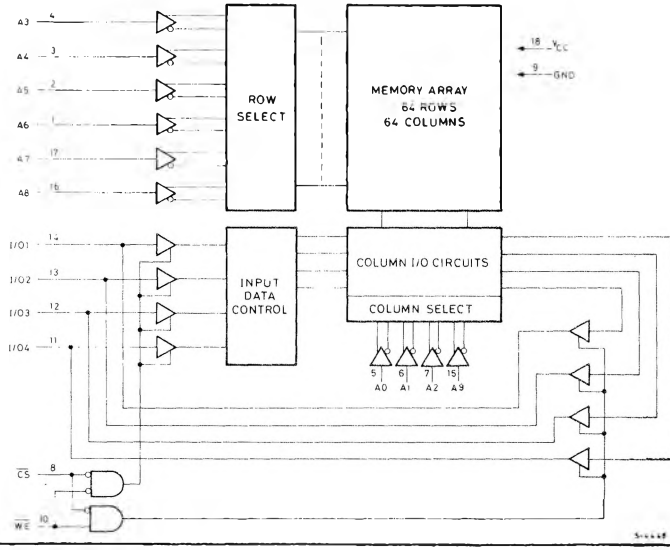
LOGIC DIAGRAM



PIN NAMES

A0–A9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O1–I/O4	DATA INPUT/OUTPUT	

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted)

Parameter		Test conditions	2114-2, 2114-3, 2114			2114L2, 2114L3, 2114L			Unit
			Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
I_{LI}	Input Load Current (All Input Pins)	V_I = 0 to 5.25V			10			10	µA
$\|I_{LO}\|$	I/O Leakage Current	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}			10			10	µA
I_{CC1}	Power Supply Current	V_I = 5.25V, $I_{I/O}$ = 0 mA, T_{amb} = 25°C		80	95			65	mA
I_{CC2}	Power Supply Current	V_I = 5.25V, $I_{I/O}$ = 0 mA, T_{amb} = 0°C			100			70	mA
V_{IL}	Input Low Voltage		-0.5		0.8	-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		6.0	2.0		6.0	V
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.1	6.0		2.1	6.0		mA
I_{OH}	Output High Current	V_{OH} = 2.4V	-1.0	-1.4		-1.0	-1.4		mA
I_{OS}(2)	Out. Short Circuit Current				40			40	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted)

Parameter		2114-2, 2114L2		2114-3, 2114L3		2114, 2114L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE (3)								
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Deselection		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns
WRITE CYCLE (4)								
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Output 3-state from Write		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

CAPACITANCES(5) (T_{amb} = 25°C, f = 1.0 MHz)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V			5	pF
C_I	Input Capacitance	V_I = 0V			5	pF

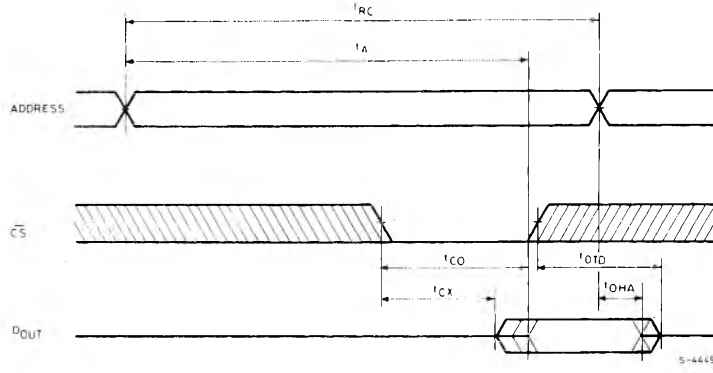
Notes: 1. Typical values are for T_{amb} = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.
3. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
4. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
5. This parameter is periodically sampled and not 100% tested.

A.C. TEST CONDITIONS

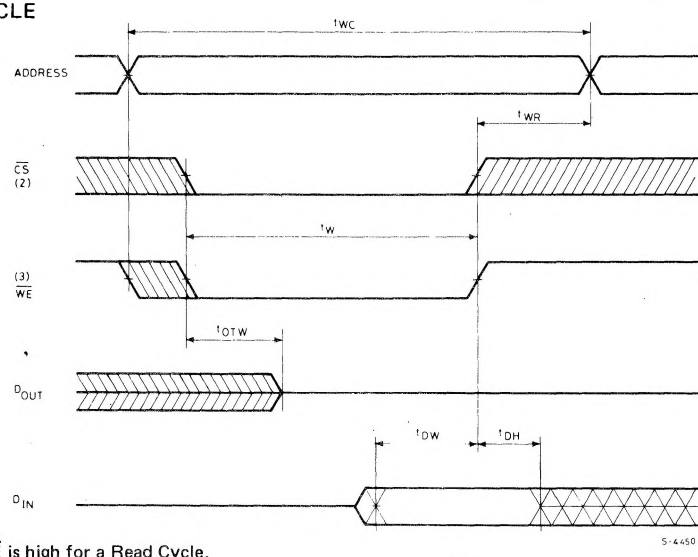
Input Pulse Levels for M2114 = 0.8V to 2.4V
Input Rise and Fall Times = 10 ns
Input and Output Timing Levels = 1.5V
Output Load = 1 TTL Gate and C_L = 100 pF

WAVEFORMS

READ CYCLE (1)



WRITE CYCLE



Notes: 1. $\overline{WE}$ is high for a Read Cycle.
2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
3. $\overline{WE}$ must be high during all address transitions.