MOS INTEGRATED CIRCUIT

SGS M 190

16 KEY KEYBOARD ENCODER AND LATCH

- ANTIBOUNCE AND ANTINOISE CIRCUITRY
- INTERLOCK PREVENTS INCORRECT SELECTION
- OPERATES WITH SINGLE POLE PUSH-BUTTONS
- SELECTION OF PROGRAM 1 AT POWER ON
- MUTING OUTPUT AVAILABLE DURING PROGRAM CHANGES AND POWER SUPPLY SWITCHING
- STEP-BY-STEP PROGRAM CHANGE INPUT
- KEYBOARD LOCKING
- OUTPUTS DIRECTLY COMPATIBLE WITH M 193 (ELECTRONIC PROGRAM MEMORY), M 192 (7-SEGMENT DECODER DRIVER), H 770/1/2/3 (QUAD ANALOG SWITCHES)

The M 190 is a monolithic integrated circuit which automatically scans an up to 16 Key keyboard, generating continuous sequential pulses on X outputs and detecting key closure on Y inputs.
A key closure is retained as valid when the key remains closed for all the time corresponding to one scan pulse (i.e. when the bounce is over).
When it occurs an internal flip-flop is set but the key closure is accepted only if it is detected on a second scan cycle. At this point a 4 bit word corresponding to the key closed is internally latched and a pulse is available on the Muting output.
During the time this pulse lasts, no other key closure will be recognized. The new output code follows the Mute signal with a delay.
All the timing for the circuits is determined by the clock oscillator whose frequency is externally fixed by an RC network.
The M 190 also includes a "step-by-step" program change input that, when connected to V_{SS} (GND), advances by one the selected channel and a Lock which blocks the circuit on the last selected channel.
The circuit is produced in N-channel silicon gate technology and is available in a 18 pin dual in-line plastic package.

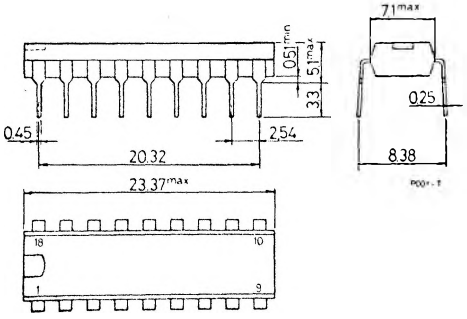
ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to 20	V
$V_{O(off)}$	Off state output voltage (pins 1-2-3-4-11)	20	V
I_O	Output current	|5|	mA
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 125	°C
T_{op}	Operating temperature	0 to 70	°C

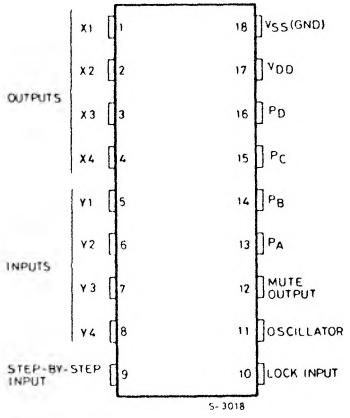
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
** All voltage are referred to V_{SS} pin voltage.

ORDERING NUMBER: M 190 B1

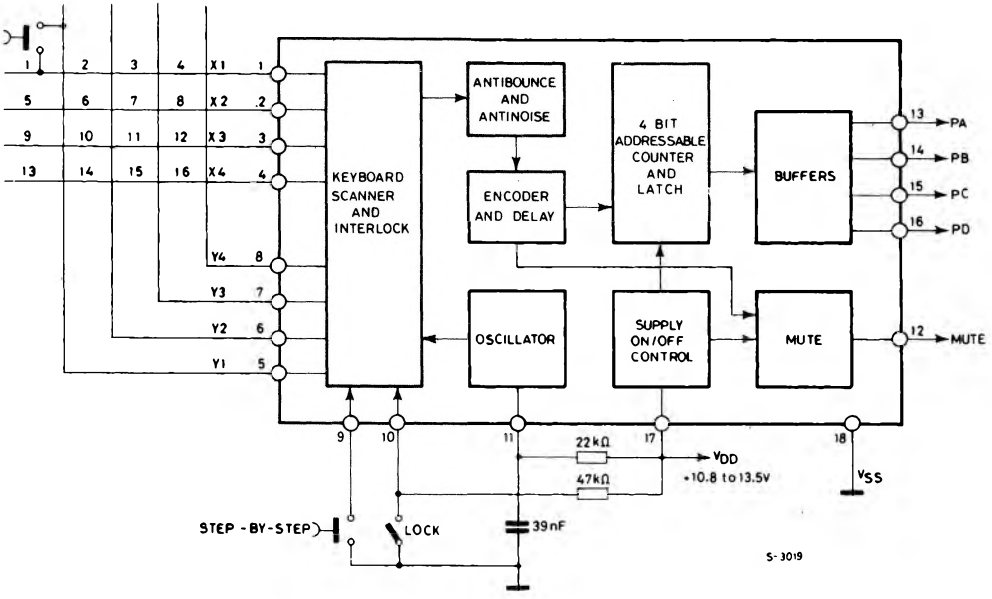
MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	10.8 to 13.5	V
V_I	Input voltage	0 to 13.5	V
$V_{O(off)}$	Off state output voltage (pins 1-2--3-4-11)	max 13.5	V
I_O	Output current	max |2|	mA
T_{op}	Operating temperature	0 to 70	°C
R_t	Timing resistor	8 to 47	KΩ
C_t	Timing capacitor	1 to 330	nF

STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Parameter		Test conditions	Values at 25°C			Unit
			Min.	Typ.	Max.	
V_{IH}	High level input voltage	pins 5, 6, 7, 8, 9, 10	3.5			V
V_{IL}	Low level input voltage	pins 5, 6, 7, 8, 9, 10			0.8	V
I_{IH}	High level input current	V_{DD}= 13.5V, V_{IH}= 13.5V pins 5, 6, 7, 8, 9, 10			10	μA
I_{IL}	Low level input current	V_{DD}= 13.5V, V_{IL}= 0.8V pins 5, 6, 7, 8, 9, 10	0.1		0.8	mA
V_{OH}	High level output voltage	V_{DD}= 10.8V I_{OH}= -1 mA, pin 12	2.4			V
		V_{DD}= 10.8V I_{OH}= -1 mA, pins 13. 14, 15, 16	4			
V_{OL}	Low level output voltage	V_{DD}= 10.8V I_{OL}= 0.8 mA pins 1, 2, 3, 4, 11			0.4	V
		V_{DD}= 10.8V I_{OL}= 2 mA, pins 13, 14, 15, 16			0.4	
$I_{O(off)}$	Output leakage current	V_{DD}= $V_{O(off)}$= 13.5V, pins 1, 2, 3, 4, 11			20	μA
I_{DD}	Supply current	V_{DD}= 13.5V (all inputs and outputs open)			18	mA

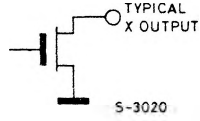
TRUTH TABLE

Key	Connection	Output code (positive logic)			
		PA	PB	PC	PD
1	$X_1 - Y_1$	L	L	L	L
2	$X_1 - Y_2$	H	L	L	L
3	$X_1 - Y_3$	L	H	L	L
4	$X_1 - Y_4$	H	H	L	L
5	$X_2 - Y_1$	L	L	H	L
6	$X_2 - Y_2$	H	L	H	L
7	$X_2 - Y_3$	L	H	H	L
8	$X_2 - Y_4$	H	H	H	L
9	$X_3 - Y_1$	L	L	L	H
10	$X_3 - Y_2$	H	L	L	H
11	$X_3 - Y_3$	L	H	L	H
12	$X_3 - Y_4$	H	H	L	H
13	$X_4 - Y_1$	L	L	H	H
14	$X_4 - Y_2$	H	L	H	H
15	$X_4 - Y_3$	L	H	H	H
16	$X_4 - Y_4$	H	H	H	H

DESCRIPTION

Pins 1, 2, 3, 4 – X_1, X_2, X_3, X_4 outputs

The internal open drain transistors on these outputs are sequentially switched on.

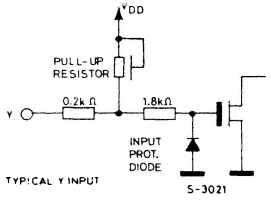


Pins 5, 6, 7, 8 – Y_1, Y_2, Y_3, Y_4 inputs

These inputs correspond to the columns of the keyboard matrix. When a key is pushed, one of the X output signal is present on one of the 4 rows, putting a low level on the Y input.
An interlock circuit rejects more than one key pressed at the same time.
To increase the noise immunity of the system and to avoid bouncing problems, the key closure is considered valid only when it is present for all the time corresponding to the scan pulse. With this system spurious noise signals are also rejected.
Another increase in the noise immunity is given by detecting key closure over two consecutive scanning cycles.

DESCRIPTION (continued)

After the key bounce time, the acceptance time of a command is between 35T and 63T, where T is the period of the clock pulse.
When any input is open it is pulled-up to logic H by an integrated MOS load of about 50 KΩ and protected by a diode.



Pin 9 - Step-by-step program change

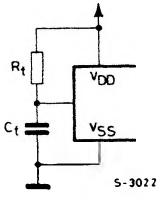
This input advances by one the previously selected channel every time ti is connedted to ground.
This input can be considered as a 17th key and follows all the rules of command acceptance time and partially of interlock.
The unput is pulled-up to logic H by an integrated resistor of about 50 KΩ ; if the input is not used, it should be connected to V_{DD}.

Pin 10 - Lock

If this input is connected to V_{SS} (GND) the circuit is locked on the selected channel.
If the input is not used, it must be connected to V_{DD}.

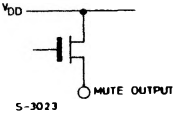
Pin 11 - RC network (clock oscillator input)

An internal clock provides all the timing for the circuits.
The frequency of the clock oscillator is controlled by two external components, resistor R_t and capacitor C_t.
The period of the clock pulse is approximately given by $T = R_tC_t$.
The oscillator works in the following way: assuming the capacitor C_t is discharged, the resistor R_t charges the capacitor till an internal threshold is reached. At this point the capacitor is discharged by an internal transistor.
Afterwards the internal transistor is switched off and the cycle can restart.
With R_t= 22 KΩ and C_t= 39 nF a clock frequency of about 800 Hz is obtained, corresponding to a scan cycle of the keyboard of about 40 ms.
In these conditions the mute signal will be present for about 100 ms before the program changing and will last 300 ms.

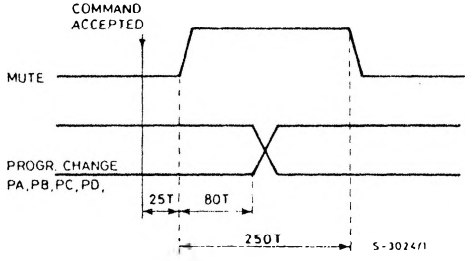


Pin 12 - Mute

The mute signal is available as a high level output (source follower transistor).
It is present during power ON/OFF and program changes.



When a command is given the Mute signal and the program information are available in the following way:



The Mute signal is not available when the same program is selected again.

Pins 13, 14, 15, 16 - PA, PB, PC, PD outputs

These static outputs select the program according to the truth table.
They interface directly with the inputs of M 193 (Electronic Program Memory), M 192 (7 segment Decoder/Driver), H 770/1/2/3 (Quad Analog Switches).
The program 1 is internally selected at power ON.