MOS INTEGRATED CIRCUIT

M 120

PRELIMINARY DATA

1024 BIT - NON VOLATILE RANDOM ACCESS MEMORY (NV-RAM)

- 256 x 4 ORGANIZATION
- OPTIMUM DATA RETENTION: ONE ORDER OF MAGNITUDE GREATER THAN MNOS DEVICES
- MORE THAN 10^4 MODIFY OPERATIONS PER BIT
- THREE VERSIONS WITH DIFFERENT READ AND MODIFY ACCESS TIMES: M120-2:450 ns - M120 : 700 ns - M120-4 : 950 ns
- INTERNAL WORD MODIFY TIME LESS THAN 100 msec
- "MODIFY END" OUTPUT LINE
- TTL COMPATIBLE: EASY CONNECTION TO ANY MICROPROCESSOR
- COMMON DATA INPUTS AND OUPUTS
- ON CHIP LATCHES FOR ADDRESSES AND DATA
- POWER SUPPLIES V_{DD} = 12V ± 10%
  V_{PP} = 25V ± 5%
- STANDARD 18-PIN DUAL-IN-LINE PACKAGE

The M120 is a new Non Volatile Random Access Memory (NV-RAM). Contents of every word (256 x 4 available on-chip) can be erased and written electrically and data is retained without power supply for 100 years (calculated from test results). SGS-ATES proprietary n-channel, Si-gate, double Polysilicon MOS Technology insures maximum reliability and data retention and allows any number of read operations and more than 10.000 modify cycles per bit. Thanks to an internal circuitry taking care of the modify sequence, access times for both read and modify operations are short enough to allow use with most microprocessors without insertion of wait states. The M120 is available in three different versions. The slowest M120-4 in particular, with 950 ns access time, is intended for applications where the M120 is used in combination with a single chip microcomputer. In these applications all the signals are supplied by the microcomputer I/O ports, and the access time required is always in the range of microseconds. The M120 is available in a standard 18-pin dual-in-line plastic or ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS*

	Input or output voltages (except V_{DD} and V_{PP})	-0.5 to 15	V
V_{DD}	Supply voltage	-0.5 to 20	V
V_{PP}	Supply voltage	-0.5 to 28	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

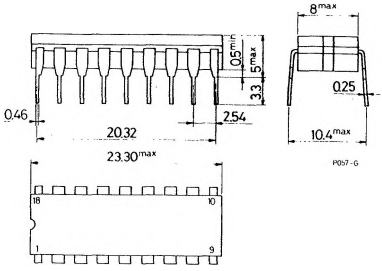
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stresses rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS:

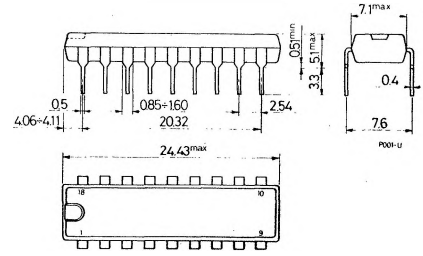
M120F1	for dual in-line ceramic package (frit seal)
M120B1	for dual in-line plastic package
M120-2F1	for dual in-line ceramic package (frit seal)
M120-2B1	for dual in-line plastic package
M120-4F1	for dual in-line ceramic package (frit seal)
M120-4B1	for dual in-line plastic package

MECHANICAL DATA (dimensions in mm)

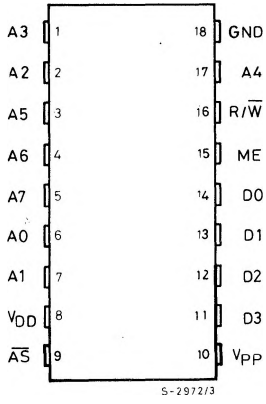
Dual in-line ceramic package, frit-seal



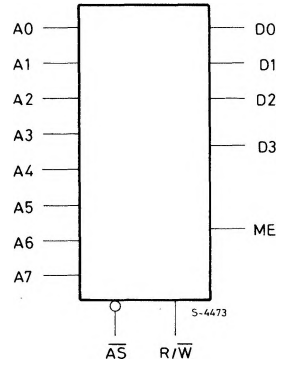
Dual in-line plastic package



PIN CONNECTIONS



LOGIC DIAGRAM



PIN NAMES

D0–D3	DATA INPUTS/OUTPUTS (OPEN DRAIN)
A0–A7	ADDRESS INPUTS
$\overline{AS}$	ADDRESS STROBE INPUT
R/$\overline{W}$	READ/WRITE INPUT
ME	MODIFY END OUTPUT (OPEN DRAIN)
V_{PP}	POWER (+25V)
V_{DD}	POWER (+12V)
GND	GROUND

DC AND OPERATING CHARACTERISTICS (T_{amb}= 0°C to 70°C, V_{DD}= +12V ± 10%, V_{PP}= +25V ± 5%)

Parameter		Test conditions	Values			Unit
			Min.	Typ.*	Max.	
I_{DD1}	V_{DD} supply current				30	mA
I_{PP1}	V_{PP} supply current				20	mA
I_{DD2}	Standby V_{DD} supply current	$\overline{AS}$ @ V_{IH}			20	mA
I_{PP2}	Standby V_{PP} supply current	$\overline{AS}$ @ V_{IH}			10	mA
V_{IH}	Input high voltage		2.4	5		V
V_{IL}	Input low voltage		-0.3	0	0.6	V
V_{OL}	Output low voltage	I_{OL}= 1.6 mA			0.4	V
I_{LI}	Input leakage current				10	µA
I_{LO}	Output leakage current				10	µA

* Typical values are at +25°C and nominal voltages.

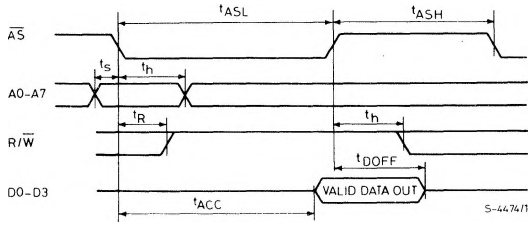
AC CHARACTERISTICS

Parameter		M 120-2		M 120		M 120-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_s	Set-up time	50		50		100		ns
t_h	Hold time	150		150		250		ns
t_{ASL}	$\overline{AS}$ active time	450	100K	700	100K	950	100K	ns
t_{ASH}	$\overline{AS}$ inactive time	350		500		500		ns
t_R	$\overline{AS}\downarrow$ to R/$\overline{W}\uparrow$ (Read)		100		150		200	ns
t_{ACC}	Access time from $\overline{AS}\downarrow$		450		700		950	ns
t_{DOFF}	Data output turn-off delay		150		250		300	ns
t_M	Modify time (1) from R/$\overline{W}\uparrow$		100		100		100	ms
t_{WHE}	$\overline{AS}\downarrow$ to R/$\overline{W}\downarrow$ (Early write) (2) (3)		100		150		200	ns
t_{WE}	$\overline{AS}\downarrow$ to R/$\overline{W}\uparrow$ (Early Write)	450		700		950		ns
t_{MHE}	ME turn-on delay from R/$\overline{W}\downarrow$ (Early Write)		400		500		600	ns
t_{AS}	R/$\overline{W}\downarrow$ to $\overline{AS}\uparrow$ rising edge (Read/Write)	250		400		500		ns
t_{WH}	$\overline{AS}\downarrow$ to R/$\overline{W}\downarrow$ (Read/Write)	100		200		250		ns
t_{WL}	R/$\overline{W}$ Low time (Read/Write)	350	100K	500	100K	650	100K	ns
t_{DF}	Data Float from $\overline{AS}\downarrow$ (Read/Write)	150		250		300		ns
t_{MH}	ME turn-on delay from R/$\overline{W}\downarrow$ (Read/Write)		250		350		450	ns

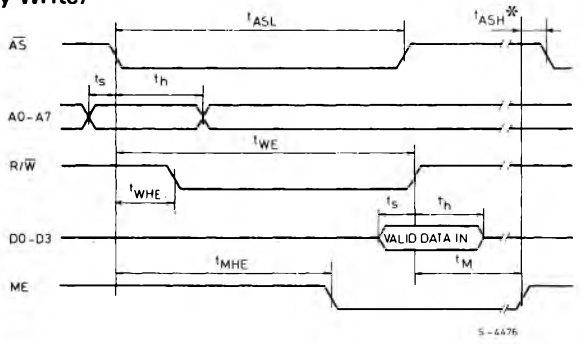
Notes:
1) $t_{M\,max}$ is 2 ms for the first 10 modify operations and increases to a maximum of 100 ms after 10^4 operations.
2) If $t_{WHE} \leqslant t_{WHE\,max}$ then D_{OUT} remains floating and there is no conflict between D_{OUT} and D_{IN}.
3) t_{WHE} can be < 0.

TIMING WAVEFORMS

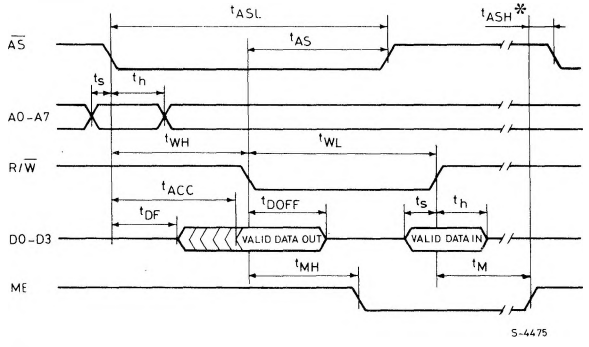
Read Cycle



Modify Cycle (Early Write)



Modify Cycle (Read/Write)



* The first falling edge of $\overline{AS}$ following the end of a modify cycle must occur at least t_{ASH} after the positive edge of ME.

DESCRIPTION OF OPERATION

M120 operation is controlled by the Address Strobe ($\overline{AS}$) control input (active low), which also performs the device selecting function.
The device is deselected (Stand-by Mode) by a high level on $\overline{AS}$ input.
The falling edge of $\overline{AS}$ latches Address lines (A0 ÷ A7) contents into the chip and starts both read and modify cycles.
If R/$\overline{W}$ remains high while $\overline{AS}$ is active a **Read Cycle** occurs. The contents of addressed memory location will be available on the Data lines (D0 ÷ D3) after an access time (t_{ACC}) from the leading edge of $\overline{AS}$.
The trailing edge of $\overline{AS}$ three-states Data lines after t_{DOFF} delay.
If R/$\overline{W}$ is or becomes low while $\overline{AS}$ is active a **Modify Cycle** starts.
Depending on timing relationships between $\overline{AS}$ and R/$\overline{W}$ leading edges, there are two possible modify sequences.
If R/$\overline{W}$ falling edge occurs either before or a maximum of t_{WHE} after $\overline{AS}$ falling edge, an **Early Write** Modify Cycle proceeds.
All timing relationships are related to $\overline{AS}$ falling edge and Data lines are not driven by the M120 thus avoiding any possible bus contention in this mode.
If R/$\overline{W}$ falling edge occurs a minimum of t_{WH} after $\overline{AS}$ falling edge a **Read/Write** Modify Cycle procedes.
Most timing relationships are in this case related to R/$\overline{W}$ falling edge. Because until R/$\overline{W}$ becomes active, the M120 assumes a read cycle is in process, the device will output addressed location contents on Data lines according to t_{DF}, t_{ACC} and t_{WH} timing specifications.
This allows a read/write operation to be performed but might also generate some contention on data lines.
However if set-up time requirements are satisfied, the M120 will operate properly since it floats data lines before latching data input.

INTERNAL MODIFY OPERATION AND "ME" OUTPUT

At rising edge of R/$\overline{W}$ in a modify cycle the contents of data lines are latched and the internal modify cycle starts.
The ME output, which indicates Modify Cycle End, goes false (low) after a delay of either t_{MHE} from $\overline{AS}$ leading edge (Early Write Modify Cycle) or t_{MH} from R/$\overline{W}$ falling edge (Read/Write Modify Cycle).
As long as ME is false the device is internally disconnected from buses and control lines, data outputs are floating and no further external operation will be acknowledged by M120.
During internal modify cycle an on-chip circuitry performs a bit by bit comparison between "old" and "new" data word and according to this result writes, erases or leaves unchanged each single bit of the addressed location.
At modify completion (t_M) ME line becomes true again and M120 is again available for external access.

POWER-UP

In order to avoid a spurious modify cycle, care should be taken during the power up sequence to ensure that $\overline{AS}$ and R/$\overline{W}$ are at the non-active (high) level before V_{DD} and V_{PP} reach half their operating value.
The opposite sequence should be followed during the power-down.
Power-on and power-down sequences can start arbitrarily with either V_{DD} or V_{PP}.