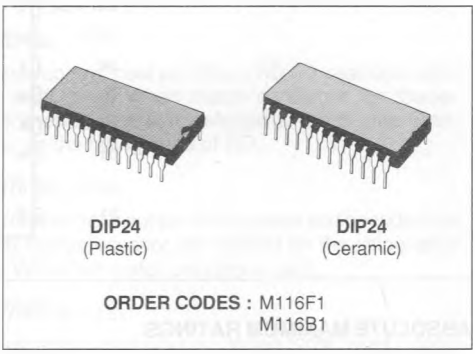
SGS-THOMSON MICROELECTRONICS

M116

PCM CONFERENCE CALL AND ATTENUATION/NOISE SUPPRESSION CIRCUIT

- 32 MAXIMUM CONFERENCED CHANNELS IN ANY COMBINATION FROM 10 CONFERENCES OF 3 CHANNELS TO 1 CONFERENCE OF 32 CHANNELS
- 3 TO 32 SERIAL CHANNELS PER FRAME (controlled by $\overline{\text{SYNC}}$ signal period)
- TWO OPERATION MODES AVAILABLE (conference and transparent modes)
- TYPICAL BIT RATES : 1536/1544/2048Kbits/s
- COMPATIBLE WITH ALL KINDS OF PCM BYTE FORMAT
- MU AND A LAWS AVAILABLE (pin programmable)
- EQUAL PRIORITY TO EVERY CHANNEL
- ONE FRAME (and one channel) DELAY FROM SENDING TO RECEIVING CHANNELS
- OVERFLOW INFORMATION FOR EACH CONFERENCE SENT OUT BY PINS $\overline{\text{OS}}$ (overflow signalling) AND ON DATABUS ON MPU REQUEST
- TONE OUTPUT FOR MASKABLE CONFERENCED CHANNELS. THE DURATION AND FREQUENCY ARE CONTROLLED BY EXTERNAL PINS (TD and TF)
- INSTRUCTION SET COMPATIBLE WITH THE M088
- PROGRAMMABLE ATTENUATION (0/3/6dB) ON EACH INPUT CHANNEL (both in conference or transparent mode)
- PROGRAMMABLE NOISE SUPPRESSION FOR EACH OUTPUT CHANNEL ACTING ON FOUR DIFFERENT LEVELS
- 5V POWER SUPPLY
- MOS AND TTL COMPATIBLE INPUT/OUTPUT LEVELS
- MAIN INSTRUCTIONS CONTROLLED BY THE MICROPROCESSOR INTERFACE :
  - Channel connection to a conference
  - Channel attenuation and/or noise suppression in transparent mode
  - Channel disconnection from both conference and transparent modes
  - Overflow status
  - Operating mode
  - Channel status



DIP24 (Plastic)

DIP24 (Ceramic)

ORDER CODES : M116F1
M116B1

DESCRIPTION

The M116 is a product specifically designed for applications in connection with PCM digital exchanges. It is able to handle up to 32 channels in any conference combination, from 3 people (max number of conferences is 10) to 32 people (only one conference).

The parties to be conferenced must previously be allocated through the Digital Switching Matrix (M088) in a single serial wire at the M116 PCM input (IN PCM pin).

Each channel is converted inside the chip from PCM law to linear law (14 bits). Then it is added to the sum of its conference, from which was previously subtracted its information from the previous frame. In this way a new sum signal is generated.

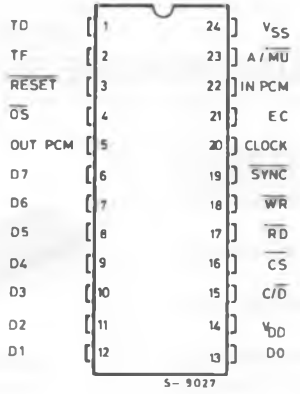
The channel output signal will contain the information of all the other channels in its conference except its own.

After the PCM encoding, the data is serialized by the M116 in the same sequence as the PCM input frame, with one frame (plus one channel) delay and will be reallocated by the DSM (M088) at the final channel and bus position.

A programmable attenuation as well as a programmable noise suppression threshold can be inserted in any channels connected in conference mode or in transparent mode.

M116 is realized with N-Channel technology and packaged in a 24 pin DIL package.

PIN CONNECTION

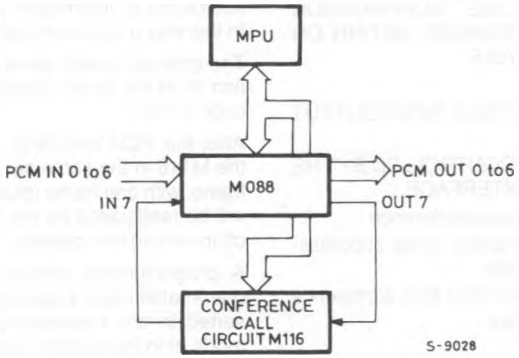


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage	– 0.3 to 20	V
V_i	Input Voltage	– 0.3 to V_{DD}	
$V_{O\ (off)}$	Off State Output Voltage	– 0.3 to 20	V
P_{tot}	Total Power Dissipation	500	mW
T_{stg}	Storage Temperature	– 65 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1 : PCM Conference Call Insertion Scheme.



PIN DESCRIPTION

TD (pin 1)

Tone Duration input pin. When TD = 1, a PCM coded tone is sent out to all channels of the enabled conferences instead of PCM data. TD is latched by the SYNC signal so that all channels have the same tone during the same number of frame. TD = 0 for normal operation.

TF (pin 2)

Tone Frequency input pin. When TF = 1, the tone's amplitude is high. When TF = 0, the tone's amplitude is low. TF is latched by the SYNC signal so that all channels have the same tone frequency during the same number of frame. The PCM coded tone levels correspond to the 1/10 of the full scale.

$\overline{\text{RESET}}$ (pin 3)

Master reset input pin. Reset must be used at the very beginning after power up to initialize the device or when switching from A Law to Mu Law. The internal initialization routine takes two time frames starting from the rising edge of $\overline{\text{RESET}}$. During this initialization time, all databus and PCM output are pulled to a high impedance state.

$\overline{\text{OS}}$ (pin 4)

Overflow Signalling output pin. When $\overline{\text{OS}}$ = 0 one conference is in overflow. This signal is delayed a little over half time slot with respect to the output channel involved in the conference in overflow, see Fig. 9. Ex : if output channel 3 is one of the parties of one conference in overflow, $\overline{\text{OS}}$ = 0 during the second half of the time slot corresponding to output channel 3.

OUT PCM (pin 5)

PCM output pin. The bit rate is 2048 Kbit/s max. The sign bit is the first bit of the serial sequence. The output buffer is open drain to allow for multiple connections.

D0 to **D7** (pins 6 through 13)

Bidirectional Data bus pins. Data and instructions are transferred to or from the microprocessor. D0 is the Least Significant Bit. The bus is tristate when RESET is low and/or $\overline{\text{CS}}$ is high.

C/$\overline{\text{D}}$ (pin 15)

Control input pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data while C/D = 1 qualifies it as an opcode. In a read operation, the overflow information of the first eight conferences is selected by C/$\overline{\text{D}}$ = 0, the overflow of the last two conferences and the status by C/D = 1.

$\overline{\text{CS}}$ (pin 16)

Chip select input pin. When $\overline{\text{CS}}$ = 0, data and instructions can be transferred to or from the microprocessor and when $\overline{\text{CS}}$ = 1 the data bus is in tristate.

$\overline{\text{RD}}$ (pin 17)

Read control input pin. When $\overline{\text{RD}}$ = 0, read operation is performed. When match conditions for the opcode exist, data is transferred to the microprocessor on the falling edge of $\overline{\text{RD}}$.

$\overline{\text{WR}}$ (pin 18)

Write control input pin. Instructions and opcode from the microprocessor are latched on the rising edge of $\overline{\text{WR}}$ when match conditions exist.

$\overline{\text{SYNC}}$ (pin 19)

Synchronization input pin. When $\overline{\text{SYNC}}$ rises to logic 1, the internal counter is reset so that a new frame can start. The frame format can vary from three channel (three is the minimum number of parties required to form a conference) to thirty two and this number is selected by $\overline{\text{SYNC}}$. When PCM frames of 1544 Kbit/s are used, the rise edge of the $\overline{\text{SYNC}}$ signal must correspond to the Extra bit (193th). In the other case it must correspond to the first bit of the first channel.

CLOCK (pin 20)

Master clock input pin. Max frequency is 4096KHz.

EC (pin 21)

External clock output pin. This pin provides the master clock for the DSM (M088).
Normally is the same signal as applied to CLOCK input (pin 20). When you select, by Instruction 5, Extra bit operating mode, the first two period of the master clock are cancelled, see fig. 8, in order to allow the operation of the M116 and DSM with PCM frame with Extra bit (ex. 193 bit/frame with PCM I/O of 1544 Kbit/s).

IN PCM (pin 22)

PCM input pin. The max bit rate is 2048 Kbit/s. The first bit of the first channel is found with the rising edge of the SYNC signal if operating mode with Extra bit is not inserted. The Extra bit is found with the rising edge of the SYNC signal if operating mode with Extra bit is inserted.

PIN DESCRIPTION (continued)

A/MU (pin 23)

A Law or MU Law select pin. When A/$\overline{MU}$ = 1. A Law is selected. When A/$\overline{MU}$ = 0, MU Law is selected. The law selection must be done before initializing the device using the $\overline{RESET}$ pin.

Figure 2 : Insertion Schema of M116 in a 480 x 480 Non-Blocking Digital Switching Matrix.

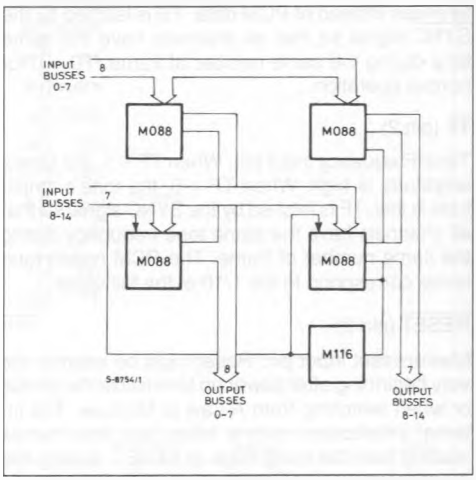
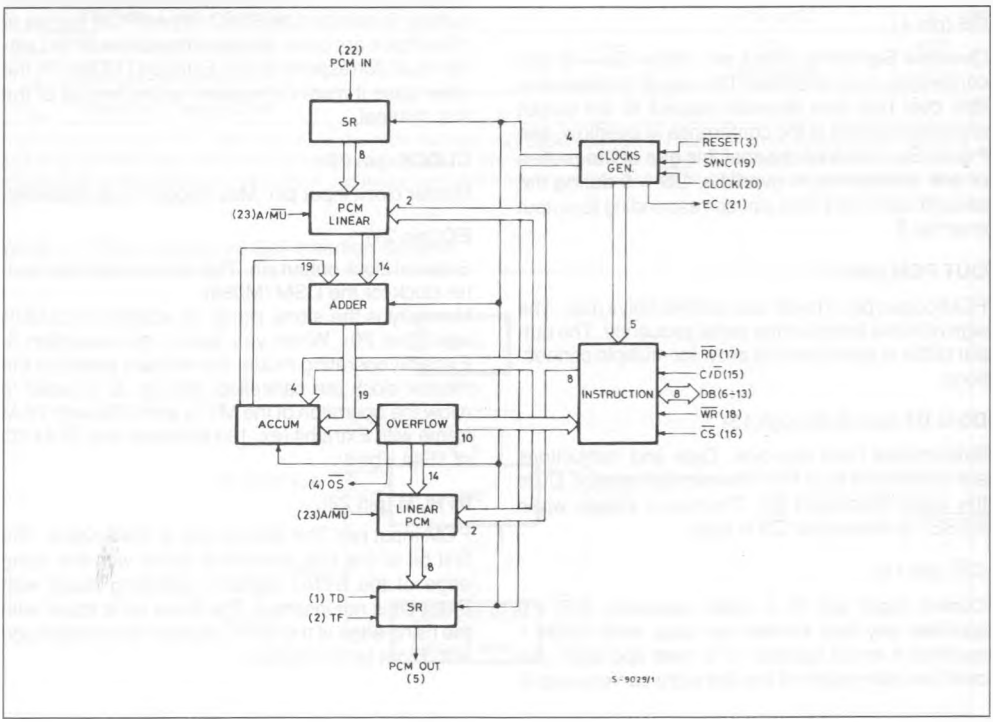


Figure 3 : Block Diagram.



CIRCUIT DESCRIPTION

Through a protocol, the MPU sends the M116 connecting information for each party : the conference number, the conference start bit, the tone insertion enable bit, the number, the attenuation and the noise suppression value for that party.

When a party has to be disconnected the information needed is the disconnection code together with the channel to be disconnected.

The information of channel N, frame M is added during the first half of channel N + 1, frame M and subtracted during the second half of channel N – 1 frame M + 1.

After the Linear to PCM conversion, the subtraction result goes to the parallel-in serial-out Shift Register appearing at the output with one frame plus one channel delay with respect to the corresponding sending information of the specific party.

When many channel are to be conferenced, an attenuation can be desired for each specific party and this is obtained from the PCM to Linear conversion ROM.

If the sum of the channels involved in one conference exceeds the full scale value a saturation appears and the device M116 can signal this overflow condition.

The overflow information, sent out to the databus on MPU request, tells specifically which conference is in overflow at the moment requested.

The number of the channel creating the overflow or in the conference already in overflow, can also be extracted from the $\overline{OS}$ pin, correlating this signal with the $\overline{SYNC}$ signal.

The $\overline{OS}$ signal is low during the second half of a generical output channel slot time N if the channel N belongs to a conference in overflow, see Fig. 9.

This information can be used in the selection of the attenuation value, and the channel to be attenuated. If noise suppression is desired, four threshold are available.

When you insert in a channel belonging to some conference this function, all the PCM output bytes which are related to all the channels belonging to that conference and which are at a level less than the selected threshold, are converted into PCM bytes corresponding to the minimum level.

The four thresholds available correspond to the first, the ninth and the sixteenth step of the first segment, and the sixteenth step of the second segment.

These thresholds correspond respectively to 1/4096, 9/4096, 16/4096, 32/4096 respect to the full scale if A-law is selected and to 1/8159, 9/8159, 16/8159, 32/8159 respect to the full scale is MU-law is selected.

The instruction 5 (operating mode) allows the device M116 to be compatible with any kind of PCM byte format, see table 1, and to work also with PCM frames with Extra bit (ex. 193 bit/frame at 1544 Kbit/s).

The EC pin (External Clock) provides the output clock signal to be applied to the DSM (M088).

This signal is usually the same as the one applied to the input CLOCK pin, only with a little delay (40ns typ.).

When you select, by instructions 5, operating mode with Extra bit, the output clock signal at pin EC has two periods "frozen" in order to allow the DSM (M008) to work also with this king of PCM frame, see fig. 8.

The M116 can also operate in transparent mode. In this case a channel of PCM information can be sent through the M116 and it will appear at the output after one frame (and one channel) delay.

This is useful for a stand/alone system or if the attenuation and noise suppression features are desired without conference.

A tone can be outputted instead of PCM information by using the two tone programming pins (TD/TF).

This tone is a square wave with the same frequency of the signal applied to pin TF, a level corresponding to 1/10 of the full scale value and it is outputed only when pin TD = 1.

Only channels connected in a conference with insertion tone bit (IT) active will have the PCM coded tone at their output.

This feature allows the system to remind the users that they are in conference, or send information of a new party connection and so on.

The chip select pin ($\overline{CS}$) allows several M116 to be connected in parallel on the same databus and access only a particular one.

For testing and diagnostic purposes, a status instruction has been added that provides (for each channel requested) its conference location, the noise suppression threshold level and the attenuation value. This information will appear on the databus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage	0 to 5.25	V
V_O	Off State Output Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	4.096	MHz
$\overline{SYNC}$ Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurements freq. = 1MHz ; T_{op} = 0 to 70°C ; unused pins tied to V_{SS})

Symbol	Parameter	Pins	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	1 to 3 ; 15 to 20 ; 22 to 23			5	pF
$C_{I/O}$	I/O Capacitance	6 to 13			15	pF
C_O	Output Capacitance	4, 5, 21			10	pF

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)
All DC characteristica are valid 250µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level	1 to 3 6 to 13 15 to 20 22 to 23		– 0.3		0.8	V
V_{IH}	Input High Level	1 to 3 6 to 13 15 to 20 22 to 23		2.0		V_{CC}	V
V_{OL}	Output Low Level	4, 6 to 13	I_{OL} = 1.8mA			0.4	V
V_{OH}	Output High Level	4, 6 to 13	I_{OH} = 250µA	2.4			V
V_{OL}	Output Low Level	5, 21	I_{OL} = 5.0mA			0.4	V
I_{IL}	Input Leakage Current	1 to 3 6 to 13 15 to 20 22 to 23	V_{IN} = 0 to V_{CC}			10	µA
I_{OL}	Data Bus Leakage Current	6 to 13	V_{IN} = 0 to V_{CC} $\overline{CS}$ = V_{CC}			± 10	µA
I_{CC}	Supply Current	14	Clock Freq. = 4.096MHz			150	mA

AC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)
All AC characteristics are valid 250µs after V_{CC} and clock have been applied. C_L is the max. capacitive load and R_L the test pull up resistor.

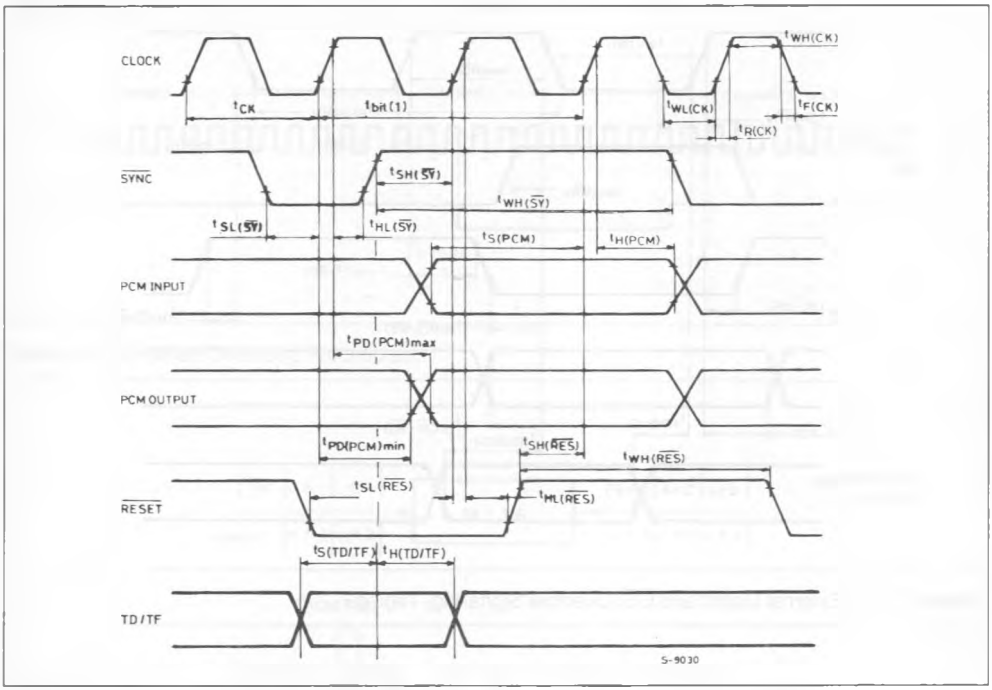
Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock Period		230			ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
$\overline{SYNC}$	t_{SL}	Low Level Set-up Time	See note 1	80			ns
	t_{HL}	Low Level Hold Time		40			ns
	t_{SH}	High Level Set-up Time		80			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input	t_S	Set-up Time		80			ns
	t_H	Hold Time		35			ns
PCM Output	$t_{PD\ min.}$	Propagation time referred to CK low level.	C_L = 50pF R_L = 1KΩ	45			ns
	$t_{PD\ max}$	Propagation time referred to CK high level.	C_L = 50pF R_L = 1KΩ See note 2			180	ns
$\overline{RESET}$	t_{SL}	Low Level Set-up Time		100			ns
	t_{HL}	Low Level Hold Time		50			ns
	t_{SH}	High Level Set-up Time		90			ns
	t_{WH}	High Level Set-up Time		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low Level Width		150			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Repetition interval between active pulses.		500			ns
	t_{SH}	High level set-up time to active read strobe.		0			ns
	t_{HH}	High level hold time from active read strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns
$\overline{RD}$	t_{WL}	Low Level Width		180			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Reception interval between active pulses.		500			ns
	t_{SH}	High level set-up time to active write strobe.		0			ns
	t_{HH}	High level hold time strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns

Notes : 1. With Extra Bit operating mode insert this time become 3 t_{CK}.
2. With Extra Bit operating mode insert these times are 80ns longer.

AC ELECTRICAL CHARACTERISTICS (continued)

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{CS}$	$t_{SL(\overline{CS}\text{-}\overline{WR})}$	Low level set-up time to $\overline{WR}$ falling edge.	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{WR})}$	Low level hold time from $\overline{WR}$ rising edge.	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{WR})}$	High level set-up time to $\overline{WR}$ falling edge.	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{WR})}$	High level hold time from $\overline{WR}$ rising edge.	Inactive Case	0			ns
	$t_{SL(\overline{CS}\text{-}\overline{RD})}$	Low level set-up time to $\overline{RD}$ falling edge.	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{RD})}$	Low level hold time from $\overline{RD}$ rising edge.	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{RD})}$	High level set-up time to $\overline{RD}$ falling edge.	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{RD})}$	High level hold time from $\overline{RD}$ rising edge.	Inactive Case	0			ns
$C/\overline{D}$	$t_{S(C/\overline{D}\text{-}\overline{WR})}$	Set-up time to write strobe end.		130			ns
	$t_{H(C/\overline{D}\text{-}\overline{WR})}$	Hold time from write strobe end.		25			ns
	$t_{S(C/\overline{D}\text{-}\overline{RD})}$	Set-up time to read strobe start.		20			ns
	$t_{H(C/\overline{D}\text{-}\overline{RD})}$	Hold time from read strobe end.		25			ns
$\overline{OS}$	$t_{PD(\overline{OS})}$	Propagation time from rising edge of CK.	C_L = 50pF			100	ns
EC	$t_{PD(EC)}$	Propagation time referred to CK edges.	C_L = 50pF			80	ns
TD/TF	t_S	Set-up		80			ns
	t_H	Hold Time		40			ns
D0 to D7 (interface bus)	$t_{S(BUS\text{-}\overline{WR})}$	Input set-up time to write strobe end.		130			ns
	$t_{H(BUS\text{-}\overline{WR})}$	Input hold time from write strobe end.		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling edge of read strobe.	C_L = 200pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising edge of read strobe to high impedance state.				80	ns

Figure 4 : $\overline{\text{SYNC}}$, PCM I/O, $\overline{\text{RESET}}$, TD/TF Timings.



(1) t_{bit} corresponds to bit 0, channel 0 or Extra Bit.

Figure 5 : WRITE Operating Timing.

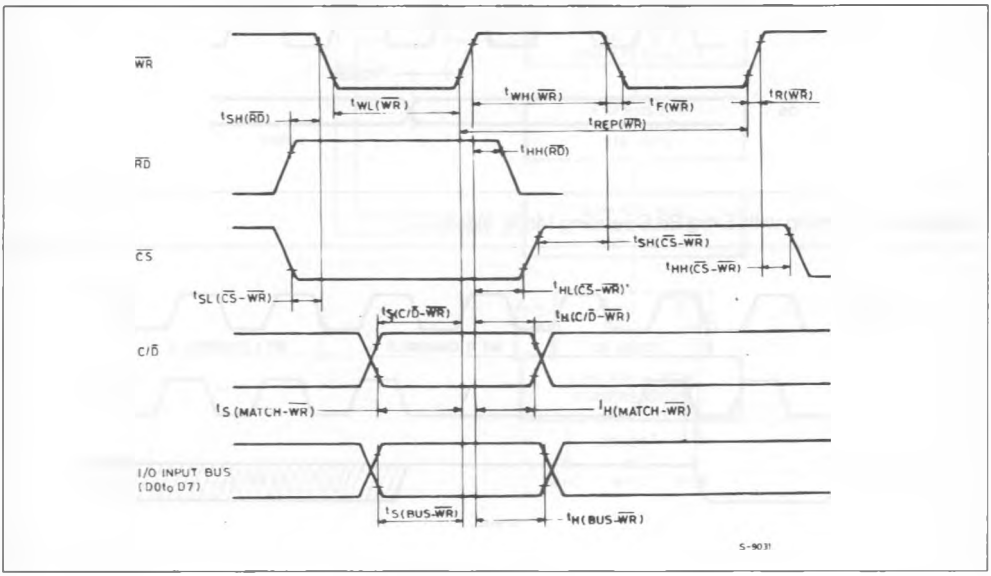


Figure 6 : READ Operating Timing.

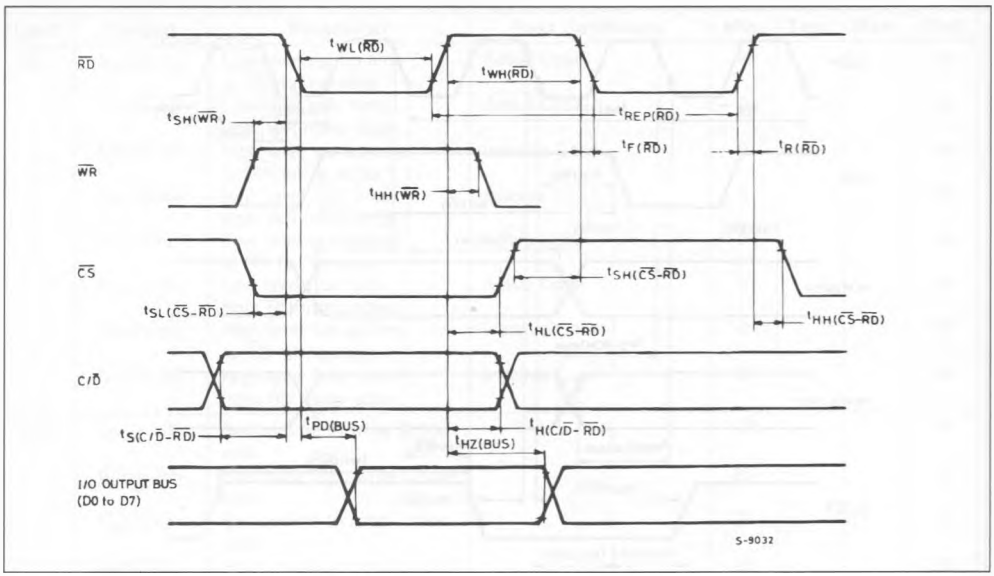


Figure 7 : EC (External Clock) and $\overline{OS}$ (Overflow Signalling) Timings.

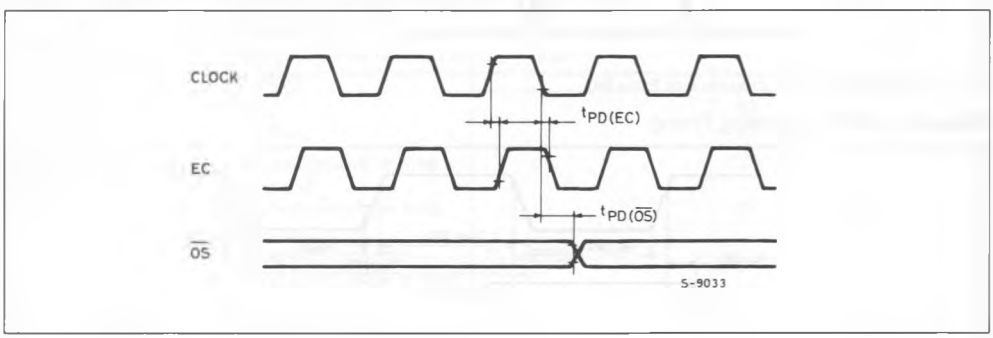


Figure 8 : EC Timing with Extra Bit Operating Mode Insert.

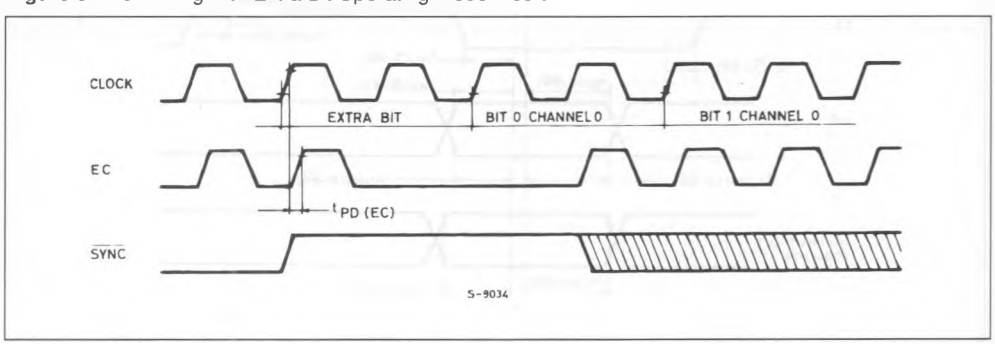


Figure 9 : $\overline{OS}$ Timing with Output PCM Channel (n) belonging to a Conference in Overflow.

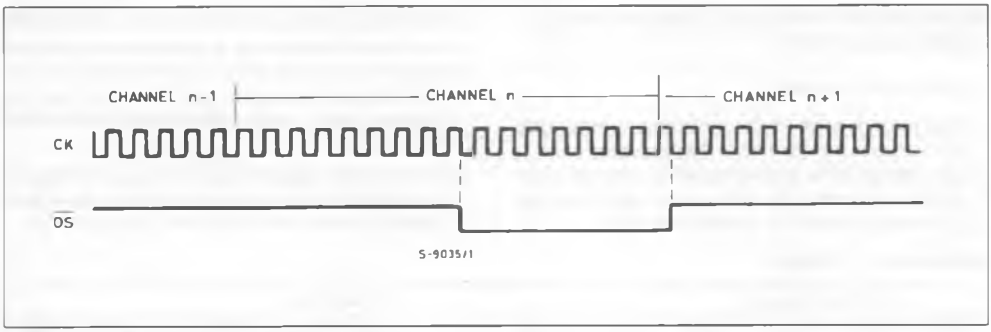
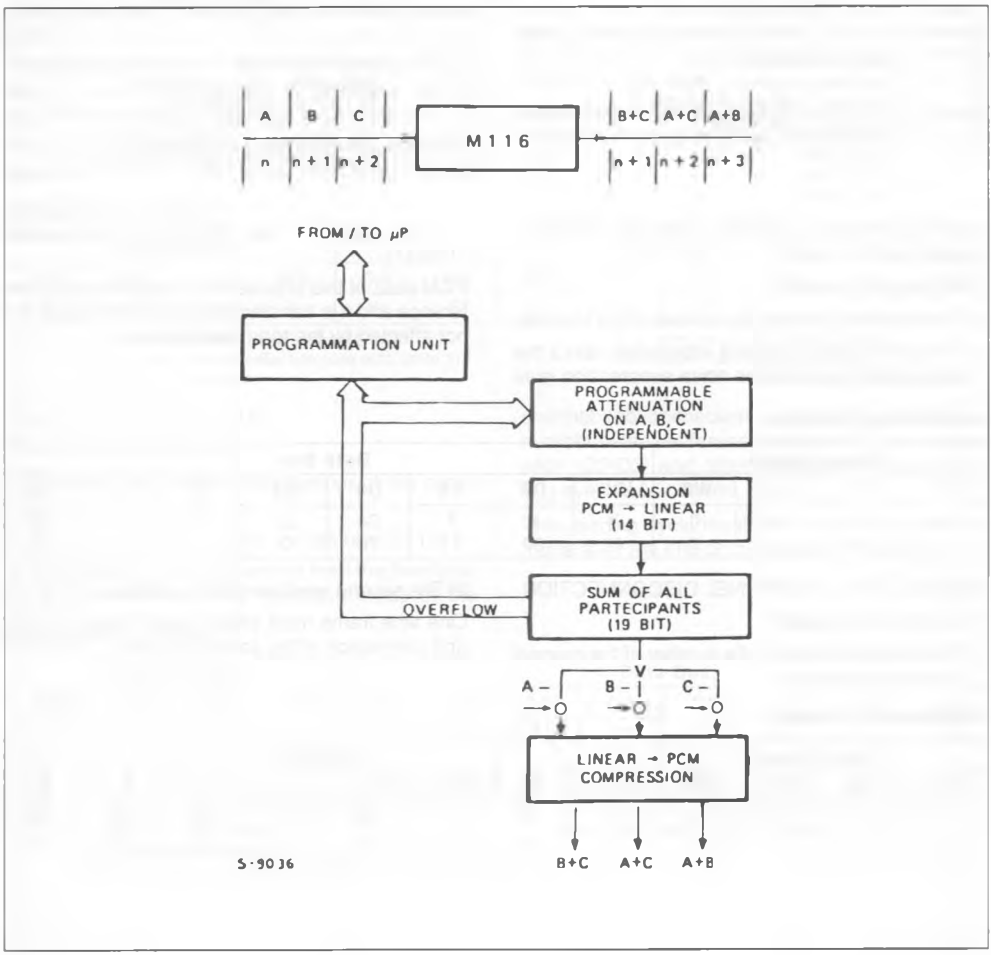


Figure 10 : Simplified Operating Procedures.



INSTRUCTION SET

INSTRUCTION 1 : CHANNEL CONNECTION IN CONFERENCE MODE

Three byte are needed :

1) The first byte contains the conference number (bits D0-D3) and the Start bit S (bit D4). When S = 1, all registers of the conference will be cleared. S = 1 is only required in the instruction 1 set of the first channel connected to a new conference.
2) The second byte contains in the bits (D0-D4) the number of the channel to be connected and the Insert Tone Enable bit IT (D5). When bit IT = 1 all the channels belonging to that conference are enabled using insert tone function if it's active (TD = 1).
3) The third byte contains information about the attenuation level and the noise suppression level to be applied to that channel and the opcode (0111).

Instruction 1 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	S	P3	P2	P1	P0
0	1	0	0	X	X	IT	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	T1	T0	0	1	1	1

S : Conference Start bit
P3 - P0 : Conference number (1-10)
IT : Insertion Tone function enable (IT = 1)
C4 - C0 : Channel number (0-31)
A1 - A0 : Channel attenuation
00 = – 0dB
01 = – 3dB
10 = – 6dB
T1 - T0 : Noise suppression decision value (referred to PCM coding, 128 + 128 steps)
00 = no noise suppression
01 = ninth step, first segment
10 = sixteenth step, first segment
11 = sixteenth step, second segment

INSTRUCTION 2 : CHANNEL CONNECTION IN TRANSPARENT MODE

Two bytes are needed :

1) The first byte contains the number of the channel.
2) The second byte contains information about the attenuation level and the noise suppression level to be applied to that channel and the opcode (0011).

PCM data of this channel is not added to any conference and it is transferred to the PCM output. It is not affected by the tone control pins.

Instruction 2 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	T1	T0	0	0	1	1

INSTRUCTION 3 : CHANNEL DISCONNECTION

Two bytes are needed :

1) The first word contains the number of the channel to be disconnected.
2) The second word contais the opcode (1111).

One time frame must exist between disconnection and connection of the same channel.

Instruction 3 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	1	1	1	1

INSTRUCTION SECTION (continued)

INSTRUCTION 4 : OVERFLOW INFORMATION

Two bytes are needed to know the status of all 10 conferences : C/$\overline{D}$ = 0 reads the first byte (first 8 conferences) and C/$\overline{D}$ = 1 reads the second byte (the last 2 conferences). A conference is in overflow when the corresponding bit is high.

Instruction 4 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1
0	0	1	1	X	X	X	X	X	X	CF10	CF9

CF10 – CF1 : Conference in overflow when high.
nb : as long as $\overline{RD}$ remains low, the overflow status of the conference selected by C/$\overline{D}$ can be monitored in real time.

INSTRUCTION 5 : OPERATING MODE

The single byte needed contains the Extra bit E (D6), the format bits F1-F0 (D5-D4) and the opcode (0101).

The E bit must be E = 1 when the PCM frame contains a number of bit multiple of eight plus one bit (ex. PCM frame at 1544Kbit/s). Normally E = 0.

The bits F1-F0 select the kinds of PCM format byte according table 1. After Reset the default values correspond to F1 = 0, F0 = 1 if A-law is selected and F1 = 1, F0 = 1 if Mu-law is selected.

All channels must be disconnected when the Operating Mode Instruction is sent. They must remain disconnected for at least two time frames after the instruction was sent.

We recommende to use this instruction right after the RESET (see pin $\overline{RESET}$ description).

Instruction 5 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	0	1	0	1

E : Extra bit insertion (active when E = 1)
F1 - F0 : PCM byte Format selection (see also table 1)
00 = no bit inverted
01 = even bit (B0-B2-B4-B6) inverted
10 = odd bit (B1-B3-B5) inverted
11 = all bit (B0-B1-B2-B3-B4-B5-B6) inverted

INSTRUCTION 6 : STATUS

Three bytes are needed :

1) The first byte contains the number of the channel ;

2) The second byte contains the opcode (0110) ;

3) By a reading cycle you extract from the third byte the information about the operating mode of the channel (no connection or transparent mode or number of the conference, bits D4-D7) ; the attenuation (D2-D3) and noise suppression values (D0-D1) eventually inserted.

This reading cycle must be executed at least one frame after the end of the opcode writing cycle.

Instruction 6 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	1	1	0
0	0	1	1	P3	P2	P1	P0	A1	A0	T1	T0

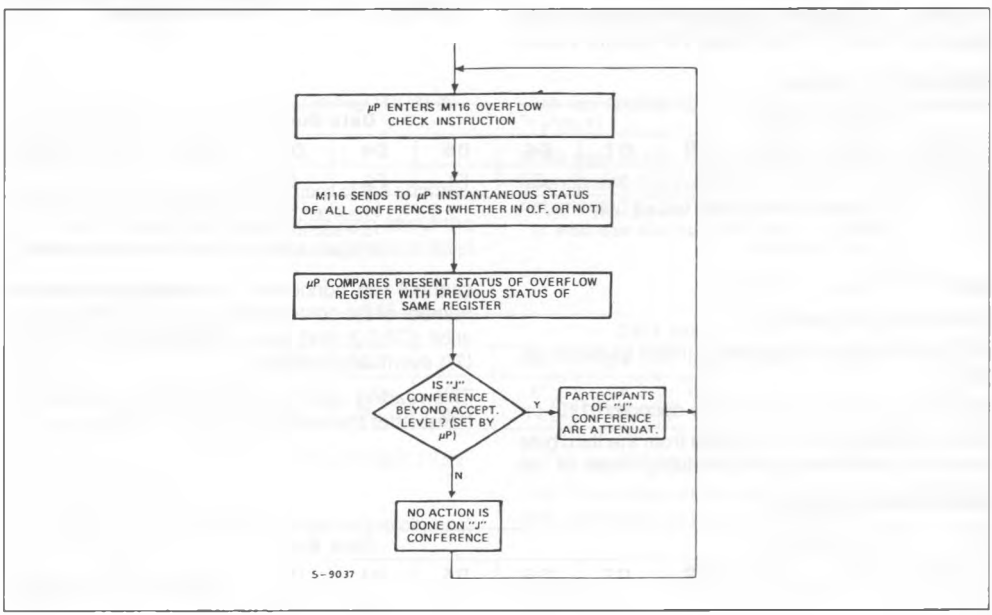
P3 - P0 : channel mode operation information
0000 = no connection
1111 = transparent mode
1010 - 0001 = conference mode,
P3-P0 give the number of the conference.

nb : the Instruction 6 enables the data bus to read the status until reset by C/$\overline{D}$ = 0 and $\overline{WR}$ = 1.

Table 1 : PCM Byte Format. B7 (sign-bit) is the MSB and B0 is the LSB. F1-F0 corresponds to D5-D4 in the byte of the Operating Mode Instruction (instruction 5).

F1	F0		B7	B6	B5	B4	B3	B2	B1	B0
0	0	+ FULL SCALE	1	1	1	1	1	1	1	1
		MIN LEVELS	1	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	0
		– FULL SCALE	0	1	1	1	1	1	1	1
0	1	+ FULL SCALE	1	0	1	0	1	0	1	0
		MIN LEVELS	1	1	0	1	0	1	0	1
			0	1	0	1	0	1	0	1
		– FULL SCALE	0	0	1	0	1	0	1	0
1	0	+ FULL SCALE	1	1	0	1	0	1	0	1
		MIN LEVELS	1	0	1	0	1	0	1	0
			0	0	1	0	1	0	1	0
		– FULL SCALE	0	1	0	1	0	1	0	1
1	1	+ FULL SCALE	1	0	0	0	0	0	0	0
		MIN LEVELS	1	1	1	1	1	1	1	1
			0	1	1	1	1	1	1	1
		– FULL SCALE	0	0	0	0	0	0	0	0

Figure 11 : Overflow Control with µP Interactive Procedure.



SUPPORT MATERIAL AVAILABLE

A) DEMONSTRATION BOARD : Developed to introduce users to the use of the M088 and M116, without building any external hardware but using mnemonic and easy commands through a standard asynchronous terminal. (order code : DEMO-CONF).

B) TECHNICAL NOTE : AN177 and AN299.