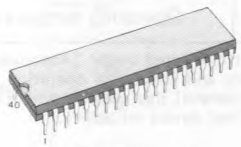
SGS-THOMSON MICROELECTRONICS

M114S

DIGITAL SOUND GENERATOR

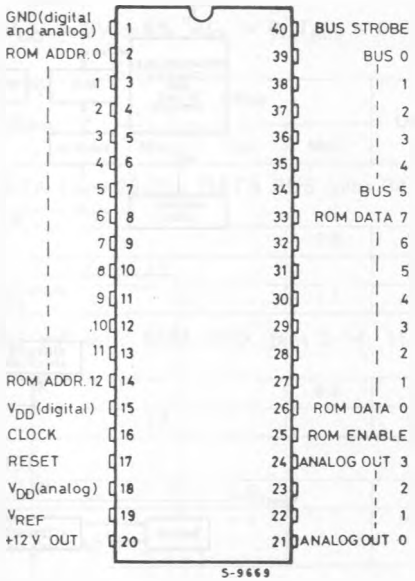
- SOUND GENERATED BY READING TABLES CODED IN DELTA CODING OR IN ABSOLUTE VALUES SITUATED IN AN INTERNAL MEMORY OF 16K MAX.
- 16 INDEPENDENT CHANNELS
- 12 BIT EQUIVALENT D/A CONVERTER RESOLUTION (DELTA CODING)
- 8 DIFFERENT TABLE LENGTHS AND 8 READING MODES GIVING A TOTAL OF 58 DISTINCT COMBINATIONS
- 16 DIFFERENT MIXABLE LAYERS BETWEEN TWO SEPARATE TABLES
- MULTIPLE READING PERMITS INTERPOLATION BETWEEN TWO ADJOINING SAMPLES ON THE SAME TABLE
- 4 SELECTABLE ANALOG OUTPUTS
- 10 BIT INTERNAL ATTENUATOR WITH GRADUAL AMPLITUDE VARIATION
- ROM ENABLE OUTPUT TO MINIMISE EXTERNAL MEMORY POWER CONSUMPTION
- POSSIBILITY OF SYNCHRONOUS AND ASYNCHRONOUS FREQUENCY-TABLE CHANGE AT THE END OF THE READING TABLE



DIP-40 Plastic

ORDERING NUMBER: M114S

CONNECTION DIAGRAM



The M114S is a 16 channel digital polyphonic, politimbric sound generator.

The M114S must be driven by a microprocessor and needs an external memory.

With this device it is possible to synthesize a large range of sound by simply transcribing the most significant periods of the sound to be reproduced into an external memory and programming a suitable reading sequence for these periods with the use of a microprocessor.

The M114S is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology and is assembled in plastic DIP.40.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 7	V
V_I	Input voltage	-0.3 to V_{DD}	V
V_O	Output voltage	-0.3 to V_{DD}	V
P_{tot}	Total package power dissipation	800	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 - Block Diagram

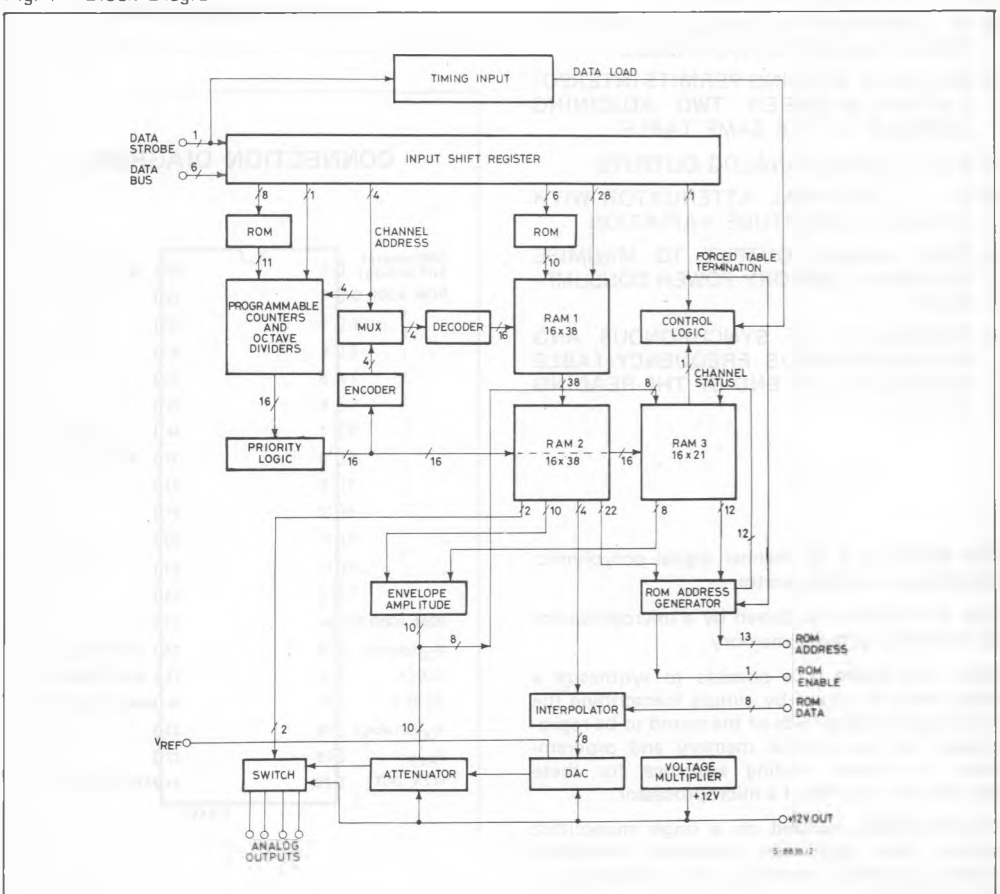
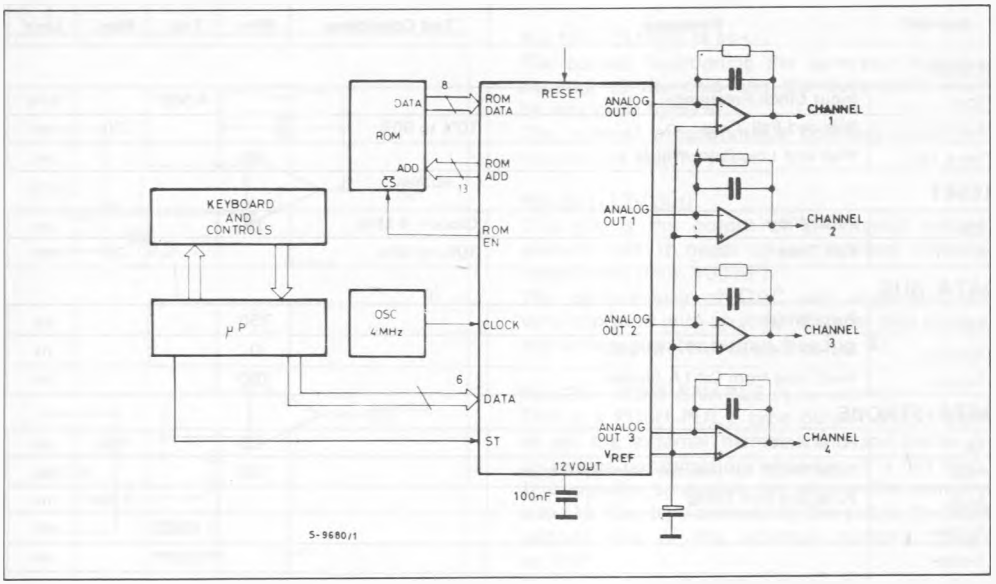


Fig. 2 - System Configuration



STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 5%, V_{SS} = 0, T_{amb} = 0/70°C, V_{DD} DIG = V_{DD} Analog)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
INPUTS: RESET (pin 17), CLOCK (pin 16), ROM DATA (pins 26-33), DATA BUS (pins 34-39), DATA ST. (pin 40)						
V_{IL}	Low Input Level				0.8	V
V_{IH}	High Input Level		2.2			V
I_I	Input Leakage Current	$V_I = V_{DD}$ to V_{SS}			± 1	μA
DIGITAL OUTPUTS (HIGH IMPEDANCE* with 10KΩ pull-up): ROM-ADD (pins 2-14; 11-17) ROM-EN (pin 25)						
V_{OL}	Low Output Level	I_{OL} = 1mA			0.4	V
V_{OH}	High Output Level	I_{OH} = 100μA	2.4			V
ANALOG OUTPUTS: (pins 21, 22, 23, 24), V_{REF} (pin 19)						
V_{REF}	Voltage Reference Output	I_O = ± 1mA		2.5		V
I_O	Output Current (current generator)	Zero attenuation Max input code to the DAC		± 1		mA
POWER DISSIPATION						
I_{DD}	Supply Current	V_{DD} = 5.25V			120	mA

* High impedance means that, when the addresses are off, the digital output is connected with an internal resistive pull-up.

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLOCK						
t_{CK}	Input Clock Frequency			4.000		KHz
t_r, t_f	Rise and Fall Time	10% to 90%			20	ns
t_{WH}, t_{WL}	High and Low Pulse Width		80			ns
RESET						
t_W	Pulse Width	Clock = 4 MHz	10			µs
t_f	Fall Time	10% to 90%			20	ns
DATA BUS						
t_W	Pulse Width		750			ns
t_{set-up}	Set-up Time to DATA Strobe		0			ns
t_{hold}	Hold time from DATA Strobe		750			ns
DATA STROBE						
t_W	Pulse width		1.5		128	µs
t_{WR}	Pulse Width for Internal Reset generation		128			µs
t_f, t_r	Pulse and Fall Times				100	ns
t_{LOW}				600		ns
t_{HIGH}				350		ns
t_{set-up}(*)	Set-up Time ROM-EN		70			ns

(*) t_{set-up} time means that the data coming from ext. ROM must be stable at least 70 nsec before the rising edge of ROM-EN.

PIN FUNCTIONS

PIN 1 – GND (Analog and Digital)
Analog ground and digital ground are both linked to this pin.

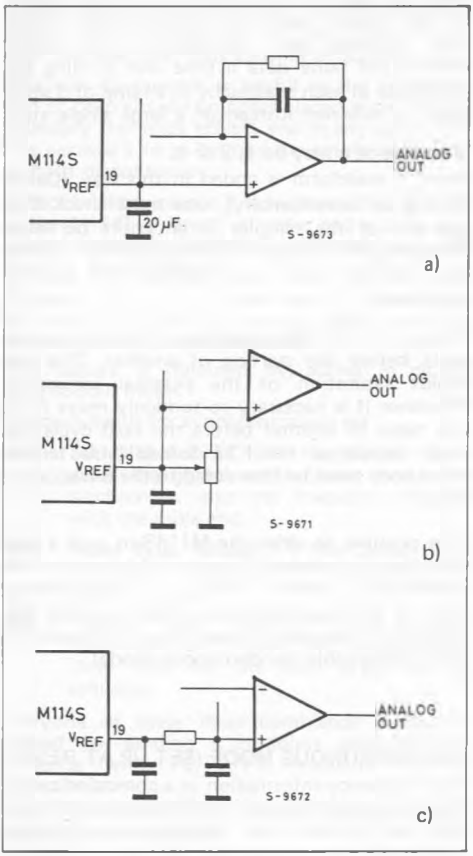
Pins 21-24 – Analog Outputs
These outputs are under current with an output impedance of approximately 1 KΩ and the filter or external integrator must have a low input impedance. This means that the voltage drop between output pin and V_{REF} must be negligeable so as to obtain a good signal linearity.
An integrator together with a low pass filter are necessary if the tables have been "DELTA" coded. If on the other hand they have been coded in absolute values then only a low pass filter is needed.
If the channels do not have to be separated for stereophonic effects or otherwise, a single output may be used routing, by µP programming, all channels to this pin.

Pin 19 – Voltage Reference Output (V_{REF})
V_{REF} is the average value of the DAC output. With V_{supply} = 5V V_{REF} is nominally 2.5V but could vary by chip to chip (~10mV).

It's only necessary to filter the V_{REF} output with an external capacitor of some tens of µF (Fig. 3a). To get a voltage suitable to act as V_{REF} towards external integrator which reconstruct the output signal. Since such a voltage is quite the same than DAC output for a null input code, it automatically conforms itself, following possible differencies between various device instances. It is possible to modify slightly, from the external environment, the obtained V_{REF} value with suitable resistive networks so that the operational integrator offset can be compensated. (Fig. 3b) To improve the V_{REF} it's possible to use a filter as in Fig. 3c.

PIN FUNCTIONS (continued)

Fig. 3.



Pin 18 – Analog Power Supply
The power supply for all analog parts, i.e. DAC, attenuator, etc...., are linked to this pin.
It is therefore important that this power supply should be very stable and well smoothed.
The internal power supply chip separation allows a great improvement of signal/noise ratio.

Pin 15 – Digital Power Supply

The power supply for all digital parts, i.e. counters, memories, etc...., are linked to this pin.

Pin 17 – RESET
All channels are reset by raising this pin and the 13 external ROM address outputs together with the 4 sound outputs are placed in a high impedance state.

Pin 16 – CLOCK (4 MHz)
For correct functioning the generator must be external to the chip and the duty cycle must be very close to 50%.
The internal programmable counters switch on the positive leading edge.

Pin 20 (+12V out)
This pin is the output of an internal voltage elevator and it needs of an external filtering capacitance (min. 100 nF).
The performance of DAC and attenuator are very improved with an external zener that clamps the voltage elevator output (see Fig. 4).

Pins 25 – ROM-ENABLE (Low active)
This is a PUSH-PULL type output and is used to set the external memory in stand-by so as to reduce consumption whenever it is not read. It is possible to double the addressable memory size (16 Kbyte by connecting this pin to the MSB address line of the external memory trough an F/F.

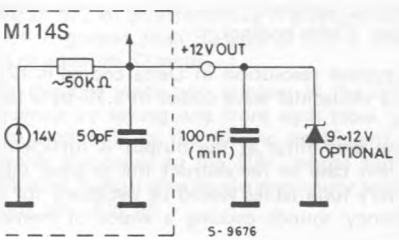
Pins 26 & 33 – ROM-DATA
8 input pins for data from external memory.

Pins 2 & 14 – ROM-ADDRESS
13 PUSH-PULL type output pins for external memory address.

Pins 34-39 – DATA-BUS
6 input pins for data from the microprocessor. 8 of these data groups make up a complete piece of information.

Pin 40 – DATA-BUS Strobe
A signal from the microprocessor must arrive at this input in order to memorise the present code onto the DATA-BUS.
Memorization occurs on both edges.

Fig. 4



GENERAL DESCRIPTION

The M114S is a device that allows digital sound synthesis.

The essential system needed consists of a microprocessor, an M114S and an external memory with a maximum of 8192 bytes.

Sound generation is based on cyclic reading of a table corresponding to a waveform of the timbre to be reproduced.

As the waveform and therefore also the spectrum frequently change, a series of tables of form and frequency appropriate to the sound are cyclically scanned during sound reproduction.

The effect caused by the sudden passage from one table to the next would be unpleasant unless there is such a large number of tables to allow a smooth unnoticeable change from one table to the following.

A favourable compromise between number of tables and quality of sound, that has been implemented in the M114S is the following: A limited number of tables which may even diverge from one another are chosen during an initial phase of analysis after which, during the reproduction phase, two adjoining tables are read simultaneously by extracting a percentage of one and the remaining percentage of the other.

Therefore by starting with 100% of one and zero of the other and successively increasing the second while decreasing the first, so that the sum of the percentages is always equal to 100, there will come a point at which there is a 100% of the second and zero of the first thus having achieved a smooth passage from one table to the next. In the M114S this passage is made up of a maximum of 16 steps.

The tables are stored in an external memory and may be of eight different lengths ranging from 16 to 2048 bytes. The M114S can handle up to a maximum of 16Kbytes (see fig. 8).

The tables may be coded using waveform's absolute value or by the difference between adjoining samples, that is, in a incremental manner (Delta coding).

The typical resolution in Delta coding is 12 bit with a sinusoidal wave coded in a 16-byte table.

A low pass filter at the output is sufficient in the first case to reconstruct the original signal, but very long tables would be necessary for low frequency sounds causing a waste of memory.

With the use of an integrator at the output in the second case, the waveforms are coded thus allowing easy interpolation. By simply reading the same data n time and dividing the amplitude of each reading by n, a ramp of n small steps is obtained instead of a large single step.

The value of n may be 1, 2 or 4.

When a waveform is coded in this way (Delta-Coding or incrementally), one must check that the sum of the samples in an entire period is always equal to zero or there would be a continuity which could even saturate the external integrator.

Always the M114S completes the reading of a table before the starting of another. This too avoids saturation of the external integrator. Whenever it is necessary to suddenly move from one table to another before the read cycle has been completed the FTT forced table termination code must be forwarded to the 8 frequency bits.

It is possible to drive the M114S in such a way that the programmed frequency becomes active immediately, without waiting for the running table to end (asynchronous mode); or that this change of frequency occurs only at the end of the running table (synchrounous-mode).

ASYNCHRONOUS MODE (SET UP AT RESET)

The frequency-information in a command causes the immediate change of the frequency, while the table and all the other parameters are changed only when the running table has been completely scanned.

This type of operation is useful for producing vibrato effects on long tables or vibrato effects on low frequency sounds.

In fact in these cases it is useful to be able to vary continuously the scanning frequency of the same table, without being bound to execute the variation of frequency at the end of the table.

SYNCHRONOUS MODE

The frequency-information in a command causes the synchronous change of table and frequency; this is obtained by delaying the frequency change until the running table has been completely scanned.

GENERAL DESCRIPTION (continued)

This command is very useful in some special effects (glide) because it avoids the reading of the table in part with the old frequency and in part with the new one, thus causing an audible click.

This way-to-operate is useful in the reproduction of deep vibrato on notes placed at the octave boundary, for glide effects and in any case when it is necessary to go beyond the octave boundary without discontinuity.

In fact in these causes it is necessary to schedule in the M114S a length of table and a table frequency scanning completely different from the previous programming.

To avoid clicks it is indispensable to finish the old table with the old frequency before starting the new one with new frequency.

The feature is obtained by acting in global synchronous mode.

The commands for synchronization are:

SSG **Set Global Sync.** (FB Hex Code). Activates the global synchronous mode i.e. sinchronize, also the frequency change with the table end.

RSG **Reset Sync. Global** (F9 Hex Code). This command disables global synchronous mode.

RSS **Reverse Sync. Status** (FA Hex Code). This command inverts the synchronism state only for the next programming sequence.

Everyone of these three commands is accomplished by sending a complete programming sequence with F9/FA/FB frequency codes, respectively.

They affect the whole working mode of the device (all its channels).

All the remaining bits are ignored.

Note that the **RSS** command can be obtained by sending eight times the 6-bit data 111110.

As shown in Tab. 3, there are six bit among the control bits that are dedicated to the choice of table pair length and n number of repeated readings of each table.

The frequency of sample readings is synchronous.

This means that the frequency is a whole multiple of the table length.

In this way any problem caused by intermodulation is eliminated but a noise due to "collision" is produced. As there is a single output circuit for all channels, that is interpolator, D/A converter, attenuator, ecc., each time more than one channel requires access to this circuit one or more other channels must wait.

The amount of time necessary for the output circuit to process each table, that is the period of time for which each channel uses the circuit during each sample reading cycle, is of 2μs. The delay will therefore be proportional to the number of channels operating simultaneously and to the frequency that they are generating. As these parameters casually vary, so will the delay thus producing a casual alteration of the original waveform.

Simulation has proved that under worst possible conditions the signal/noise ratio due to this problem is around 60dB.

In conclusion let us mention the envelope that has to be controlled by the microprocessor which, at suitable intervals, must forward the desired attenuation coefficient.

There are 64 possible attenuations each with steps of approximately 0.75dB;
These passage from one level to another may be immediate or to gradual increments of 1/256 of the maximum amplitude at a frequency proportional to external table reading frequency.

OPERATION

The M114S receives from the μP a single programming sequence at a time. This programming sequence is made up of 48 bits.

The μP must send a 48 bit set for every M114S active channel.

Each M114S channel continuously generates the same signal, that is it reads the same table, with the same mixing coefficient, with the same amplitude, ecc., until the microprocessor forwards a different programming sequence (variation of one or more parameters characterising the sound to be generated within a single channel.

Timbre amplitude evolution and any other slight frequency changes must be handled in real-time by the microprocessor.

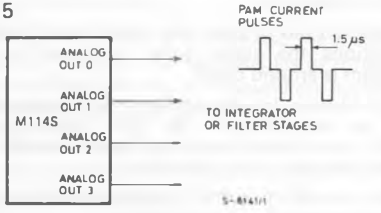
Often the microprocessor is unable to update the amplitude with sufficient speed. For this reason the M114S carries out a gradual change from one amplitude to another at steps of 1/256 of maximum sample frequency amplitude if the change in level is greater than 128 steps, of 1/2 of this frequency if greater than 64, of 1/4 if greater than 32 and of 1/8 if smaller than or equal to 32 steps.

Each channel reads two samples at the sample frequency by taking one from each table, sums them according to the mixing coefficient and forwards the result to the DAC whose suitably attenuated output goes to the previously selected output pin (Fig. 5).

GENERAL DESCRIPTION (continued)

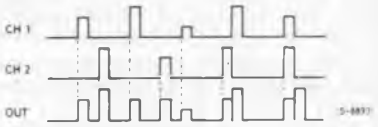
This operation requires 2μs and as there is a single output circuit for all channels it is certain that one or more channels will simultaneously request the use of the circuit. Thus a priority order has been assigned to each channel. This order is fixed, channel zero being that of greatest priority followed in order by the others.

Fig. 5



When more than one channel is simultaneously active at the output pin there will be an overlap of impulse sequence of each channel.
The example of Fig. 6 shows an output signal with 2 active channels, CH1 has greater priority then CH2:

Fig. 6



The signal will change from impulsive to continuous by passing through:

- a low pass filter if the table have been coded using absolute values.
- an integrator if in delta coding

PROGRAMMING

48 bits subdivided into 8 groups of 6 bits each must be forwarded in order to programme a channel.
A group of 6 bits is memorised on every Data Strobe switch front. As the data bus is read approximately 250ns after transition from the Data Strobe, the 6 data bits may simultaneously arrive with the Delta Strobe switch.

DATA PROGRAMMING ORDER

N. PIN / BYTE	34	35	36	37	38	39
1st	ATTENUATION					
	A5	A4	A3	A2	A1	A0
2nd	4 OUTPUTS		TABLE 1 ADDRESS		TABLE 2 ADDRESS	
	1	0	7	6	7	6
3rd	TABLE 2 ADDRESS					
	5	4	3	2	1	0
4th	TABLE 1 ADDRESS					
	5	4	3	2	1	0
5th	TABLE LENGTH			READING METHOD		
	L2	L1	L0	M2	M1	M0
6th	INTERPOLATION				IMMEDIATE CONNECTION	OCTAVE DIVISOR
	3	2	1	0	0	0
7th	CHANNEL NUMBER				FREQUENCY	
	3	2	1	0	1	0
8th	FREQUENCY					
	7	6	5	4	3	2

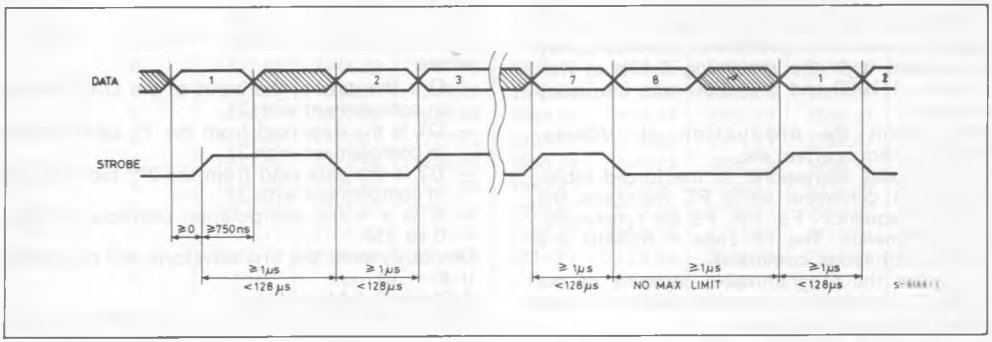
GENERAL DESCRIPTION (continued)

The graph of fig. 7shows the time lapse that must be assigned to these signal for correct functioning.

No more than 128μs must pass between one Data Strobe transition and the next during transmission of the 8 groups of data or else synchronisation is lost due to the internal automatic reset generated after 128μs from the last Data Strobe transition, causing the data to be misinterpreted.

One should wait for at least 9μs after the forced-zero-cross command has been given between the last group of data of one instruction and the first group of the next.

Fig. 7



The degree of priority of the channel and the number of channels in use at that moment must be taken into account in order to shorten this wait, If there is maximum priority the wait will be a minimum wait of approximately 2μs. The same holds if the priority is not maximum but there are no other channels in use. There will however be a maximum wait of 2μs for each active channel with greater priority than the channel in question.

If another instruction were to be transmitted without a sufficient wait, there would be the risk of losing the previous instruction of forced table termination.

The wait is unnecessary after normal commands.

Every data group must be remain present for at least 1μs after Data Strobe transition.
The 48 bit functions are the following:

A) 8 address bits for the 1st table (ext. ROM)
B) 8 address bits for the 2nd table (ext ROM)
C) 8 frequency bits (4-note and 4-twelfths of note and ± 1 or 2/1000)
D) 6 attenuation or amplitude address bits
E) 4 interpolation bits
F) 4 channel address bits
G) 6 reading mode and table length bits (ext. ROM)
H) 2 bits for choice between four outputs
I) 1 bit for a frequency octave change
J) 1 bit for gradual disable of envelope

While waiting for the present 1st table reading to terminate, the above data (not immediately operational) is memorized into the internal RAM1).

The new data is transfered to RAM2 and becomes operational when the addressed channel ends the current table scanning.

An exception is made by the 8 frequency bits and the one varying the frequency octave as they operate immediately (See synchronization).

All data may be made operational by giving the forced-table-termination command.

48 PROGRAMMING BIT FOR CHANNEL SELECTION

8 Address Bits 1st Table (ext. ROM)
These determine the most significant part of the 13 external memory address bits but according to the table length chosen by the 6 mode bits, some of the least significant of these 8 bits are suitably substituted by the M114S.

In the case of a maximum table length, 2048 bytes, there will only be 2 significant bits to address the table while the remaining 11 will address each single table word.

By already knowing the table length, the programmer will be able to programme the most significant bits needed for table address only and ignore the others.

As the maximum memory that can be handled is of 8Kbytes, if the table has a length of 1Kbyte it is sufficient to program the 3 MSB bits and ignore the other five.

48 PROGRAMMING BIT FOR CHANNEL SELECTION (continued)

8 Address Bits 2nd Table (ext. ROM))
As above but refering to the second table.
One must consider that the forced table termination refers to the first table and that during table mixing the second table may assume a percentage value of zero while the first table can only assume a minimum percentage value of 1/16 of the maximum value.

8 Frequency Bits
The 4 most significant bits characterize one of the 15 available notes with HEX. Codes from 0 to E. Eleven movements in twelfths of a semitone may be obtained with the remaining 4 bits as well as four ± 1/1000 and ± 2/1000 note frequency variations.
These permit the production of: Vibrato, Glissando, chorus effect etc.....
The FF codes correspond to the forced-table-termination command while FC maintains the previous frequency. F9, FA, FB are synchronisation commands. The F8 code = ROMID is a ROM identification command.
It just sets the programmable counters of the M114S to a very short counting modulo (8 + 0) useless for musical purposes.
The remaining codes are used for testing and therefore must not be used by the operator. Table 1 shows the 240 frequencies obtainable by setting the external clock to 4MHz and the table length to 16 bytes, with single reading and without inserting an octave divisor. These are the highest octave frequencies obtainable with the M114S.
In practice double, quadruple, etc . . . frequencies may be obtained by writing 2, 4, etc. complete waveform periods in the table.

6 Attenuation Bits
These are the addresses for the internal attenuation table.
The contents of this table follow a logarithmic pattern so as to produce a decrease of 0.75dB for each address unit increment. See table 2. The word length is of 10 bits.
After processing by a suitable circuit in order to obtain a gradual amplitude variation the ten outputs of this table are linked to the 10 bit attenuator.
The gradual movement from the present level to that just programmed takes place by increasing or decreasing the 8 most significant bits of the attenuation table contents, with the same frequency with which the external memory tables are being scanned if the difference in level is greater than 128 steps, or with 1/2 of this frequency if greater than 64 steps or 1/4 if greater than 32, or 1/8 if smaller than or equal to 32.

In conclusion, the output signal amplitude increases of decreases at each variation by 1/256 of the maximum value.
By setting the bit that deals with the gradual envelope there is an immediate passage from the present level to that programmed.

4 Interpolation Bits
These define the mixing coefficient between the two waveform tables.
It is possible in this way to sum the 1st waveform percentage with the remaining 2nd waveform percentage thus obtaining a third signal which will be forward to the output.
In greater detail, the operation carried out is the following:

$$D = (D1 * (K + 1)/16) + (D2 * (15 - K)/16)$$

where :
- D is the data at the input of the DAC (8 bits in complement with 2)
- D1 is the data read from the 1st table (8 bits in complement with 2)
- D2 is the data read from the 2nd table (8 bits in complement with 2)
- K is a 4 bit interpolation coefficient (from 0 to 15)

Obviously only the first waveform will be output if K = 15.

4 Channel Address Bits
These indicate to which of the 16 M114S channel the remaining 44 bits will be forwarded.

6 Mode Bits
These indicate the table couple reading mode (ext. ROM).
For each table there are 58 distinct combinations that include, both table lengths and the number of repeated readings from the same address. (ext ROM). See table n. 3.
The three most significant bits characterize the table lengths while the other three characterise the length ratio between tables and the number of repeated readings.

2 Output Address Bits
These indicate to which of the 4 output pins the corresponding channel signal must be forwarded. This is necessary in order to obtain stereophonic effect or to separate channels used for accompanyment from those of "SOLO", etc. . .

1 Octave Divisor Bit
This is used to pass from one octave to another without changing the table length. If octave divisor bit is set to 1 the programming frequency is divided by two.

1 Instant ENVELOPE Change Bit
This orders instant passage from the present amplitude to that programmed.

TABLE 1 – FREQUENCIES

NOTE	DEVIATION	-6/12	-5/12	-4/12	-3/12	-2/12	-1/12	-2/1000	-1/1000
	(Hex)	0	1	2	3	4	5	6	7
C	0	1016.78	1021.45	1026.69	1031.46	1036.27	1041.67	1044.39	1045.48
C#	1	1077.01	1082.25	1087.55	1092.90	1098.30	1103.14	1106.81	1107.42
D	2	1140.90	1146.79	1152.07	1158.08	1163.47	1168.91	1172.33	1173.71
D#	3	1209.19	1215.07	1221.00	1226.99	1232.29	1238.39	1242.24	1243.78
E	4	1281.23	1287.00	1293.66	1299.55	1305.48	1312.34	1315.79	1317.52
F	5	1356.85	1363.33	1369.86	1376.46	1383.13	1389.85	1393.73	1395.67
F#	6	1437.81	1445.09	1451.38	1458.79	1466.28	1472.75	1478.20	1479.29
G	7	1523.23	1530.22	1538.46	1545.60	1552.80	1560.06	1564.95	1566.17
G#	8	1614.21	1622.06	1629.99	1638.00	1644.74	1652.89	1658.37	1659.75
A	9	1709.40	1718.21	1727.12	1734.61	1743.68	1751.31	1757.47	1759.01
A#	A	1811.59	1819.84	1829.83	1838.24	1846.72	1855.29	1860.47	1862.20
B	B	1919.39	1928.64	1937.98	1947.42	1956.95	1966.57	1972.39	1974.33
2C	C	2032.52	2042.90	2053.39	2063.98	2072.54	2083.33	2087.68	2089.86
2C#	D	2155.17	2164.50	2176.28	2185.79	2195.39	2207.51	2212.39	2214.84
2D	E	2283.11	2293.58	2304.15	2314.81	2325.58	2339.18	2344.67	2347.42
	F	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing	For Testing

NOTE	DEVIATION	0	+1/1000	+2/1000	+1/12	+2/12	+3/12	+4/12	+5/12
	(Hex)	8	9	A	B	C	D	E	F
C	0	1046.57	1047.67	1048.77	1051.52	1056.52	1061.57	1066.67	1071.81
C#	1	1108.65	1109.88	1111.11	1114.21	1119.19	1124.86	1130.58	1135.72
D	2	1174.40	1175.78	1177.16	1180.64	1186.24	1191.90	1197.60	1203.37
D#	3	1244.56	1245.33	1246.88	1250.78	1256.28	1262.63	1269.04	1274.70
E	4	1318.39	1319.26	1321.00	1324.50	1331.56	1337.79	1344.09	1350.44
F	5	1396.65	1397.62	1398.60	1403.51	1410.44	1417.43	1424.50	1430.62
F#	6	1480.38	1481.48	1482.58	1486.99	1494.77	1501.50	1508.30	1516.30
G	7	1567.40	1568.63	1569.86	1576.04	1583.53	1591.09	1598.72	1606.43
G#	8	1661.13	1662.51	1663.89	1669.45	1677.85	1684.92	1693.48	1702.13
A	9	1760.56	1762.11	1763.89	1768.35	1777.78	1785.71	1793.72	1803.43
A#	A	1863.93	1865.67	1867.41	1874.41	1883.24	1892.15	1901.14	1910.22
B	B	1976.28	1978.24	1980.20	1984.13	1994.02	2004.01	2014.10	2024.29
2C	C	2092.05	2094.24	2096.44	2103.05	2114.16	2123.14	2134.47	2143.62
2C#	D	2217.29	2219.76	2222.22	2227.17	2239.64	2249.72	2259.89	2272.73
2D	E	2350.18	2352.94	2355.71	2361.28	2372.48	2383.79	2395.21	2406.74
	F	ROMID	SSG	RSS	RSG	Previously Selected Frequency	For Testing	For Testing	Forced Table Terminat.

TABLE 2 – ATTENUATION

N = six bit attenuation code decimal value (0 : 63)
V = internally decoded linear ten bit value (0 : 1023)
A = theoretical attenuation value in decibels = 20 • Log ((V + 1)/1024)

N	V	A
0	1023	0.00
1	939	0.74
2	863	1.48
3	791	2.23
4	727	2.96
5	667	3.71
6	611	4.47
7	559	5.24
8	515	5.95
9	471	6.73
10	431	7.50
11	395	8.25
12	363	8.98
13	335	9.68
14	307	10.43
15	283	11.14
16	259	11.91
17	235	12.75
18	215	13.52
19	199	14.19
20	183	14.91
21	166	15.75
22	152	16.51
23	140	17.22
24	128	17.99
25	117	18.77
26	107	19.54
27	98	20.29
28	90	21.03
29	83	21.72
30	76	22.48
31	69	23.30

N	V	A
32	64	23.95
33	58	24.79
34	53	25.56
35	49	26.23
36	45	26.95
37	41	27.74
38	37	28.61
39	34	29.32
40	31	30.10
41	28	30.96
42	26	31.58
43	24	32.25
44	22	32.97
45	20	33.76
46	18	34.63
47	16	35.60
48	14	36.68
49	13	37.28
50	12	37.93
51	11	38.62
52	10	39.38
53	9	40.21
54	8	41.12
55	7	42.14
56	6	43.30
57	5	44.64
58	4	46.23
59	3	48.16
60	2	50.66
61	1	54.19
62	0	60.21
63	0	60.21 + STOP

TABLE 3 - READING MODES

MODE		LENGTH		READ N.	
M	L	T1	T2	T1	T2
000	000	16	16	2	2
000	001	32	32	2	2
000	010	64	64	2	2
000	011	128	128	2	2
000	100	256	256	2	2
000	101	512	512	2	2
000	110	1024	1024	2	2
000	111	2048	1048	2	2
001	000	16	16	1	1
001	001	32	32	1	1
001	010	64	64	1	1
001	011	128	128	1	1
001	100	256	256	1	1
001	101	512	512	1	1
001	110	1024	1024	1	1
001	111	2048	2048	1	1
010	000	16	16	4	4
010	001	32	32	4	4
010	010	64	64	4	4
010	011	128	128	4	4
010	100	256	256	4	4
010	101	512	512	4	4
010	110	1024	1024	4	4
010	111	1024*	1024	4	4
011	000	16	16$	1	1
011	001	32	16	1	1
011	010	64	32	1	1
011	011	128	64	1	1
011	100	256	128	1	1
011	101	512	256	1	1
011	110	1024	512	1	1
011	111	2048	1024	1	1

MODE		LENGTH		READ N.	
M	L	T1	T2	T1	T2
100	000	16	8	1	2
100	001	32	16	1	2
100	010	64	32	1	2
100	011	128	64	1	2
100	100	256	128	1	2
100	101	512	256	1	2
100	110	1024	512	1	2
100	111	2048	1024	1	2
101	000	16	16$	1	1
101	001	32	16$	1	1
101	010	64	16	1	1
101	011	128	32	1	1
101	100	256	64	1	1
101	101	512	128	1	1
101	110	1024	256	1	1
101	111	2048	512	1	1
110	000	16	4	1	4
110	001	32	8	1	4
110	010	64	16	1	4
110	011	128	32	1	4
110	100	256	64	1	4
110	101	512	128	1	4
110	110	1024	256	1	4
110	111	2048	512	1	4
111	000	16	16$	1	1
111	001	32	16$	1	1
111	010	64	16$	1	1
111	011	128	16	1	1
111	100	256	32	1	1
111	101	512	64	1	1
111	110	1024	128	1	1
111	111	2048	256	1	1

* Repetitions
$ Exceptions

Fig. 8 - The M114S can handle up to 16Kbyte of memory with this application circuit.