MOS INTEGRATED CIRCUIT

M 090

ADVANCE DATA

A - LAW SINGLE CHANNEL PCM CODEC

- ± 5V SUPPLY
- FOLLOWS CCITT A-LAW COMPANDING CODE
- EXCEEDS CCITT SPECIFICATIONS
- INDEPENDENT RECEIVE AND TRANSMIT SECTIONS
- FULLY ASYNCHRONOUS
- ON-CHIP AUTOZERO
- LOW EXTERNAL COMPONENT COUNT
- SEPARATE ANALOG AND DIGITAL GROUNDS
- SINGLE 16-PIN PACKAGE
- TTL COMPATIBLE

The M090 is a monolithic N-channel silicon-gate PCM CODEC (coder-decoder) which performs analog-to-digital conversion (coding) and digital-to-analog conversion (decoding) using the A-Law companding code. It is intended for use as a per-channel voice frequency CODEC in telephone systems but features completely independent ADC and DAC sections to permit asynchronous transmission/reception. Transmission and reception is in form of 8 bit words at a data rate up to 2.048M bits/sec using audio sampling at 8 KHz. Capacitive network AD and DA converters are used to ensure high long term stability and immunity to temperature variations. The maximum power consumption is 90 mW (70 mW typ). The M090 is available in a 16-lead dual in-line plastic and ceramic package.

ABSOLUTE MAXIMUM RATINGS*

$V+$**	Positive supply voltage	+7.5	V
$V-$	Negative supply voltage	-7.5	V
V_{DI}	Digital inputs	-0.3 to 10	V
V_{AI}	Analog inputs	$V- \leqslant V_I \leqslant V+$	V
$+V_{ref}$	Positive reference voltage	$-0.3 \leqslant V_I \leqslant V+$	V
$-V_{ref}$	Negative reference voltage	$V- \leqslant V_I \leqslant 0.3$	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-55 to 125	°C

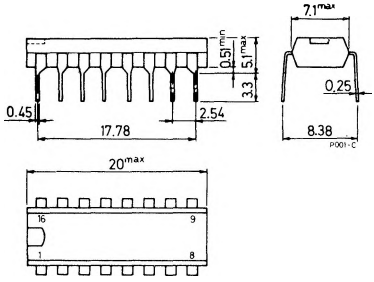
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** With respect to Analog or Digital ground.

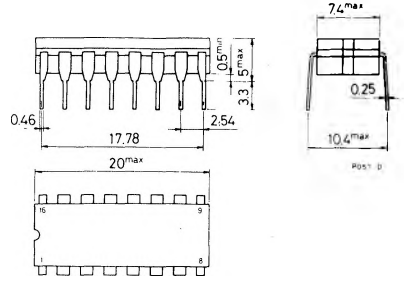
ORDERING NUMBERS: M090 B1 for dual-in-line plastic package
M090 F1 for dual-in-line ceramic package (frit seal)

MECHANICAL DATA (dimensions in mm)

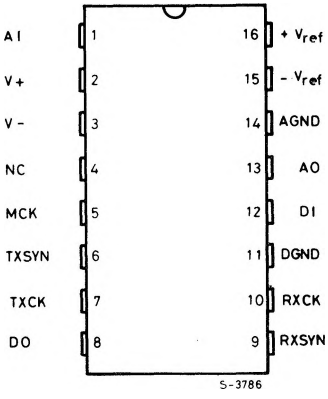
Dual in-line plastic package



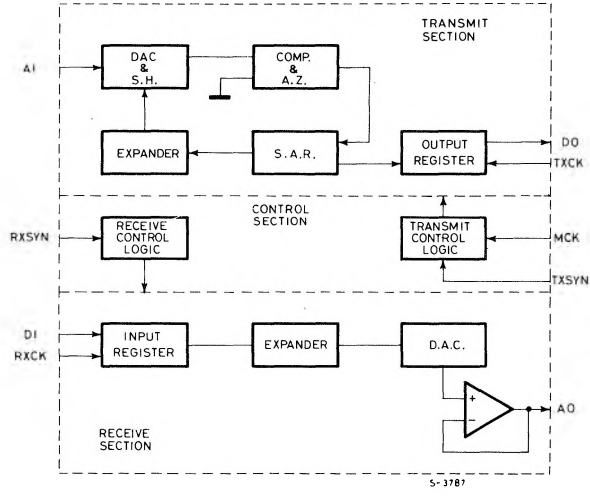
Dual in-line ceramic package, frit seal



PIN CONNECTIONS



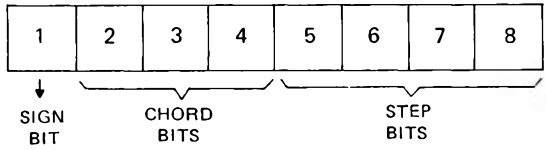
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Data word format

The eight bit words used for transmission and reception consist of a sign bit and seven magnitude bits. The magnitude bits are further divided into three chord bits and four step bits. The sign bit, which indicates the polarity of the analog signal, is the first to be transmitted and is thus the first to be received. The division of the seven magnitude into chord and step bits is to obtain higher ADC resolution at low (analog) signal levels. The analog value of each step bit is doubled for each successive chord, i.e. for the first two chords the step bit value is 1.2 mV; for the third chord the step value is 2.4 mV; for the fourth, 4.8 mV etc.



Analog Input (AI), pin 1

The audio signal supplied to this input is sampled at 8 kHz and coded. The input level on this pin must always be between $+V_{ref}$ and $-V_{ref}$.

Master Clock (MCK), pin 5

The Master Clock is used to time conversion operations and is completely independent of the transmit and receive clocks (TXCK and RXCK).

Transmit Sync (TXSYN), pin 6

This input enables the transmission output register. The TXSYN signal is synchronised to the transmit clock and lasts eight TXCK periods.

Transmit Clock (TXCK), pin 7

This determines the transmission rate and may be up to 2.1 MHz.
Each of the eight bits in the output register is transmitted when the logic AND of TXSYN and TXCK is true.

Digital Output (DO), pin 8

The eight bit word stored in the transmission register is shifted out via the Digital Output by TXCK when TXSYNC is high. When TXSYNC is low this output is in the high impedance condition..
The M090 also provides inversion of the even bits (bits 2, 4, 6, 8).

Receive Sync (RXSYN), pin 9

This input is synchronised with the receive clock and lasts eight RXCK periods, enabling the PCM input to the receive register.

Receive Clock (RXCK), pin 10

Each of the 8 bits of the input word is loaded by the receive clock when RXSYNC is high. RXCK may be completely asynchronous with the transmit clock.

FUNCTIONAL DESCRIPTION (continued)

Digital Input (DI), pin 12

The eight bit receive register is loaded via the Digital Input.

Analog Ground and Digital Ground (AGND, DGND), pins 14, 11

Separate grounding pins are provided for the digital and analog parts of the circuit to prevent signal degradation. The same criteria should be applied during the design of the P.C. board on which CODEC and filters are mounted.

Analog Output (AO), pin 13

The PCM word loaded into the input register is transferred to the DAC for conversion to the analog signal. This signal, in the form of 100% duty cycle voltage steps, reaches the Analog Output via a low impedance buffer. A low-pass filter must be connected to this output to recreate the voice signal.

Reference Voltages ($+V_{ref}$, $-V_{ref}$), pins 16, 15

The D/A converter reference voltages are connected to these pins. The difference between the absolute values of $+V_{ref}$ and $-V_{ref}$ must be less than 1%.

ELECTRICAL CHARACTERISTICS (All parameters are tested at $T_{amb}=25°C$, $V^+=5V$, $V^-=5V$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Note
STATIC ELECTRICAL CHARACTERISTICS							
V^+	Positive supply voltage		4.75	5.0	5.25	V	
V^-	Negative supply voltage		-5.25	-5.0	-4.75	V	
$+V_{ref}$	Positive reference voltage		2.375	2.5	2.625	V	
$-V_{ref}$	Negative reference voltage		-2.625	-2.5	-2.375	V	
R_{IS}	AI resist. during sampling			200		Ω	
R_{INS}	AI resistance non sampling			10		MΩ	
R_O	AO resistance			50		Ω	
V_{OH}	Digital output	I_{OH}= 5 mA	4.5			V	
V_{OL}	Digital output	I_{OL}= 5 mA			0.5	V	
V_{IH}	Pins 5, 6, 7, 9, 10		2			V	
V_{IL}	Pins 5. 6. 7. 9. 10				0.8	V	
I^+	Positive supply current			9	11	mA	
I^-	Negative supply current			5	7	mA	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Note
DYNAMIC ELECTRICAL CHARACTERISTICS (see Fig. 1)							
t_{WS}	TXSYN, RXSYN width			8/FX(FR)		µs	
t_{XCS}	TXCK to TXSYN delay		25		1/FX-80	ns	1
t_{SDON}	DO to TSYN on delay				90	ns	2
t_{SDOFF}	DO to TXSYN off delay				70	ns	2
t_{CDXH}	DO high to TXCK delay				200	ns	2
t_{CDXL}	DO low to TXCK delay				180	ns	2
t_{DOR}	DO rise time			40		ns	2
t_{DOF}	DO fall time			20		ns	2
t_{SRC}	RSYN to RXCK delay		50		1/FR-50	ns	1
t_{CDRS}	DI to RXCK set up time		10			ns	
t_{CDRH}	DI to RXCK hold time		60			ns	
t_{SAO}	AO to RXSYN delay	for sample n - 1		800		ns	
t_{RC}	Clock rise time				50	ns	
t_{FC}	Clock fall time				50	ns	
M_{CKF}	MCK frequency				2.1	MHz	
FX, FR	TXCK, RXCK, frequency		0.064		2.1	MHz	
CK D.C.	TXCK, RXCK duty cycle		40	50	60	%	
$SLEW^+$	AO positive slew rate				5	V/µs	
$SLEW^-$	AO negative slew rate				5	V/µs	
SYSTEM CHARACTERISTICS (see Fig. 2 and 3)							
S/Q	Total distortion	AI = -1 dBm 0		30		dB	3
		AI = -15 dBm 0		38		dB	3
		AI = -34 dBm 0		35		dB	
		AI = -50 dBm 0		20		dB	3
ΔG/G	Gain traking	AI = +3 dBm 0		0		dB	4
		AI = -20 dBm 0		0		dB	4
		AI = -50 dBm 0		±0.15		dB	4
		AI = -55 dBm 0		±0.2		dB	4
	Idle channel noise			-80	-74	dBmOp	

Note: 1) FR and FX are expressed in Hz.
2) Driving one 74 LS TTL load plus 30 pF.
3) The signal at the analog input is a pseudorandom noise (350 ÷ 550 Hz).
4) The signal at analog input is a 840 Hz sinewave.

Fig. 1 - Transmit and receive sections

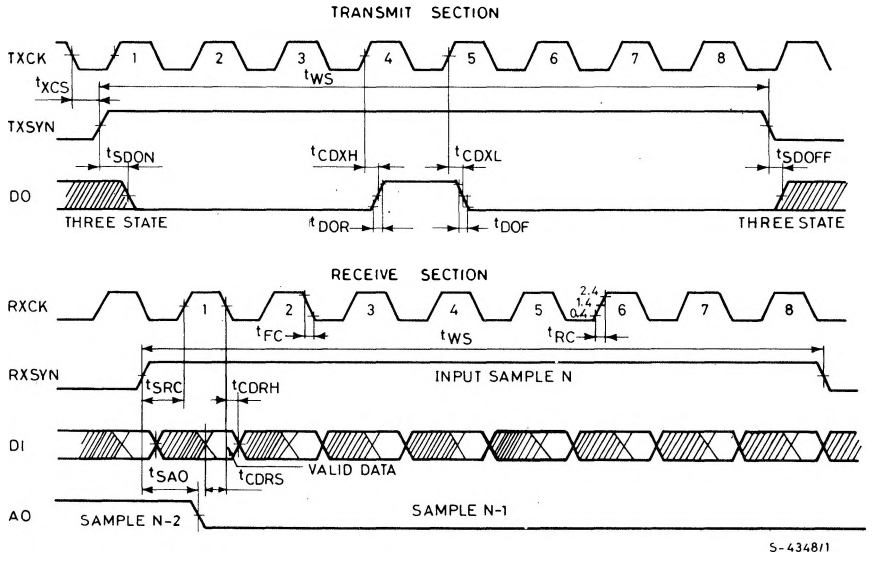


Fig. 2 - S/Q ratio vs. input level.

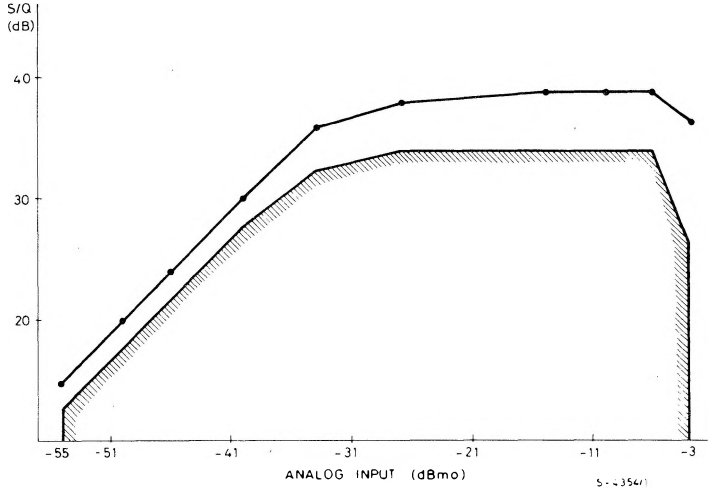


Fig. 3 - Gain tracking performance