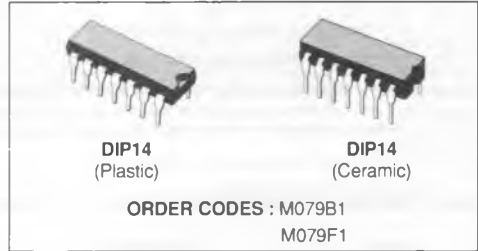


N-CHANNEL 2 x 2 x 2 CROSSPOINT SWITCH WITH CONTROL MEMORY

- LOW ON RESISTANCE : 18Ω
- INTERNAL CONTROL LATCHES
- 5.5V_{PP} ANALOG SIGNAL CAPABILITY
- LESS THAN 1% TOTAL DISTORTION AT 0dbm
- LESS THAN - 90db CROSS-TALK AT 1.6KHZ
2V_{rms}



DESCRIPTION

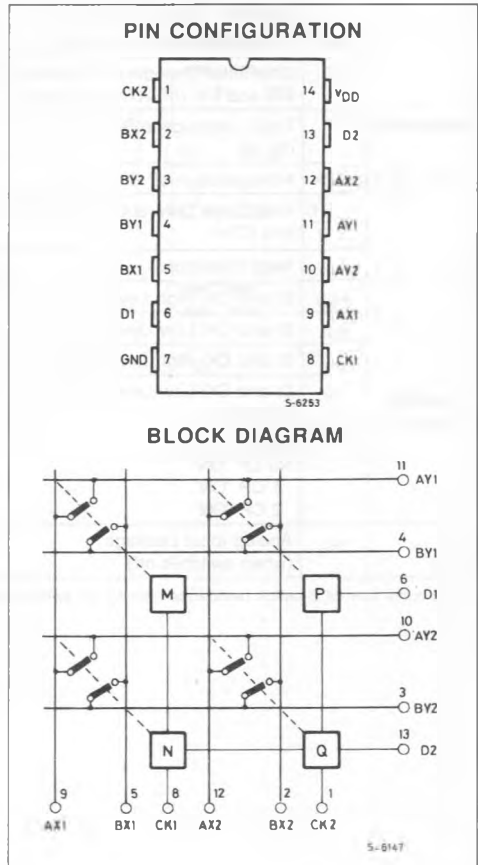
The M079 consists of a 2 x 2 x 2 crosspoint array and 4 memory cells. Connection between two paths is determined by the status of the corresponding memory elements. If the latch is ON the paths are connected, if OFF disconnected.

Every memory configuration can be set by writing the two D inputs using the two clocks. "1" on D determines the ON status and 0 the OFF status. The clock enters the Data input, on the high level. The correspondent switch is influenced at once. Data is then latched on falling edge of CK input. Thus storage is defined when CK goes down (see fig. 6, 7). CK and D levels are TTL compatible. The power on reset puts the memory elements into OFF status disconnecting the switches.

The M079 is available in 14 pin dual in-line plastic and ceramic packages.

TRUTH TABLE

Logic Input	Analog Connections Involved				Memory Status
D1 D2 CK1 CK2	AX1	BX1	AY1	BY1	
1 X 1 0	AX1	BX1	AY1	BY1	M on
0 X 1 0	AX1	BX1	AY1	BY1	M off
X 1 1 0	AX1	BX1	AY2	BY2	N on
X 0 1 0	AX1	BX1	AY2	BY2	N off
1 X 0 1	AX2	BX2	AY1	BY1	P on
0 X 0 1	AX2	BX2	AY1	BY1	P off
X 1 0 1	AX2	BX2	AY2	BY2	Q on
X 0 0 1	AX2	BX2	AY2	BY2	Q off



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.5 to 14	V
V_i	Input Voltage Range (CK1, CK2, D1, D2)	$V_{DD} + 0.5$	V
V_{IN}, V_{OUT}	Differential Voltage between the Two Ends of every Crosspoint in "OFF" Status	14	V
P_{tot}	Power Dissipation	600	mW
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	- 55 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress ratings only and functional operation of the the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions to extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, V_{DD} at $12\text{V} \pm 5\%$, $V_{EE} = 3\text{V}$)

Symbol	Parameter	Test Conditions*	Min.	Typ.	Max.	Unit
Crosspoint	αN	(cross talk) Diaphony Attenuation between Each Couple (fig. 2)	$V_{IN} = 2V_{rms}$ 1.6KHz	90		dB
	αN	Longitudinal Attenuation (fig. 3)	$V_{IN} = 2V_{rms}$ 1.6KHz		0.15	dB
	RD	Differential Impedance between AXi and BXi (on AYm an BYm)	$V_{IN} = 2V_{rms}$ 1.6KHz	200		K Ω
	RT	Total Longitudinal Resistance* (fig. 3)			18	Ω
	CP	Attenuation in off Status	$V_{IN} = 2V_{rms}$ 1.6KHz	100		dB
	$\Delta \frac{RT}{2}$	Resistance Difference Related to one CP			1	Ω
		Total Distortion	$V_{IN} = 0\text{dBm}$ 1.6KHz		1	%
Control Logic	V_{INH}	Di and CKi High Level Input		2.4		V
	V_{INL}	Di and CKi Low Level Input			0.8	V
	I_{INH}	Di and CKi High Level Input	$V_{CK} = 2.7\text{V}$ $V_D = 2.7\text{V}$		1	μA
	I_{INL}	Di and CKi Low Level Input Current	$V_{CK} = 0.4\text{V}$ $V_D = 0.4\text{V}$		1	μA
	I_{DD}	Supply Current : NO CP "ON" 1 CP "ON" 2 CP "ON"			3 2.5 2	 mA mA
I_{AL}	Analog Input Leakage (when switches off)	$V_{IN} = 0$ to 12V			1	μA

* This is the sum of 2-switch resistance : the single switch is tested at 9Ω and its typical value is 5Ω .

AC CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $V_{DD} = 12\text{V}$)

Symbol	Parameter	Refer to Figure	Min.	Typ.	Max.	Unit
f	Clock	fig. 5			0.7	MHz
t	Turn-on	fig. 6		300	500	ns
t	Turn-off	fig. 6		330	700	ns
t _S	Setup	fig. 7	300			ns
t _H	Hold	fig. 7	300			ns
t _w	Clock Pulse Width		300			ns

Supply voltage must rise in more than 5ms.

Figure 2 : Cross Talk Measurement.

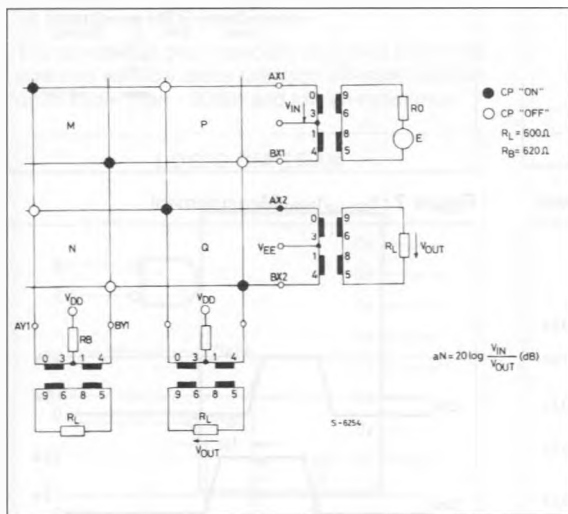


Figure 3 : Equivalent Circuit of an Activated Phonic Connection.

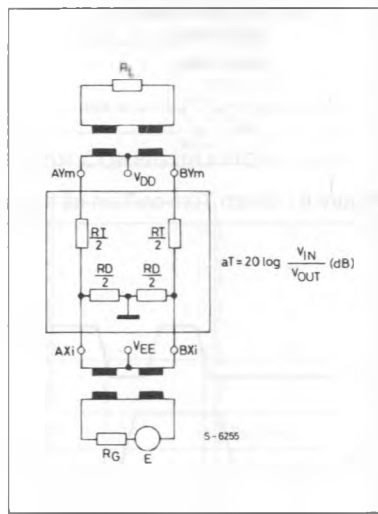


Figure 4 : Equivalent Circuit in Unactivated Phonic Connection.

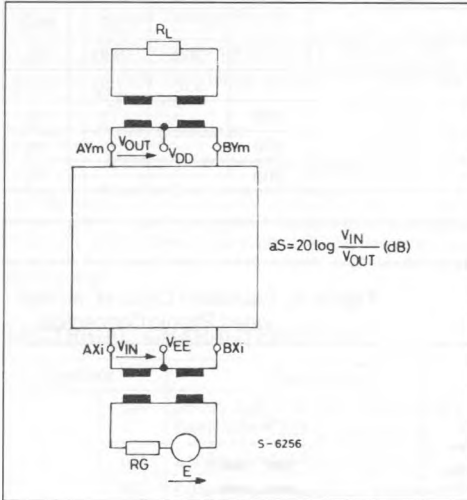


Figure 5 : Circuit for Turn-on/Turn-off Measurement.

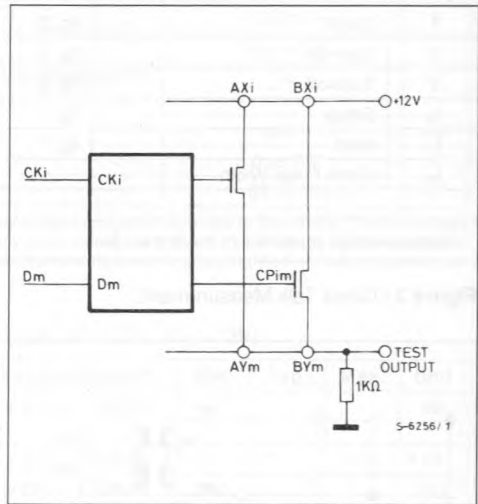


Figure 6 : Switch Turn-on/Turn-off Measurement.

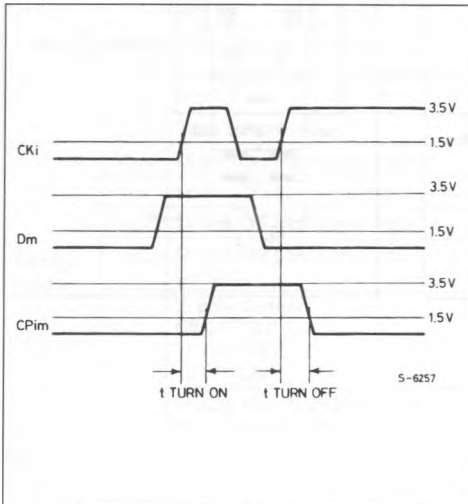


Figure 7 : t_{set-up}/t_{Hold} Measurement.

