SGS-THOMSON MICROELECTRONICS

M044

128 X 128 DIGITAL SWITCHING MATRIX

- 128 INPUT AND 128 OUTPUT CHANNEL DIGITAL SWITCHING MATRIX (non blocking)
- TYPICAL APPLICATION IN PABX
- PCM INPUTS AND OUTPUTS MATUALLY COMPATIBLE
- ACTUAL INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA AN ON-CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- 5 MAIN "FUNCTIONS" or "INSTRUCTIONS" AVAILABLE
- TYPICAL BIT RATE : 2Mbit/s
- TYPICAL SYNCHRONIZATION RATE : 8 KHz (time frame is 125 µs)
- 5 VOLT POWER SUPPLY WITH INTERNALLY GENERATED BIAS VOLTAGE
- MOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- DIFFUSED WITH ST N-CHANNEL SILICON GATE HIGH DENSITY MOS PROCESS

Main instruction controlled by the microprocessor interface

- CHANNEL CONNECTION/DISCONNECTION
- CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CONTROL WORD

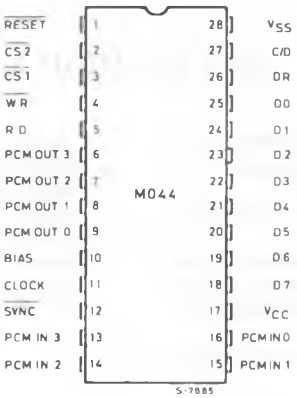
DIP28
(Ceramic)

ORDER CODE : M044F1

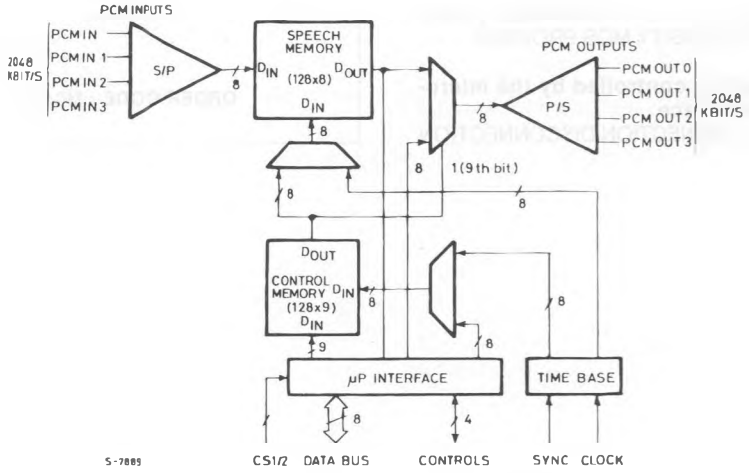
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7	V
V_I	Input Voltage	– 0.3 to 7	V
V_O	Off State Output Voltage	7	V
P_{tot}	Total Package Power Dissipation	1.5	W
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

PIN CONNECTION



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage	0 to 5.25	V
V_O	Off State Input Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	4.096	MHz
$\overline{\text{SYNC}}$ Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurements freq. = 1 MHz ; T_{op} = 0 to 70 °C ; unused pins tied to V_{SS})

Symbol	Parameter	Pins	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	6 to 15 ; 26 to 30 ; 32 to 36			5	pf
$C_{I/O}$	I/O Capacitance	20 to 24			15	pf
C_O	Output Capacitance	1 to 4 ; 17 to 19 ; 25 ; 37 to 40			10	pf

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C, V_{CC} = 5 V ± 5 %)
All DC characteristics are valid 250 µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{ILC}	Clock Input Low Level	6		– 0.3		0.8	V
V_{IHC}	Clock Input High Level	6		3.0		V_{CC}	V
V_{IL}	Input Low Level	7 to 15 20 to 24 26 to 30 32 to 36		– 0.3		0.8	V
V_{IH}	Input High Level	7 to 15 20 to 24 26 to 30 32 to 36		2.0		V_{CC}	V
V_{OL}	Output Low Level	17 to 25	I_{OL} = 1.8 mA			0.4	V
V_{OH}	Output High Level	17 to 25	I_{OH} = 250 µA	2.4			V
V_{OL}	PCM Output Low Level	1 to 4 37 to 40	I_{OL} = 2.0 mA			0.4	V
I_{IL}	Input Leakage Current	6 to 15 26 to 30 32 to 36	V_{IN} = 0 to V_{CC}			10	µA
I_{OL}	Data Bus Leakage Current	17 to 24	V_{IN} = 0 to V_{CC} V_{CC} applied ; Pins 35 and 36 tied to V_{CC}. After device Initialization			± 10	µA
I_{CC}	Supply Current	16	Clock Freq. = 4.096 MHz		170		mA

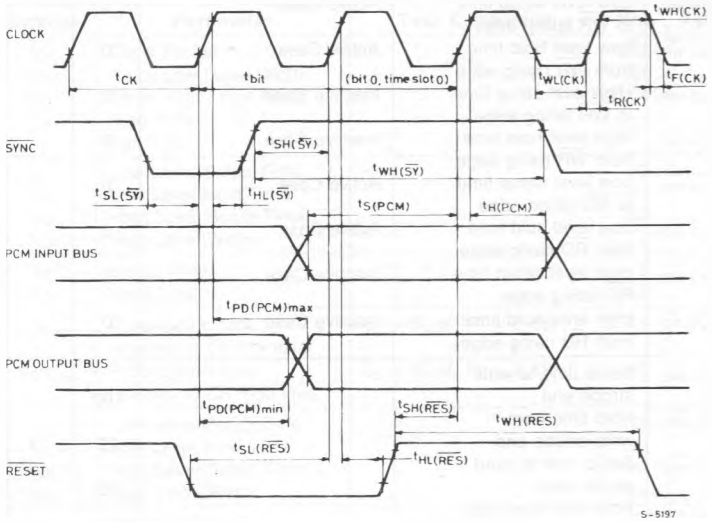
AC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C, V_{CC} = 5 V ± 5 %)
All AC characteristics are valid 250 µs after V_{CC} and clock have been applied. C_L is the max capacitive load and R_L the test pull up resistor.

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock Period		230			ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
$\overline{SYNC}$	t_{SL}	Low Level Setup Time		80			ns
	t_{HL}	Low Level Hold Time		40			ns
	t_{SH}	High Level Setup Time		80			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input Busses	t_S	Setup Time		− 5			ns
	t_H	Hold Time		45			ns
PCM Output Busses	$t_{PO\ min}$	Propagation time referred to CK low level	C_L = 50 pf, R_L = 2 KΩ	45		180	ns
	$t_{PO\ max}$	Propagation time referred to CK high level	C_L = 50 pf, R_L = 2 KΩ	45		200	ns
$\overline{RESET}$	t_{SL}	Low Level Setup Time		100			ns
	t_{HL}	Low Level Hold Time		50			ns
	t_{SH}	High Level Setup Time		90			ns
	t_{WH}	High Level Width		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low Level Width		150			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval Between Active Pulses	$t_{REP} = 40 + 2\ t_{CK} + t_{WL(CK)} + t_{R(CK)}$	see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe		0			ns
	t_{HH}	High Level Hold Time from Active Read Strobe		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns
$\overline{RD}$	t_{WL}	Low Level Width		180			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval Between Active Pulses	$t_{REP} = 40 + 2\ t_{CK} + t_{WL(CK)} + t_{R(CK)}$	see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe		0			ns
	t_{HH}	High Level Hold Time from Active Read Strobe		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	

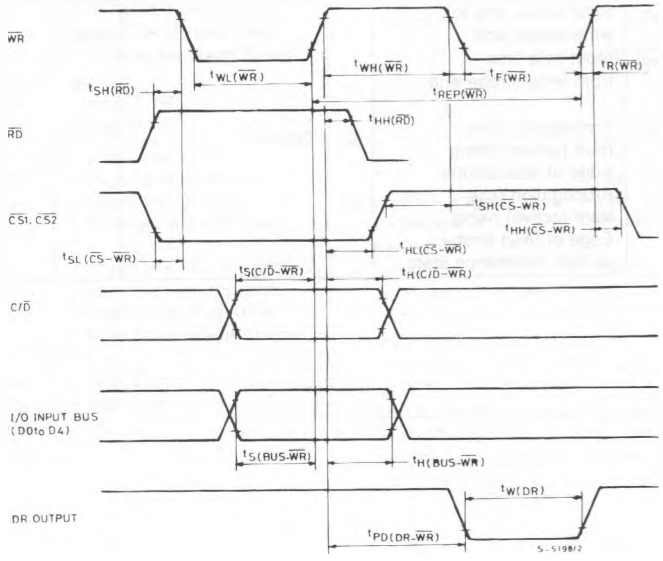
AC ELECTRICAL CHARACTERISTICS (continued)

Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{CS1}$, CS2	$t_{SL(\overline{CS}\text{-}\overline{WR})}$	Low level setup time to $\overline{WR}$ falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{WR})}$	Low level hold time from $\overline{WR}$ rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{WR})}$	High level setup time to $\overline{WR}$ falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{WR})}$	High level hold time from $\overline{WR}$ rising edge	Inactive Case	0			ns
	$t_{SL(\overline{CS}\text{-}\overline{RD})}$	Low level setup time to $\overline{RD}$ falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{RD})}$	Low level hold time from $\overline{RD}$ rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}\overline{RD})}$	High level setup time $\overline{RD}$ falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}\overline{RD})}$	High level hold time from $\overline{RD}$ rising edge	Inactive Case	0			ns
$\overline{C/D}$	$t_{S(\overline{C/D}\text{-}\overline{WR})}$	Setup time to write strobe end		180			ns
	$t_{H(\overline{C/D}\text{-}\overline{WR})}$	Hold time from write strobe end		25			ns
	$t_{S(\overline{C/D}\text{-}\overline{RD})}$	Setup time to read strobe start		20			ns
	$t_{H(\overline{C/D}\text{-}\overline{RD})}$	Hold time from read strobe end		25			ns
DR (data ready)	t_W	Low state width	Instructions 5 and 6			$2\text{-}t_{CK}$	ns
	t_{PD}	DP output delay from write strobe end (active command)	Instruction 5, C_L = 50 pf	$5\text{-}t_{CK}$		$14\text{-}t_{CK}$	ns
D0 to D7 (interface bus)	$t_{S(BUS\text{-}\overline{WR})}$	Input setup time to write strobe end		130			ns
	$t_{H(BUS\ \overline{WR})}$	Input hold time from write strobe end		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling Edge of read strobe	C_L = 200 pF			130	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising Edge of read strobe to high impedance state				80	ns

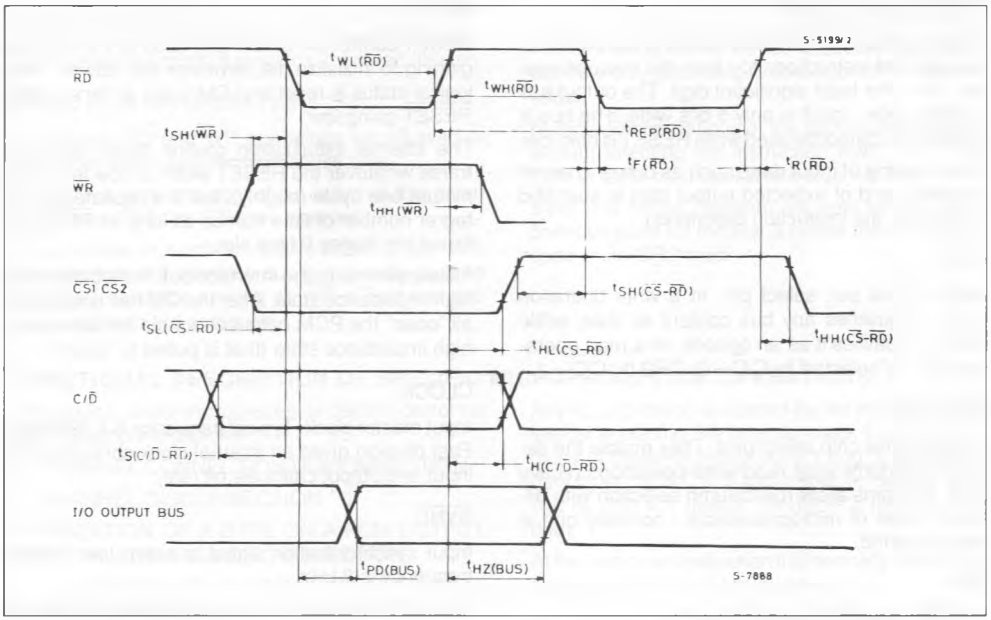
PCM TIMING, $\overline{RESET}$



WRITE OPERATION TIMING



READ OPERATION TIMING



GENERAL DESCRIPTION

The M044 is intended for PABX Systems and digital like concentrators where a micromputer control approach is extensively used. It consists of a speech memory (SM), a control memory (CM), a serial/parallel and a parallel/serial converter, an internal parallel bus, and interface (8 data lines, 11 control signals) and dedicated control logic. By means of repeated clock division two timebases are generated. These are preset from an external synchronisation signal to two specific count numbers so that sequential scanning of the bases give synchronous addresses to the memories and I/O channel controls. The timebase for the input channels is delayed and the timbase for output channels is advanced with respect to the actual time. Each serial PCM input channel is converted to parallel data and stored in the speech memory at the beginning of any new time slot (according to first timebase) in the location determined by input pin number and time slot number. The control memory CM maintains the correspondences between input and output channels. More exactly for any output pin/output channel combination the control memory gives either the full address of the speech memory location involved in the PCM transfer or an 8-bit word to be supplied to the parallel/serial output converter, A 9th bit at each CM location defines the data source for output links, low for SM, high for CM.

The late timebase is used to scan the output channels and to determine the pins to be serviced within each channel : enough idle cycles are left to the microprocessor for asynchronous instruction processing.

Two 8-bit registers OR1 and OR2 supply feedback data for control or diagnostic purposes ; OR1 comes from internal bus i.e. from memories, OR2 gives an opcode copy and additional data to the microcomputer. A four byte-five bit stack register and an instruction register, under microcomputer control store input data available at the interface.

PIN DESCRIPTION

D7 to D0 (pins 17 to 24)

Data bus pins. The bidirectional bus is used to transfer data and instructions to / from the microprocessor. D0 is the least significant digit. The output bus is 8 bits wide ; input is only 5 bits wide. The bus is tristate and cannot be used while $\overline{RESET}$ is held low.

The meaning of input data, such as bus or channel numbers, and of expected output data is specified in detail by the instruction description.

C/$\overline{D}$

Input control pin, select pin. In a write operation C/D = 0 qualifies any bus content as data, while C/D = 1 qualifies it as an opcode. In a read operation OR1 is selected by C/D = 0, OR2 by C/D = 1.

$\overline{CS1}$, $\overline{CS2}$

Commutative chip select pins. They enable the device to perform valid read/write operations (active low). Two pins allow row/column selection with different types of microprocessors ; normally one is tied to ground.

$\overline{WR}$

Pin $\overline{WR}$, when $\overline{CS1}$ and $\overline{CS2}$ are low, enables data transfer from microprocessor to the device. Data or opcode and controls are latched on $\overline{WR}$ rising edge. Because of internal clock resynchronization one single additional requirement is recommended in order to procedure a simultaneous instruction execution in a multichip configuration : $\overline{WR}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsed late relative to clock falling edge.

$\overline{RD}$

When $\overline{CS1}$ and $\overline{CS2}$ are low and a low level on $\overline{RD}$ enables a register OR1 or OR2 read operation, through the bidirectional bus.

In addition, the rising edge of $\overline{RD}$ latches C/$\overline{D}$ and the match condition pins in order to direct the internal flow of operations. Because of internal clock resynchronization, one single additional requirement is recommended in order to produce a simultaneous instruction flow in a multichip configuration : the $\overline{RD}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

DR

This is the data ready signal, it informs the microprocessor that data is available for reading (through OR1/OR2 registers)

$\overline{RESET}$

$\overline{RESET}$ control pin is normally used at the very beginning to inizialize the device or the network. Any logical status is reset and CM is set all "ones" after $\overline{RESET}$ going low.

The internal initialization routine takes one time frame whatever the $\overline{RESET}$ width on low level (minimum one cycle roughly), but it is repeated an integrer number of time frames as long as $\overline{RESET}$ is found low during 0 time slot.

Initialization pulls the interface bus immediately to a high impedance state. After the CM has been set to all "ones" the PCM output channels are also set to high impedance state (that is pulled to "ones").

CLOCK

Input master clock. Typical frequency is 4.096 MHz. First division gives an internal clock controlling the input and output channels bit rate.

$\overline{SYNC}$

Input synchronization signal is active low. Typical frequency is 8 kHz.

Internal time bases are forced by synchronism to an assigned count number in order to restore channels and bit sequential addressing to a known state. Count difference between the bases is 32, corresponding to two time slots, that is the minimum PCM propagation time, or latency time.

PCM IN 3 TO PCM IN 0

PCM input busses or pins ; they accept a standard 2 Mbit/s rate. Bit 1 (sign bit) is the first of the serial sequence ; in a parallel conversion it is left adjusted as the most significant digit.

PCM OUT3 TO PCM OUT0

PCM output busses or pins ; bit rate and organization are the same as input pins.

Output buffers are open drain type in order to simplify wired-or connections and minimize current spike problems in multichip configuration systems. The device drives the output channels theoretically one bit time before input channels are needed by specifications : this feature allows inputs and outputs to be tied together cancelling any analog delay of digital outputs up to :

$$t_{DEL\ max} = t_{bit} - t_{PD(PCM)max} + t_{PD(PCM)min}$$

BIAS

Internally generated bias voltage (– 2.5 to – 3.0 V for V_{CC} in the operating range). A max 220 pf capacitor connected to pin 5 provides improved filtering.

MIXED $\overline{RD}$ & $\overline{WR}$ OPERATIONS

In principle $\overline{RD}$ and $\overline{WR}$ operations are allowed in any order within specification constraints.

In practive, only one control pin is low at any given time when CS1 and $\overline{CS2}$ are enabled.

If by mistake or hardware failure both $\overline{RD}$ and $\overline{WR}$ pins are low, the interface bus is internally pushed to tristate condition as long as $\overline{WR}$ is held low and input registers are protected.

Registers OR1 and OR2 can be read in any order with a single $\overline{RD}$ strobe using C/$\overline{D}$ as multiplexing control ; never the less this procedure is not recommended because the device is directed for instruction flow only according to data latched by $\overline{RD}$ rising edge.

Multiple $\overline{RD}$ operations of the same kind ar allowed without affecting the instruction flow : only "new" OR1 or OR2 read operations step the flow.

Input and output registers are held for sure in the previous state for the first 3 cycles following an opcode or an OR2 read.

FUNCTIONAL DESCRIPTION OF SPECIFIC MICROPROCESSOR OPERATIONS

The device, under microprocessor control, performs the following instructions :

1. CHANNEL CONNECTION/DISCONNECTION
2. CHANNEL DISCONNECTION
3. INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL/CHANNEL DISCONNECTION
4. TRANSFER OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
5. TRANSFER OF A SINGLE OUTPUT CHANNEL CONTROL WORD

Any input protocol is started by the microprocessor interface loading the internal stack register with 2 bytes (4 bytes for instructions 1 and 3) qualified as data bytes by C/$\overline{D}$ = 0 and a specific opcode qualified by C/$\overline{D}$ = 1 (match condition is normally needed).

At the end of an instruction it is normally recommended to read one or both registers.

INSTRUCTION TABLES

The most significant digits of OR2 are a copy of the PCM selected output bus ; the least significant digits of OR2 are the opcode. C8 is the control bit. In any case parentheses () define actual register content.

INSTRUCTION 1 : CHANNEL CONNECTION/DISCONNECTION

Control Signals				Data Bus								Notes
C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bi2	Bi1	Bi0	1 st Data Byte : selected input bus
0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2 nd Data Byte : selected input channel
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3 rd Data Byte : selected input bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4 th Data Byte : selected output channel
1	0	0	1	X	X	X	X	0	0	0	1	Instruction Opcode
0	0	1	0	C7 (Bi2	C6 Bi1	C5 Bi0	C4 Ci4	C3 Ci3	C2 Ci2	C1 Ci1	C0 Ci0)	OR1 : CM Content Copy
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 0	0 0	0 0	0 0	1 1)	OR2

INSTRUCTION 2 : OUTPUT CHANNEL DISCONNECTION

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected output bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected output channel
1	0	0	1	X	X	X	X	0	0	1	0	Instruction Opcode
0	0	1	0	1	1	1	1	1	1	1	1	OR1 : CM Content Copy (output channel is inactive)
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	0 0	1 1	0 0)	OR2

INSTRUCTION 3 : LOADING A MICROPROCESSOR BYTE

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Ci7	Ci6	Ci5	1 st Data Byte : Most significant digits to be inserted
0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2 nd Data Byte : Least significant digits to be inserted
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3 rd Data Byte : selected output bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4 th Data Byte : selected output channel
1	0	0	1	X	X	X	X	0	1	0	0	Instruction Opcode
0	0	1	0	C7 (Ci7	C6 Ci6	C5 Ci5	C4 Ci4	C3 Ci3	C2 Ci2	C1 Ci1	C0 Ci0	OR1 : CM content copy, that is for match condition
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	0 0	0 0)	OR2 : that is

INSTRUCTION 4 : TRANSFER OF A SINGLE PCM SAMPLE

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected output bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected output channel
1	0	0	1	X	X	X	X	1	0	1	1	Instruction Opcode
0	0	1	0	C7 S7	C6 S6	C5 S5	C4 S4	C3 S3	C2 S2	C1 S1	C0 S0	OR1 : CM Content Copy if C8 = 1 ; or SM Content Sample if C8 = 0
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 C8	1 1	0 0	1 1	1 1)	OR2 : that is

Note : S7...S0 is a parallel copy of a PCM data. S7 is the most significant digit and the first of the sequence.

INSTRUCTION 5 : TRANSFER OF AN OUTPUT CHANNEL CONTROL WORD

Control Signals				Data Bus								Notes
C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1 st Data Byte : selected input bus
0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2 nd Data Byte : selected input channel
1	0	0	1	X	X	X	X	1	0	0	0	Instruction Opcode
0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1 : CM selected CM word copy
1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 0	1 0	0 0	0 0	0 1)	OR2 : that is

CONFERENCE CALL

A kit which includes Z80 µP and the M116 allows a flexible conference call system to be built up in which the participants can enter on any channel of the M044 (refer to M116 data sheet for detailed information).

TYPICAL APPLICATION