SGS-THOMSON
MICROELECTRONICS

25-30 WATT DC-DC CONVERTERS

- MTBF IN EXCESS OF 1M HOURS AT + 45°C AMBIENT TEMPERATURE
- PCB OR CHASSIS MOUNTABLE
- NO EXTERNAL COMPONENT REQUIRED
- SIX SIDED CASE
- HIGH EFFICIENCY (see data)
- 500 V_{DC} MINIMUM ISOLATION
- WIDE INPUT VOLTAGE RANGE (36 to 72V)
- REVERSE INPUT POLARITY PROTECTION
- PEAK INPUT OVERVOLTAGE WITHSTAND (90V/1 sec.)
- MINIMIZED INPUT REFLECTED CURRENT
- SOFT START
- REMOTE INHIBIT/ENABLE WITH LOW STAND BY CURRENT
- REMOTE OUTPUT VOLTAGE SENSE
- NON LATCHING PERMANENT SHORT CIR-CUIT PROTECTION
- LATCHING OUTPUT OVERVOLTAGE PRO-TECTION
- PARALLEL OPERATION
- NO DERATING OVER THE TEMPERATURE RANGE

12V and 15V. (OTHER OUTPUT VOLTAGES available on request).

The output power is in the range of 25W to 30W.

To ensure very long life, these converters don't use any electrolytic capacitor or optoelectronic feedback system.

The converters permit paralleling of outputs.

DESCRIPTION

The GS-T25/30 series is a family of isolated DC-DC converters specially designed for Telecom application, available in different output voltages : 5V ; 6V ;
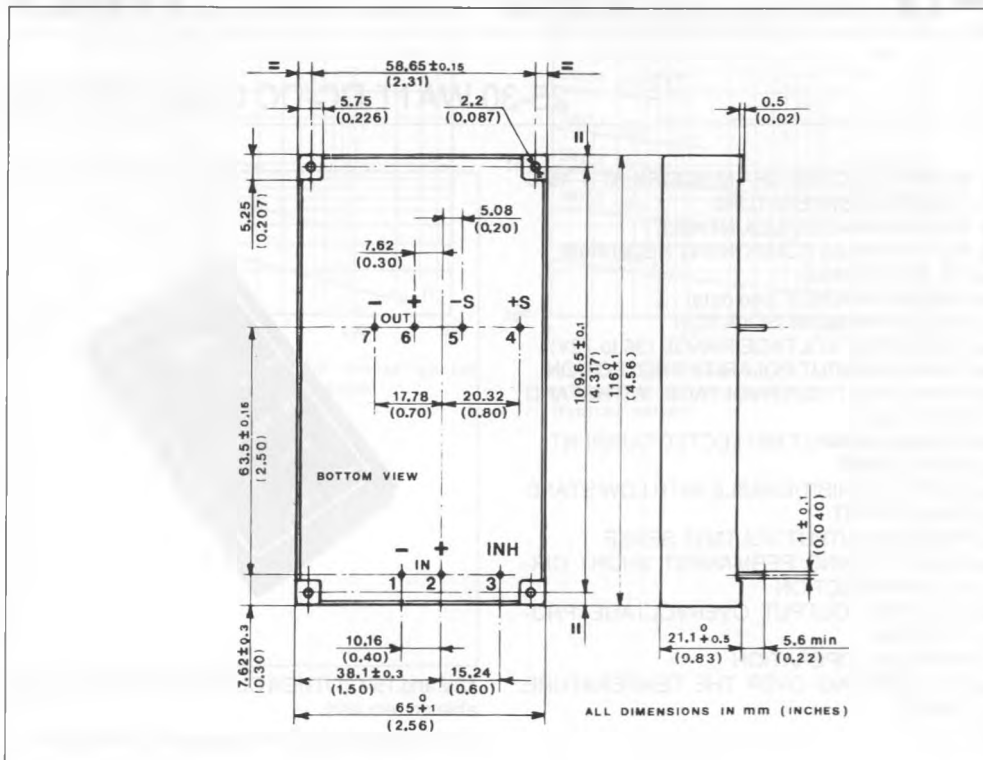
PRODUCTS FAMILY

Order Number	Output Voltage	Output Current	Output Power
GS-T25-0500	5V	5A	25W
GS-T27-0600	6V	4.5A	27W
GS-T30-1200	12V	2.5A	30W
GS-T30-1500	15V	2A	30W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	34 to 72	V
V_{ipk}	Input Transient Overvoltage (T ≤ 1sec.)	90	V
V_{ir}	Input Reverse Voltage	100	V
T_{stg}	Storage Temperature Range	– 55 to 105	°C
T_{op}	Operating Temperature Range	– 25 to 71	°C

CONNECTION DIAGRAM AND MECHANICAL DATA (bottom view)

PIN FUNCTIONS

Pin	Function
1	– Input.
2	+ Input. Unregulated input voltage (typically 48V) must be applied between pin 1-2. The input section of the DC-DC converter is protected against reverse polarity by a series diode. No external fuse is required. Input is filtered by a Pi network.
3	Remote inhibit/enable logically compatible with CMOS or open collector TTL. The converter is ON when the voltage applied to pin 3 is $1.8V_{DC}$ min or left open referenced to the pin 1. The converter is OFF for a control voltage lower than $1.2V_{DC}$.
4	Sensing Positive. For connection to remote loads this pin allows voltage sensing to the load itself. TO BE CONNECTED TO PIN 6 WHEN REMOTE SENSING IS NOT USED.
5	Sensing Negative. See pin 4. TO BE CONNECTED TO PIN 7 WHEN REMOTE SENSING IS NOT USED.
6	+ Output.
7	– Output.

ELECTRICAL CHARACTERISTICS (Tamb = 25°C unless otherwise specified)

INPUT

	Type		GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_i	Input Voltage	Full Load	36	48	72	36	48	72	36	48	72	36	48	72	V
I_i	No Load Input Current	V_{IN} = 48V		15			15			15			20		mA
I_i	Full Load Input Current	V_{IN} = 48V		640			680			730			730		mA
I_{ir}	Input Reflected Current (sinusoidal)	V_{IN} = 48V/full Load		200			200			200			200		mApp
I_i	Input Short Circuit Current	V_{IN} = 48V		22			24			43			55		mA
I_{isb}	Input Stand by Current	V_{IN} = 48V V_3 = 0V		5			5			5			5		mA
V_{INHL}	Low Inhibit Voltage	V_{IN} = 48V, Full Load			1.2			1.2			1.2			1.2	V
V_{INHH}	High Enable Voltage	V_{IN} = 48V, Full Load	1.8 or open			1.8 or open			1.8 or open			1.8 or open			V
I_{INH}	Input Inhibit Current	V_{IN} = 48V, Full Load		1.8			1.8			1.8			1.8		mA

OUTPUT

	Type		GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage	V_{IN} = 48V Full Load	4.95	5.00	5.05	5.94	6.00	6.06	11.88	12.00	12.12	14.85	15.00	15.15	V
ΔV_O	Line Regulation	V_{IN} = 36V to 72V Full Load		± 0.001			± 0.001			± 0.001			± 0.001		%
ΔV_O	Load Regulation	V_{IN} = 48V Full Load to no Load		± 0.05			± 0.05			± 0.05			± 0.05		%
V_r	Ripple and Noise Voltage	V_{IN} = 48V Full Load		5			5			5			5		mVRMS
$V_{O\ OV}$	Output Overvoltage Protection	V_{IN} = 48V Full Load			6.8			8.2			15			18	V
ΔV_O	Remote Sense per Leg	V_{IN} = 36V			0.6			0.6			0.6			0.6	V
t_{ss}	Soft Start Time	V_{IN} = 48V Full Load		30			30			30			30		ms
I_o	Max Output Current	V_{IN} = 48V			5			4.5			2.5			2	A
I_{sck}	Output Current Limit	V_{IN} = 48V Overload		5.5			4.95			2.75			2.2		A
I_{osc}	Output Average Short Circuit Current	V_{IN} = 48V,		0.7			0.8			1.1			1.2		A

ELECTRICAL CHARACTERISTICS (continued)

OUTPUT (continued)

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
T_{rt}	Transient Recovery Time	V_{IN} = 48V ΔI_o = 25% Step Load Change		75			75			75			75		μs
T_c	Temperature Coefficient	V_{IN} = 48V, Full Load ; Operating Temperature Range		+ 0.02			+ 0.02			+ 0.02			+ 0.02		%/°C

GENERAL

Type			GS-T25-0500			GS-T27-0600			GS-T30-1200			GS-T30-1500			Unit
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
η	Efficiency	V_{IN} = 36 to 72V Full Load		81			82			86			86		%
P_d	Power Dissipation in Short Circuit Condition	V_{IN} = 48V		1.06			1.15			2.06			2.6		W
V_{IS}	Isolation Voltage		500			500			500			500			V_{DC}
R_{IS}	Isolation Resistance		10^9			10^9			10^9			10^9			Ω
f_s	Switching Frequency	V_{IN} = 48V Full Load		150			150			150			150		kHz

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The GS-T25/30 series of DC-DC converter has been designed to meet the demanding application of the Telecommunication industry.

Particular attention has been devoted to maximize the reliability of the converters as described in the following.

SYSTEM ARCHITECTURE

The switching push-pull current mode architecture has been adopted because :
- it allows large duty cycle (80%) so lowering the input peak current ;
- it minimizes the transformer flux imbalance (current mode cycle by cycle control) :
- it allows, because of its symmetry and together with a switching frequency of 150kHz, to minimize the inductance and capacitance values ;
- it offers exceptional performance in terms of line regulation because of the feedforward effect inherent to current mode control.

COMPONENT CHOICE

Because of the system architecture, ceramic or solid tantalum capacitors only are used.

In addition, the voltage regulation loop is closed by sensing directly the output voltage on the secondary side without any optocoupler feedback device.

Power MOS transistors with a current capability 30 times larger than maximum operating condition have been adopted as primary side switches ; voltage capability is 2.5 times higher than nominal condition.

Efficiency is maximized by lowering switching and conduction losses on the primary side and rectification losses on the secondary side by use of Schottky diodes on the GS-T25/27 models.

PACKAGE

The package is of die casted aluminum type that offers a typical thermal resistance case to ambient of 4°C/W.

This, together with the low power dissipation, allows to keep junction temperature of silicon devices at less than 100°C even for ambient temperature of 71°C with free air convection.
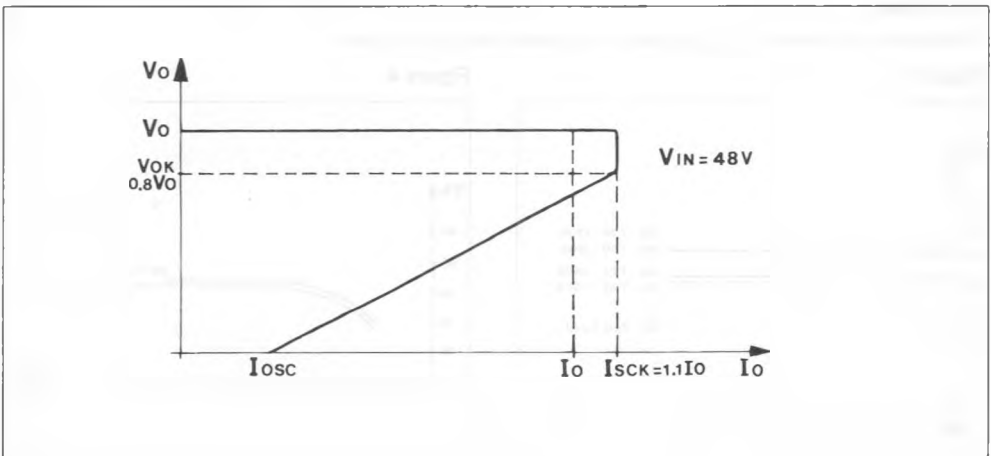
OVERLOAD PROTECTION

The overload protection has been designed so that two different objectives are met :
- parallel connection possibility, to increase available output regulated power ;
- reduction of available current during heavy overload and/or short circuit.

The typical diagram of this protection is shown in fig. 1.

Figure 1 : Typical Overload Protection.

During short circuit, current stresses on primary and secondary side are actually lower than in nominal condition.

Power dissipation inside the module is minimized.

OVERVOLTAGE PROTECTION

In case of output voltage higher than overvoltage limits, the DC-DC converter is shut down and it remains in a latching condition.

Current drain at the input is 20mA typically, so that this latching condition is not hazardous for the whole equipment where the DC-DC converter is used.

SOFT START

To avoid heavy inrush current the output voltage rise time is controlled as a function of the load condition : the larger the output current, the softer the output voltage rise. See fig. 2.

Figure 2 : Soft Start as a Function of the Output Current.
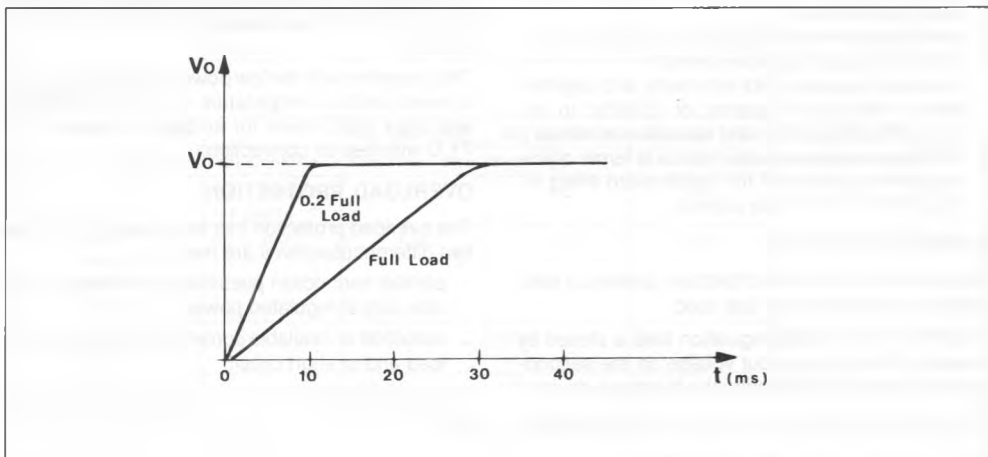
EFFICIENCY

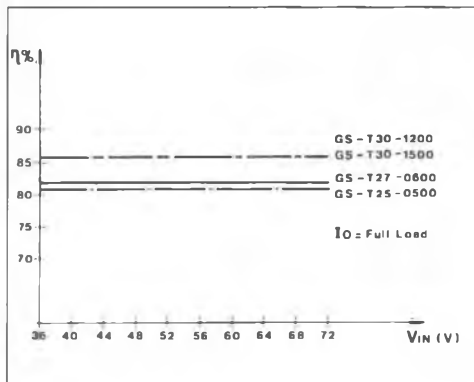The efficiency of these DC-DC converters is shown in fig. 3, 4, 5 and 6.

Figure 3.
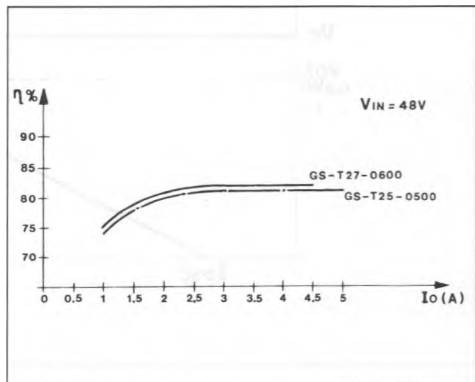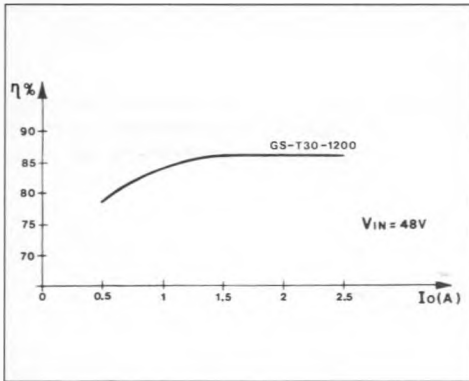

Figure 4.

Figure 5.

Figure 6.