The Development of a VLSI IC for TETRA

The FX980 Baseband Processor

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Introductions

- **Matthew Phillips** **B.Sc. (Hons)**

  Marketing Manager

  Consumer Microcircuits Ltd

- **Ken Wallace** **M.Sc. (V.L.S.I. Design)**

  Senior Project Engineer

  Integrated Microsystems Ltd

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CML Microsystems Plc.

Semiconductor Division

CML UK and division HQ

IMS Ltd

MX-COM Inc.

CML Singapore Pte

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CML History in Land Mobile Radio

- *1980* First single IC 5-Tone Selcall encoder / decoder
- *1981* First single IC CTCSS encoder / decoder
- *1984* FX409 FFSK modem used in first UK trials of MPT1317 / 1327
- *1989* Launch of single IC FFSK modem including MPT1317 data formatting
- *1995* Launch single IC modems for Mobitex/RD-LAP/ CDPD
- *1997* Sample FX980 TETRA Baseband Processor

TETRA IC design objectives

- To be attractive to users terminals need to be
  - ➔Small size
  - ➔Lightweight
  - ➔Long battery life
  - ➔Highly featured
- An IC for TETRA needs to help OEM design teams achieve these goals
- CML focussed on baseband as area of expertise

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TETRA Baseband Processor design objectives

- Integrate baseband ADC and DAC functions
- Reduce processing load on host Digital Signal Processor
- Lower effective power budget for baseband functions
- Optimize solution for operation with 3.0 volt supplies
- Reduce size and ‘glue’ with high integration

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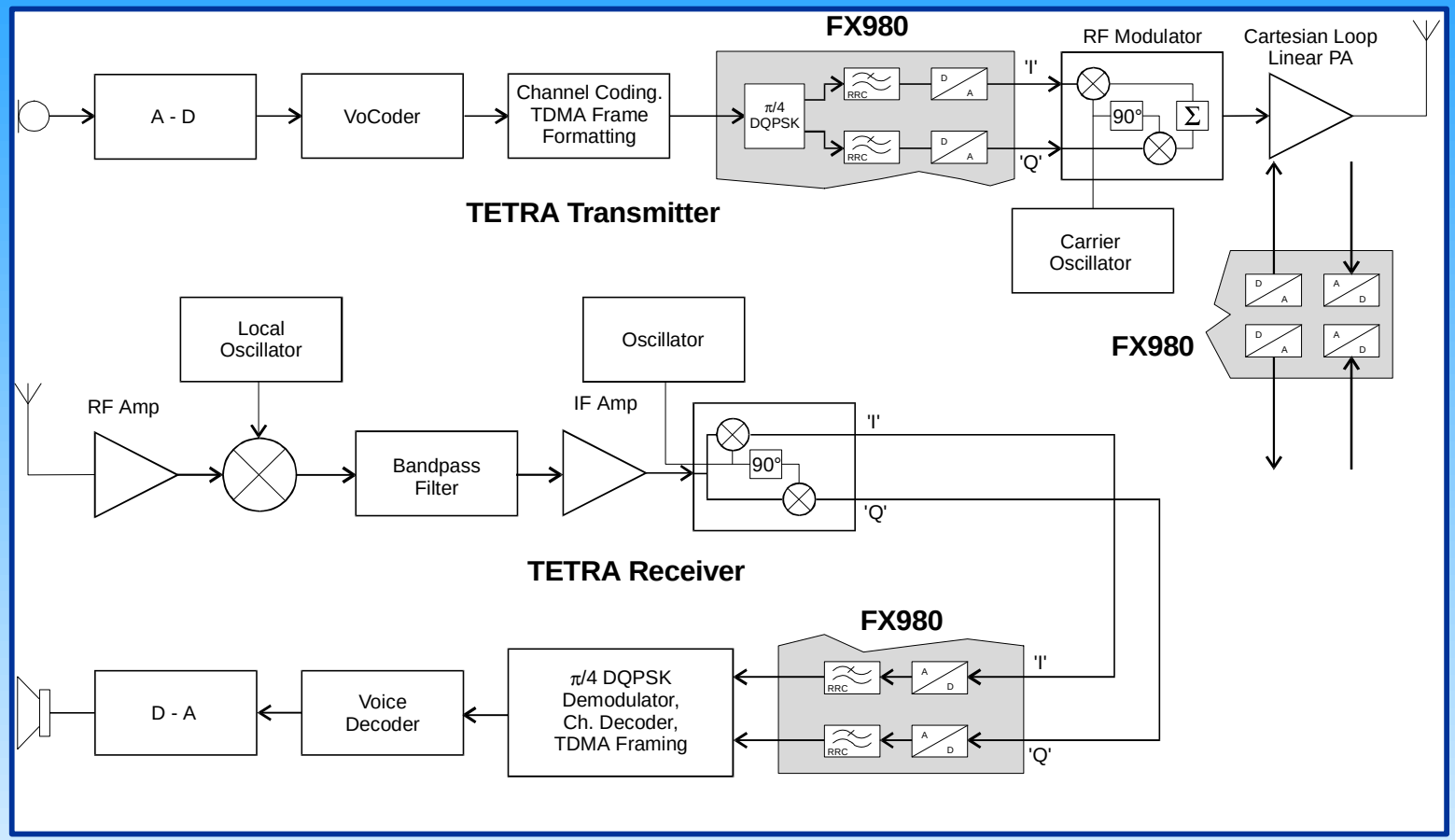
Outline TETRA terminal architecture



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TETRA Tx Specifications

- TETRA specification allows for co-channel analogue and digital systems
- Places large demands on Tx symbol filters and Tx Path DAC converters
- Requires use of Linear Tx Power Amplifier
  - ➔Non constant envelope modulation
  - ➔Spurious emissions specifications

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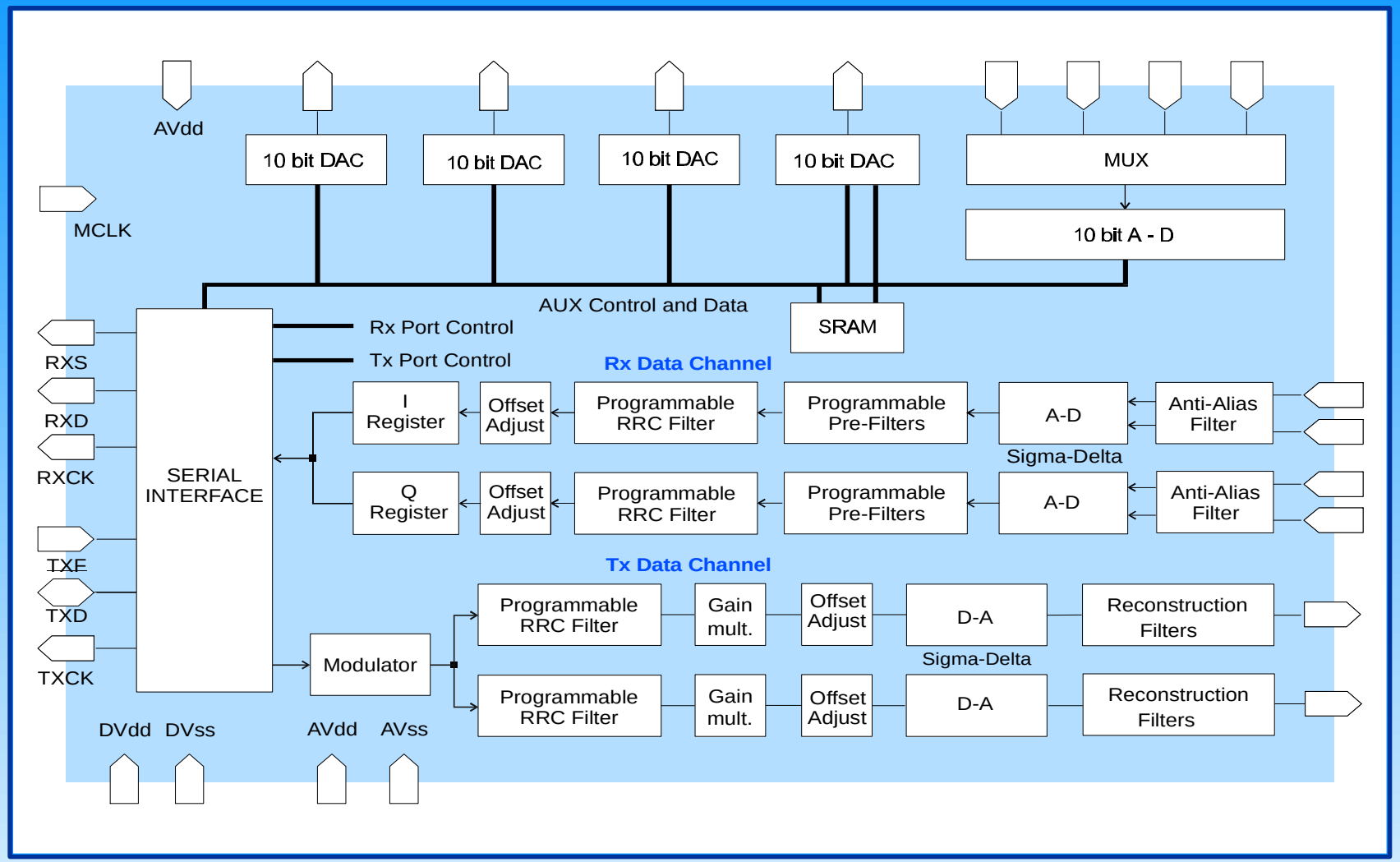
TETRA Rx Specifications

- Rx channel filters must not distort received $\pi/4$ DQPSK symbols and degrade BER
- Most of adjacent channel filtering is done at baseband
- Received signals will have very wide dynamic range
- ADC's must correctly digitize wanted channel and adjacent channels to allow baseband filters to correctly reject adjacent channel signals

TETRA Terminal Control functions

- Control and Monitoring is required
  - Tx power ramping and adaptive power control
  - PA linearising circuit adjustment
  - Battery level
  - RSSI monitoring for AGC adjustment
  - VSWR monitoring
  - According to the designers inspiration !

FX980 TETRA Baseband Processor



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System Partitioning Considerations

- Die size vs. yield vs. unit cost
- Trade off between application specific or broader use
- Noise and cross-talk limitations on common substrate
- Simulation and design validation limitations

On chip system components

- Serial Interface and control logic
- π/4 DQPSK modulator
- Digital FIR filters
- ADC's DAC's
- Auxiliary components for system level use
- Compensation facilities for off-chip deficiencies
- Test and user development features

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Off chip system components

- **Voice audio ADC and DAC**
  - ➔ **High silicon area on chip wide variety of low cost devices available**
- **Vocoder/Decoder**
  - ➔ **Requirement for asynchronous clock generation possibility of substrate cross-talk**
- **Radio Intermediate Frequency sections**
  - ➔ **Wide variety of user preferred methodologies. Increase in pin count**

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Design Implementation
Serial Interface 1

- **Serial Interface with 3 ports:**
- **Command Port - *Cmd***
  - ➔ **Input/bi-directional 16 bit data frame**
  - ➔ **For DSP/µController to FX980 commands and data read back (bi-directional mode)**
  - ➔ **Simple command/data structure compatible with most popular DSP and µController devices**

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Design Implementation
Serial Interface 2

- **Receive Data Port - *RxDat***
  - ➔ **Output with 16/32 bit data frames**
  - ➔ **For Rx data export or data read back**
  - ➔ **MSB/LSB bit order reversal**
  - ➔ **Auto clock stop**
  - ➔ **Sample phase selection**

Design Implementation
Serial Interface 3

- **Read Command Port - *RdCmd***
  - ➔Output with 16 bit data frame
  - ➔For command and data read back
- **Two data rates**
  - ➔¼ master clock (low data rate) 2.304 Mb/s
  - ➔Received data is supplied at reduced rate
  - ➔½ master clock (high data rate) 4.608 Mb/s
  - ➔Full received data available

Design Implementation
Tx Data Path 1

- **Symbol Data FIFO**
  - ➔Four deep FIFO with associated interrupt structure
  - ➔For a wide variety of data communications protocols
  - ➔FIFO free (not full)
  - ➔Trapped error conditions
    - FIFO overwrite
    - FIFO under-read
    - FIFO empty

Design Implementation
Tx Data Path 2

- Data Encoding
- $\pi/4$ DQPSK modulator with bypass
- Direct constellation point access

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Design Implementation
Tx Data Path - FIR Filters 1

- Adoption of RAMS instead of data latches for both Coefficient and Data storage gives low power consumption
- Algorithm developed for moving pointers to locations rather than data
- Single fast multiplier and accumulator per filter
- Read/Write on all Coefficients, with single bit reset to default coefficient values

Design Implementation
Tx Data Path - FIR Filters 2

- Three filters in the TX path
  - ➔79 tap zero padded filter for high stop band performance without sin(x)/x droop
  - ➔49 tap root raised cosine filter with =0.35
  - ➔15 tap DAC response correction
- Clock stop logic for low power consumption in power down modes

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Design Implementation
Tx Data Path - Arithmetic Operation

- µ-code engine to produce all arithmetic operations for both channels
- Gives independent adjustment for
  - ➔gain
  - ➔phase
  - ➔offset
- Automatic amplitude ramping up and down
- Automatic filter delay matching to ramp up signal

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Design Implementation
Tx Data Path - Sigma Delta DAC

- High performance 3rd order Sigma Delta digital to analogue converters
- Low pass band quantisation noise
- Linear - no missing codes
- 5th Order SC filters to suppress stop band noise
- Three pole RC filter to remove high frequency clock noise
  - ➔Two poles on-chip, one off-chip
- Differential outputs for high common mode rejection i.e. low noise systems

Design Implementation
Rx Data Path - Anti Alias Filter

- Three pole Chebyshev at 50 kHz, with 0.1dB ripple
  - ➔100dB attenuation at 2.304 MHz (with at least 30dBs attenuation off-chip)
  - ➔Flat response and linear phase in passband
- Only single pole off-chip RC required
- Performance maintained with on-chip component variations

Design Implementation
Rx Data Path - Sigma Delta ADC

- One bit at 2.304 MHz
- 4th Order fully differential switched capacitor feed-forward paths for stability leads to performance equivalent of theoretical 3rd order Sigma Delta
- Following digital filter can be close to signal band Sigma Delta modulator

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Design Implementation
Rx Data Path - FIR Filters 1

- **59 Tap Filter**
  - ➔ 1 bit input / 14 bit output
  - ➔ Removes high frequency contents of sigma delta converter.
- **Decimation Filter**
  - ➔ High rejection at 144 kHz and multiples
  - ➔ Averages 16 input samples at 2.3 MHz. Outputs one sample at 144 kHz. 14bit in / 16bit output
  - ➔ Sample phasing adjustable with digital vernier control.
  - ➔ Independent for I and Q

Design Implementation
Rx Data Path - FIR Filters 2

- **49 Tap RRC FIR Filter (16 bit)**
  - ➔ **49 Tap Root Raised Cosine filter with $\alpha = 0.35$**
- **63 Tap FIR Filter (16 bit)**
  - ➔ **Provides high stop band rejection required for adjacent channel suppression meeting TETRA specifications**

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Design Implementation
Rx Data Path - Rx Data Interface

- Parallel to serial data handling,
- Transfer in low data / high data rate modes
- 16 or 32 bit frames
- MSB or LSB first
- Clock Stop Logic
- Low power consumption in power down modes

Design Implementation
Auxiliary Section

- **Four Independent ADC Channels**
  - ➔ **SAR type conversion to 10 or 8 bits accuracy**
  - ➔ **Control logic for selecting channels to be converted.**
  - ➔ **Single cycle of all selected channels or continuous conversion modes .**
  - ➔ **Two conversion rates MCLK/80 or MCLK/160**

Design Implementation
Auxiliary Section

- Four Independent DAC Channels
- Ancillary user defined functions
- DAC1 input switchable to SRAM table
  - ➔64 x10 SRAM with controller for waveform or power ramp envelope generation.
  - ➔Single ramp mode
  - ➔Ramp direction control up/down
  - ➔Continuous AutoCycle mode (waveform generation)
- 8 Selectable conversion rates from 36 kHz to 4608 kHz

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Design Implementation
Interrupt Generation 1

- A comprehensive interrupt structure for detecting important events within the device during functional operations
- Allows wide range of interfacing modes for users through software routines
- All interrupts are maskable giving user complete control over events of interest

Design Implementation
Interrupt Generation 2

- Interrupts on
  - ➔FIFO events as previously outlined
  - ➔arithmetic overflows in FIR filters
  - ➔arithmetic overflows in DPO.
  - ➔EvenSample phasing for lost sync recovery

Design Implementation
Test Modes - Scan Path

- For production testing
  - ➔ Ensures high Quality levels to customers
- Gives maximum testability in shortest time for limited external pins count

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Design Implementation
Test Modes - Built in Self Test

- To provide a high level of autonomous self testing capabilities
- Pseudo Random Sequence Generator in conjunction with Cyclic Redundancy registers provide unique signatures for functional devices
- Single cycle (burst) or continuous mode available for internal or external BIST operations

Design Implementation
Test Modes - Built in Observation nodes

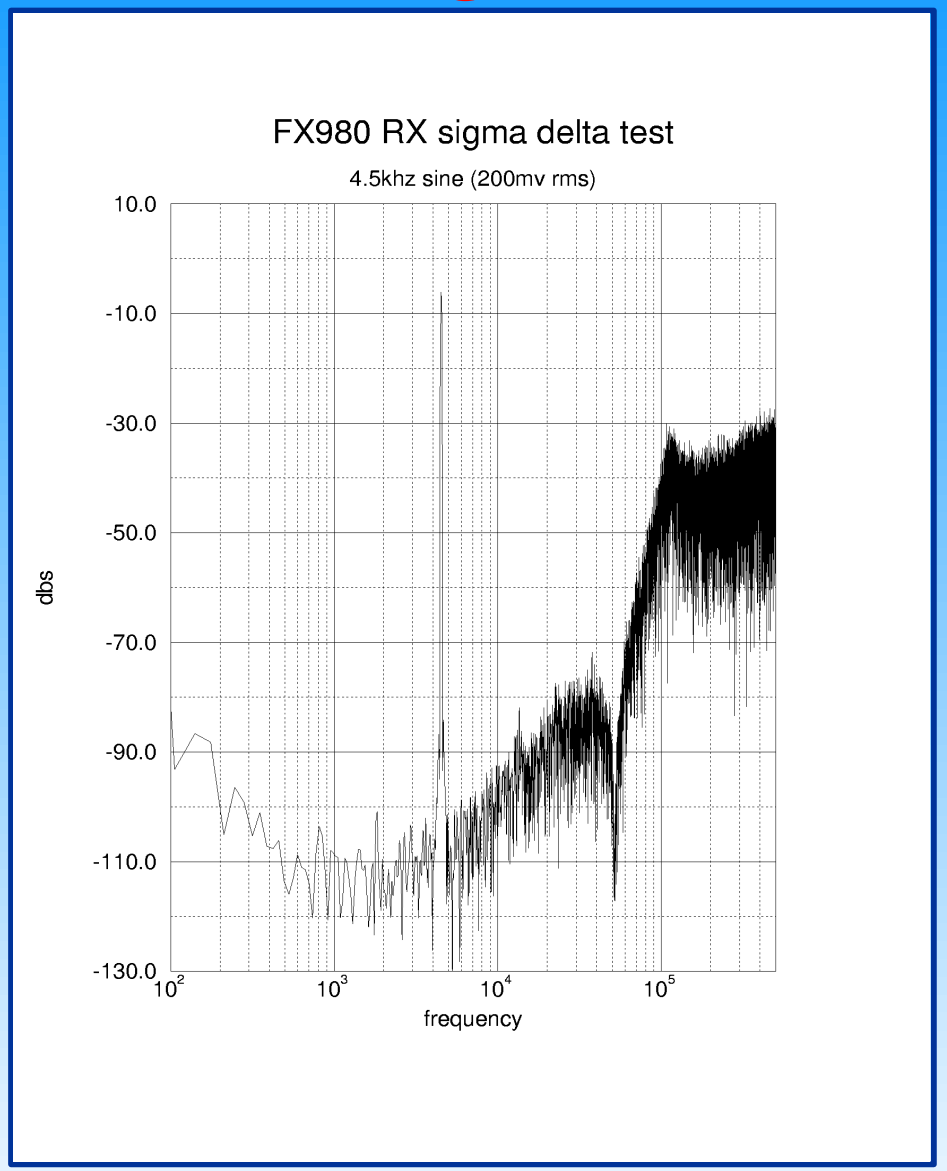
- Provides access to buried nodes within the device for testing and performance analysis of critical system components e.g. ADC's and integrator stages

Design Implementation
Test Modes - Test Path Routing

- Internal routing of data paths in the device maximizing use of on chip systems in assisting test and debug phases in the system design cycles
- Rx data path can be routed to TX 49 tap filter input. This allows users to see recovered received data on the TX DAC output pins

Results of device testing

- Rx sigma delta ADC converter tests 200 mV Sine Wave 4.5khz
- Shows pass band conformance to design spec



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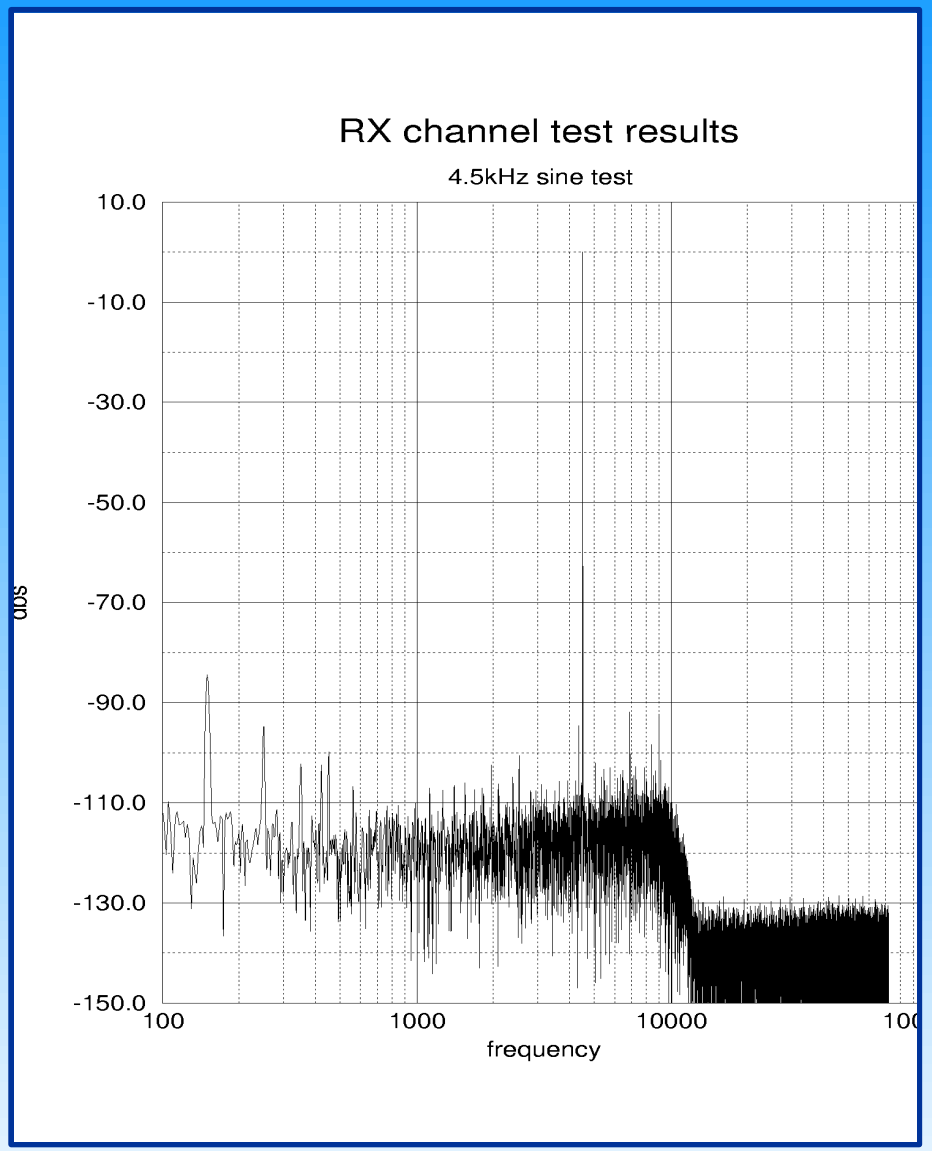
Results of device testing

- Test of Rx FIR Filter performance



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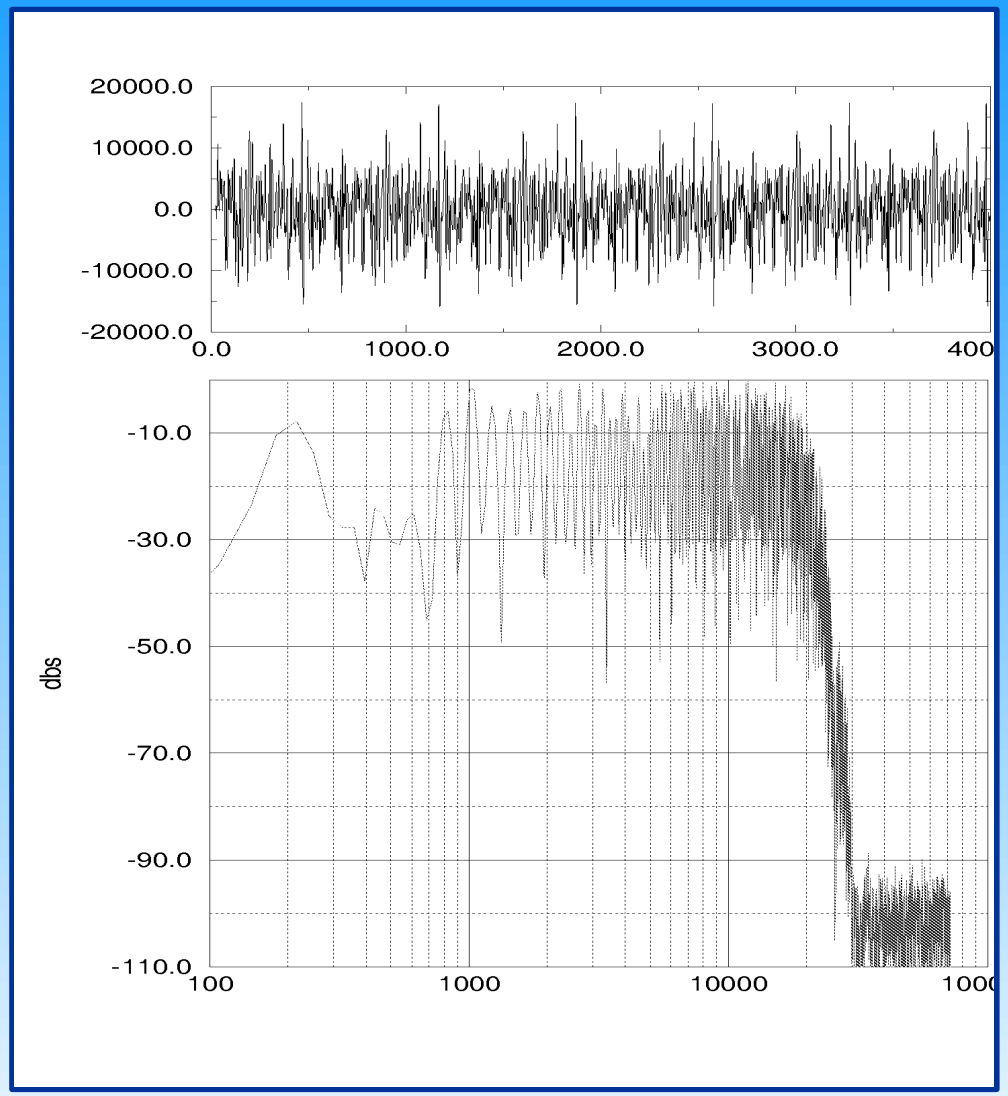
Results of device testing

- Test of Tx Path FIR Filter performance
- Using BIST for random symbol generation



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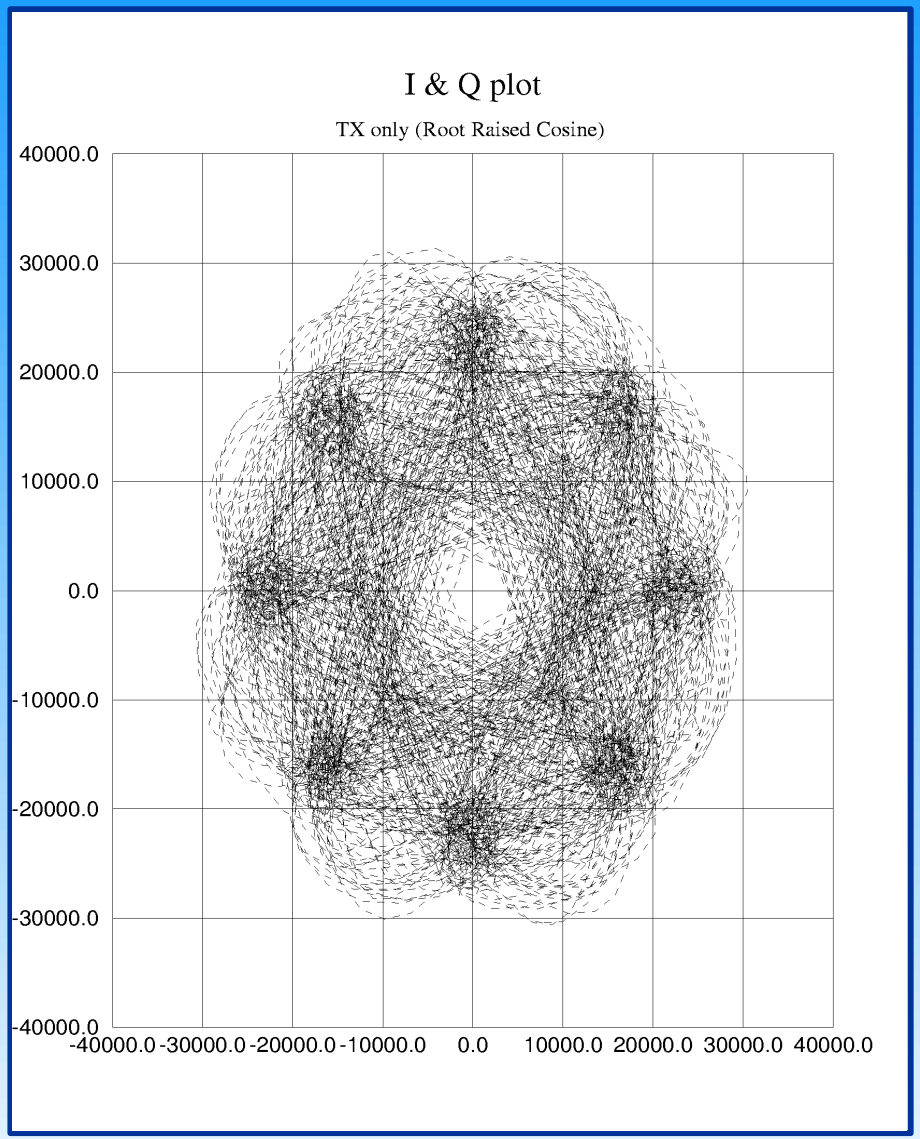
Results of device testing

- **Root Raised Cosine I and Q on vector plot shows loose constellation grouping**



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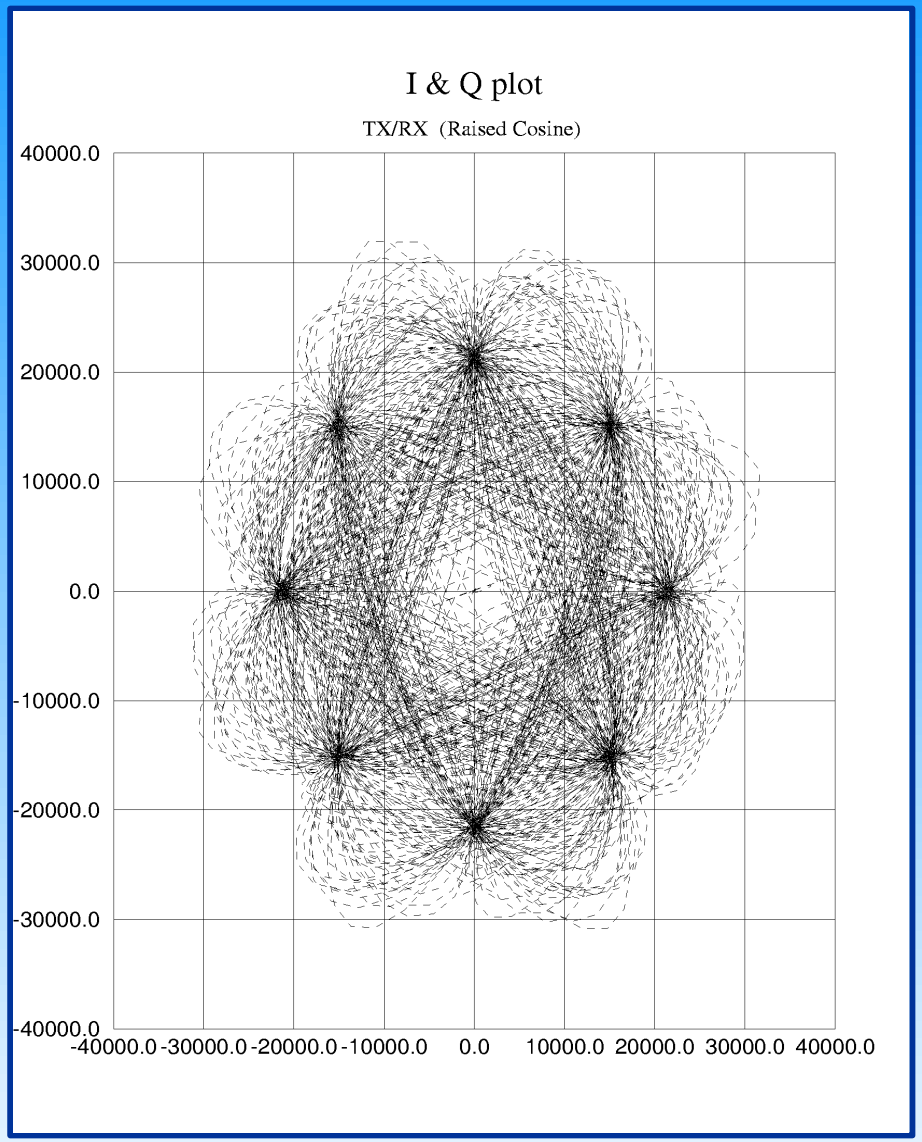
Results of device testing

- **Tx Path Data routed back through Rx. Constellation points grouped as per Raised Cosine filter**



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