

# FAN6204

## mWSaver™ Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

### Features

- mWSaver™ Technology:
  - Internal Green Mode to Stop SR Switching for Lower No-Load Power Consumption
  - 1.1mA Ultra-Low Green Mode Operating Current
- SR Controller
- Suited for Flyback Converter in QR, DCM, and CCM Operation
- Suited for Forward Freewheeling Rectification
- PWM Frequency Tracking with Secondary-Side Winding Voltage Detection
- Ultra-Low  $V_{DD}$  Operating Voltage for Various Output Voltage Applications (5V~24V)
- $V_{DD}$  Pin Over-Voltage Protection (OVP)
- 12V (Typical) Gate Driver Clamp
- 8-Pin SOP Package

### Applications

- AC/DC NB Adapters
- Open-Frame SMPS
- Battery Charger

### Description

FAN6204 is a secondary-side synchronous rectification (SR) controller to drive SR MOSFET for improving efficiency. The IC is suitable for flyback converters and forward free-wheeling rectification.

FAN6204 can be applied in continuous or discontinuous conduction mode (CCM and DCM) and quasi-resonant (QR) flyback converters based on the proprietary innovative linear-predict timing-control technique. The benefits of this technique include a simple control method without current-sense circuitry to accomplish noise immunity.

With PWM frequency tracking and secondary-side winding voltage detection, FAN6204 can operate in both fixed- and variable-frequency systems.

In Green Mode, the SR controller stops all SR switching operation to reduce the operating current. Power consumption is maintained at minimum level in light-load condition.

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6204MY	-40°C to +105°C	8-Pin, Small Outline Package (SOP)	Tape & Reel

## Application Diagrams

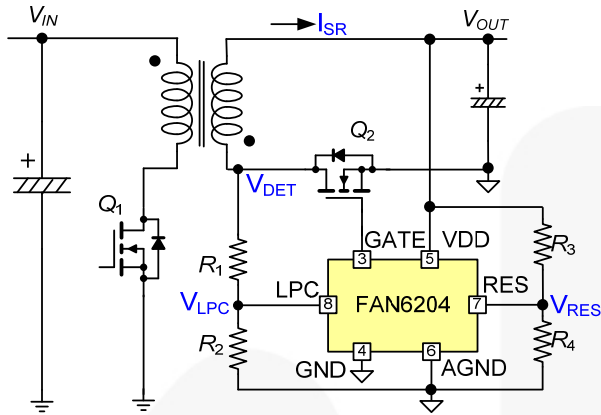


Figure 1. Typical Application Circuit for Flyback Converter

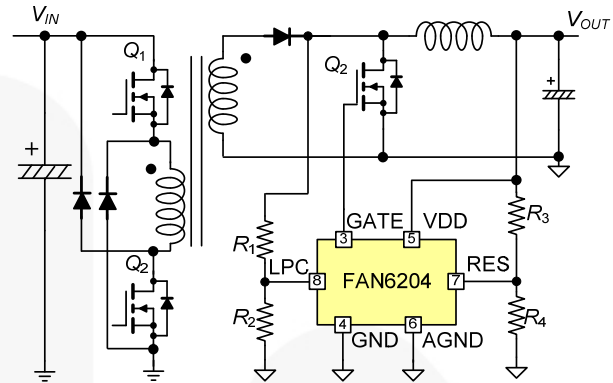


Figure 2. Typical Application Circuit for Forward Freewheeling Rectification

## Internal Block Diagram

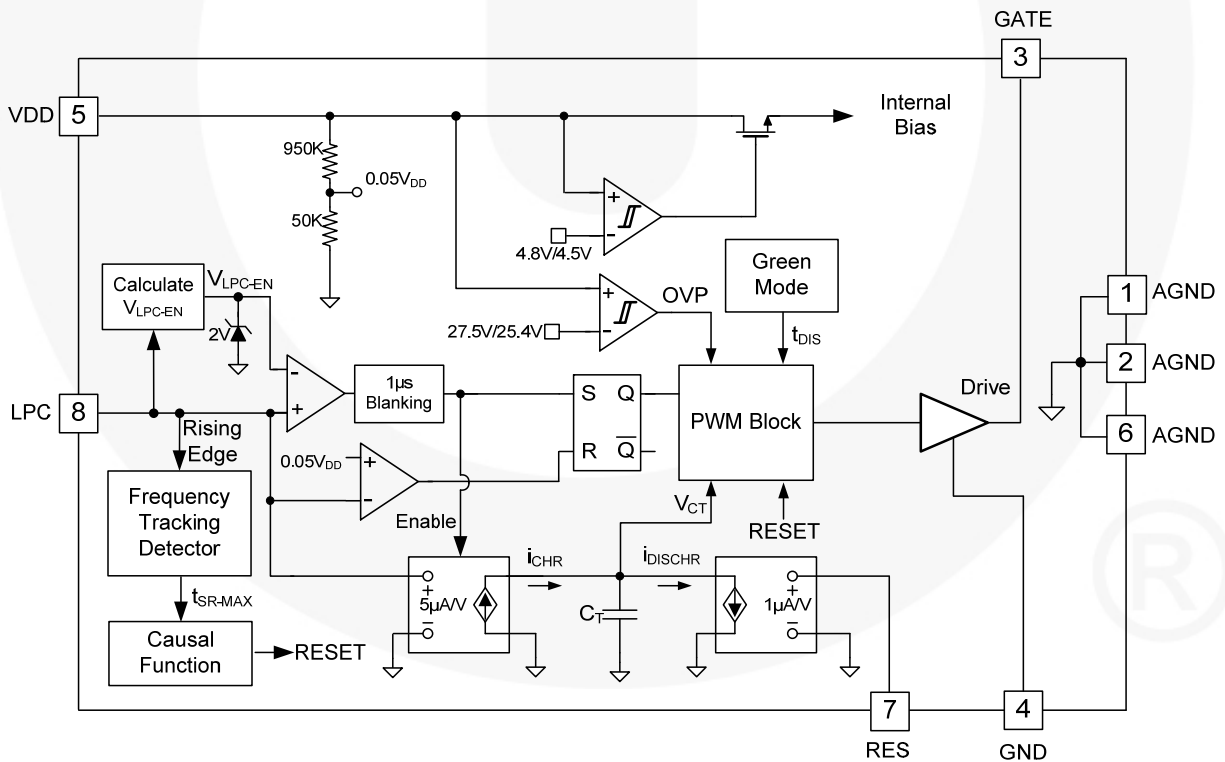
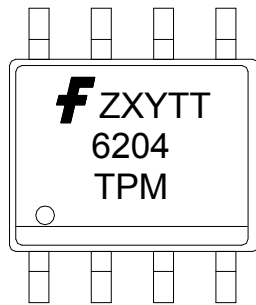


Figure 3. Functional Block Diagram

## Marking Information



**f**: Fairchild Logo  
**Z**: Plant Code  
**X**: Year Code  
**Y**: Week Code  
**TT**: Die Run Code  
**T**: Package Type (N = DIP, M = SOP)  
**P**: Y = Green Package  
**M**: Manufacturing Flow Code

Figure 4. Marking Diagram

## Pin Configuration

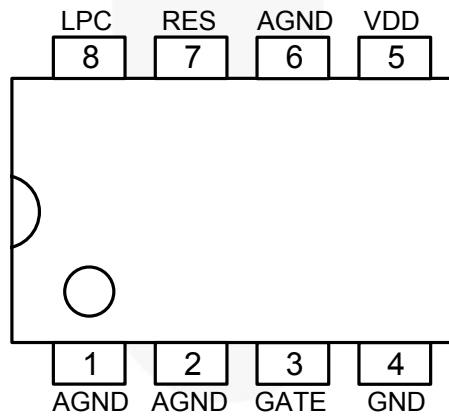


Figure 5. Pin Assignments

## Pin Definitions

Pin #	Name	Description
1	AGND	<b>Signal Ground</b>
2	AGND	<b>Signal Ground</b>
3	GATE	<b>Driver Output.</b> The totem-pole output driver for driving the power MOSFET.
4	GND	<b>Ground.</b> MOSFET source connection.
5	VDD	<b>Power Supply.</b> The threshold voltages for startup and turn-off are 4.8V and 4.5V, respectively.
6	AGND	<b>Signal Ground</b>
7	RES	<b>Reset Control</b> of linear predict. The RES pin is used to detect the output voltage level through a voltage divider. An internal current source, $I_{DISCHR}$ , is modulated by the voltage level on the RES pin.
8	LPC	<b>Winding Detection.</b> This pin is used to detect the voltage on the winding during the on-time period of the primary GATE.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage		30	V
V <sub>L</sub>	LPC, RES	-0.3	7	V
P <sub>D</sub>	Power Dissipation(T <sub>A</sub> =25°C)		45	W
Θ <sub>JA</sub>	Thermal Resistance (Junction-to-Air)		151	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)		58	°C/W
T <sub>STG</sub>	Storage Temperature Range	-55	+150	°C
T <sub>L</sub>	Lead Temperature (Soldering 10 Seconds)		+260	°C
ESD	Human Body Model		5	KV
	Charged Device Model		2	

### Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

## Electrical Characteristics

$V_{DD}=15V$  and  $T_A=25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{OP}$	Continuously Operating Voltage		$V_{DD-OFF}$		28.5	V
$V_{DD-ON}$	Turn-On Threshold Voltage		4.3	4.8	5.3	V
$V_{DD-OFF}$	Turn-Off Threshold Voltage		4.0	4.5	5.0	V
$V_{DD-HYST}$	$V_{DD-ON} - V_{DD-OFF}$		0.1	0.3	0.5	V
$I_{DD-OP}$	Operating Current	$V_{DD}=15V, L_{PC}=50KHZ, MOSFET$ $C_{ISS}=6000pF$		7	8	mA
$I_{DD-GREEN}$	Operating Current in Green Mode	$V_{DD}=15V$		1.1	1.3	mA
$I_{DD-ST}$	Startup Current	$V_{DD} < V_{DD-ON}$		150	200	$\mu A$
$V_{DD-OVP}$	$V_{DD}$ Over-Voltage Protection		26	27.5	28.5	V
$V_{DD-OVP-HYST}$	Hysteresis Voltage for $V_{DD}$ OVP		1.8	2.1	2.4	V
$t_{VDD-OVP}$	$V_{DD}$ OVP Debounce Time		40	70	100	$\mu s$
<b>Output Driver Section</b>						
$V_Z$	Gate Output Clamp Voltage		10	12	14	V
$V_{OL}$	Output Voltage Low	$V_{DD}=6V, I_O=50mA$			0.5	V
$V_{OH}$	Output Voltage High	$V_{DD}=6V, I_O=50mA$	4			V
$t_R$	Rising Time	$V_{DD}=12V, C_L=6nF, OUT=2V\sim 9V$	30	70	120	ns
		$V_{DD}=6V, C_L=6nF, OUT=0.4V\sim 4V$	70	120	170	ns
$t_F$	Falling Time	$V_{DD}=12V, C_L=6nF, OUT=9V\sim 2V$	20	50	100	ns
		$V_{DD}=6V, C_L=6nF, OUT=4V\sim 0.4V$	20	90	130	ns
$t_{PD\_HIGH\_LPC}$	Propagation Delay to OUT HIGH (LPC Trigger)	$t_R: 0V\sim 2V, V_{DD}=12V$		250		ns
$t_{PD\_LOW\_LPC}$	Propagation Delay to OUT LOW (LPC Trigger) <sup>(3)</sup>	$t_F: 100\%\sim 90\%, V_{DD}=12V$		180		ns
$t_{MAX-PERIOD}$	Limitation between LPC Rising Edge to Gate Falling Edge		22.5	25.0	28.0	$\mu s$
$V_{PMOS-ON}$	Internal PMOS Turn-On to Pull-HIGH Gate <sup>(3)</sup>			8.3		V
$V_{PMOS-ON-HYS}$	Hysteresis Voltage On <sup>(3)</sup>			0.9		V
$t_{INHIBIT}$	Gate Inhibit Time	M2 Option (Enable)	1.6	2.2	2.8	$\mu s$
$V_{GATE-PULL-HIGH}$	Gate Pull-HIGH Voltage	$V_{DD}=5V$	4.5			V
<b>LPC Section</b>						
$t_{BNK}$	Blanking Time for Charging CT		400	500	600	ns
$t_{DELAY-COMP}$	Sampling Continuous Time for $t_{BNK}$ Compensation <sup>(3)</sup>			1		$\mu s$
$V_{LPC-SOURCE}$	LPC Lower Clamp Voltage	Source $I_{LPC}=5\mu A$	0.1	0.2	0.3	V
$I_{LPC-SOURCE}$	LPC Source Current	$V_{LPC}=0V$	40	80	120	$\mu A$
$V_{LPC-EN}$	SR Enabled Threshold Voltage	$V_{LPC-EN}=V_{LPC-HIGH} \times 0.83$ at $V_{LPC-HIGH} \times 0.83 < 2V, V_O=15V, V_O=V_{DD}, V_{LPC-HIGH}=1.2V$	0.85	1.00	1.15	V
$V_{EN-CLAMP}$	SR Enable Threshold Clamp Voltage	$V_{LPC-EN}=2V$ at $V_{LPC-HIGH} \times 0.83 > 2V$		2		V
$V_{LPC-TH-HIGH}$	Threshold Voltage on LPC Rising Edge	$0.05V_O+0.05, V_O=15V, V_O=V_{DD}$	0.7	0.8	0.9	V
$t_{BNK-DIS}$	Blanking Time LPC is HIGH During SR Gate Turn-On Period	Prevent LPC Spike to Turn-Off Gate		350		ns

## Electrical Characteristics

V<sub>DD</sub>=15V and T<sub>A</sub>=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>LPC Section</b> (Continued)						
V <sub>LPC-CLAMP-H</sub>	Higher Clamp Voltage <sup>(3)</sup>			6		V
V <sub>LPC-DIS</sub>	LPC Voltage to Disable SR Gate		4.0	4.2	4.4	V
t <sub>LPC-HIGH</sub>	Debounce Time for Disable SR Gate			1		μs
t <sub>LPC-EN-RES</sub>	No LPC Signal, Reset V <sub>LPC-EN</sub>			100		μs
<b>RES Section</b>						
V <sub>RES-EN</sub>	Threshold Voltage of V <sub>RES</sub> to Enable SR MOS		0.60	0.75	0.90	V
t <sub>RES-LOW</sub>	Debounce Time for Disable RES Function			1	2	μs
V <sub>RES-CLAMP-H</sub>	Higher Clamp Voltage <sup>(3)</sup>			6		V
K <sub>RES-DROP</sub>	RES Dropping Protection Ratio within One Cycle			90		%
t <sub>RES-DROP</sub>	Debounce Time for RES Dropping Protection			1.5		μs
<b>Internal Timing Section</b>						
t <sub>CT</sub>	Linear Operation Range of CT	V <sub>LPC</sub> =1.5V	27	30	33	μs
V <sub>LPC-OP</sub>	Linear Operation Range of LPC for CT Charge	V <sub>DD</sub> <5V	0.8		3.4	V
		V <sub>DD</sub> >5V	0.8		4.0	V
V <sub>RES-OP</sub>	Linear Operation Range of V <sub>DD-RES</sub> for CT Discharge	V <sub>DD</sub> <5V	0.8		3.4	V
		V <sub>DD</sub> >5V	0.8		4.0	V
Ratio <sub>LPC-RES</sub>	Ratio Between LPC and RES		4.65	5.00	5.35	
t <sub>LPC-EN</sub>	Minimum LPC Time to Enable SR_Gate, V <sub>DET</sub> >V <sub>DET_TH_HIGH</sub>		0.9	1.1	1.3	μs
t <sub>gate-limit</sub>	t <sub>on-SR</sub> (n+1) < t <sub>gate-limit</sub> × t <sub>on-SR</sub> (n)		105		120	%
<b>Green Section</b>						
t <sub>GREEN-OFF</sub>	CT Capacitor t <sub>DIS</sub> Time to Leave Green Mode	f <sub>S</sub> =65KHz	4.60	5.35	6.10	μs
t <sub>GREEN-ON</sub>	CT Capacitor t <sub>DIS</sub> Time to Enter Green Mode	f <sub>S</sub> =65KHz	4.25	4.80	5.35	μs
t <sub>GREEN-TIME-enter</sub>	Cycle Time to Enter Green Mode	CT Discharge Time < t <sub>GREEN-ON</sub>		3		Times
t <sub>GREEN-TIME-leave</sub>	Cycle Time to Leave Green Mode	CT Discharge Time > t <sub>GREEN-OFF</sub>		7		Times
t <sub>GREEN-ENTER</sub>	No Gate Signal to Enter Green Mode <sup>(3)</sup>			75		μs
<b>Causal Function Section</b>						
t <sub>CAUSAL</sub>	If t <sub>S-PWM</sub> (n+1) > t <sub>CAUSAL</sub> × t <sub>S-PWM</sub> (n) → SR Stops Switching, Enter Green Mode	f <sub>S</sub> =65KHz → 40KHz		120		%
t <sub>DEAD-CAUSAL</sub>	SR Turn-off Dead Time by Causal Function	f <sub>S</sub> =65KHz	380	580	780	ns
t <sub>DEAD-CFR</sub>	CFR Start to Shrink Timing (Last Time from SR Gate Falling to LPC Rising)	CFR (Causal Function Regulator)		150		ns
t <sub>DEAD-RE-CFR</sub>	SR Gate Narrowed Down Width when t <sub>DEAD-CFR</sub> Triggered			1.5		μs
<b>Internal Over-Temperature Protection Section</b>						
T <sub>OTP</sub>	Internal Threshold Temperature for OTP <sup>(3)</sup>			140		°C
T <sub>OTP-HYST</sub>	Hysteresis Temperature for Internal OTP <sup>(3)</sup>			20		°C

**Note:**

3. Guaranteed by design.

## Typical Performance Characteristics

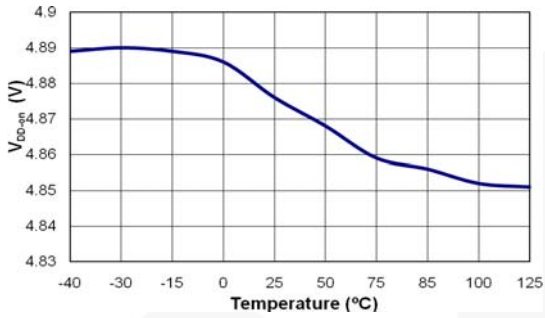


Figure 6. Turn-On Threshold Voltage

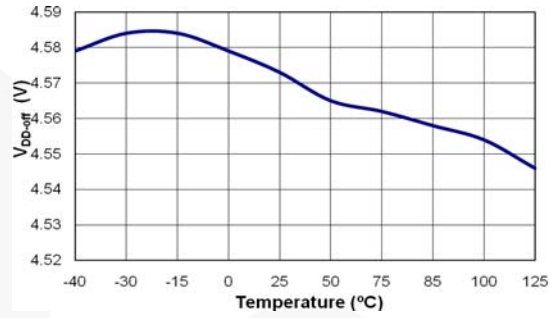


Figure 7. Turn-Off Threshold Voltage

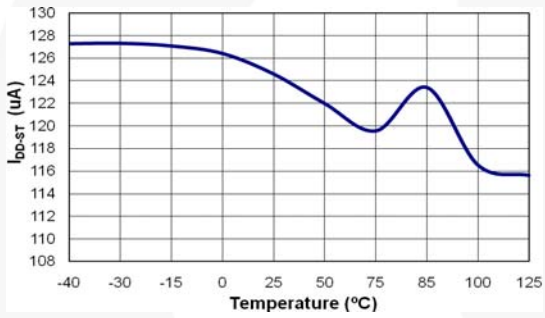


Figure 8. Startup Current

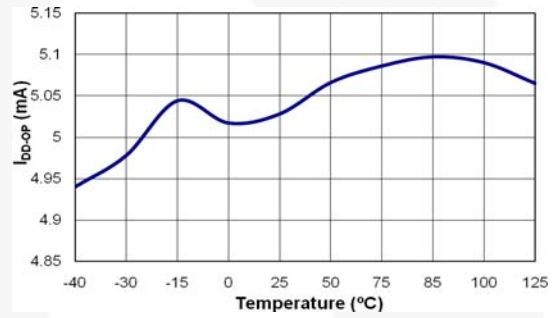


Figure 9. Operating Current

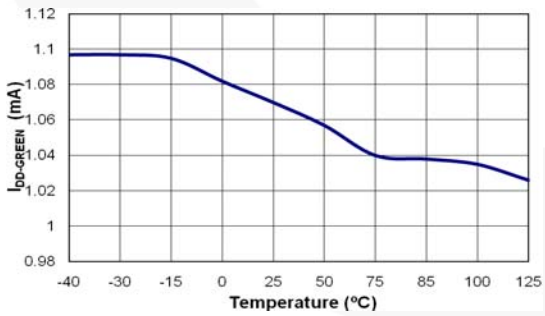


Figure 10. Operating Current in Green Mode

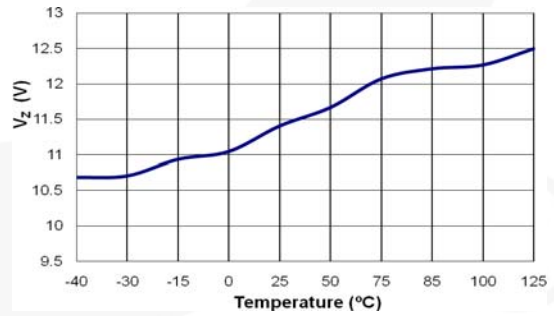


Figure 11. Gate Output Clamping Voltage

Typical Performance Characteristics (Continued)

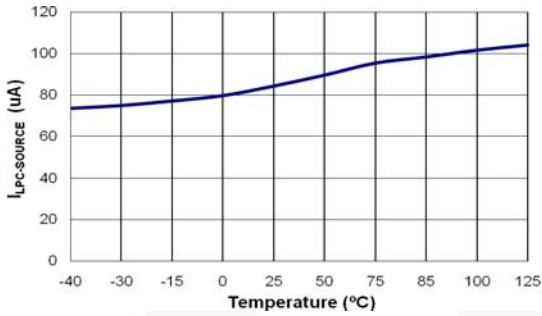


Figure 12. LPC Source Current

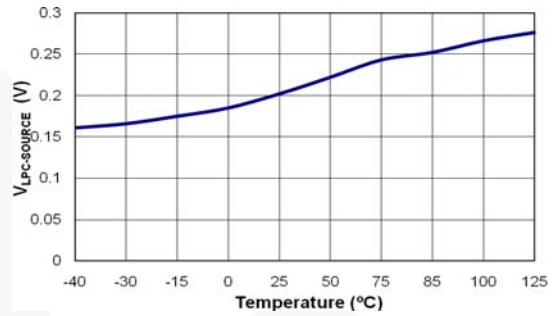


Figure 13. LPC Lower Clamp Voltage

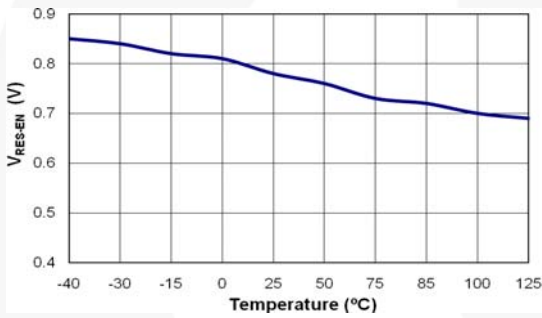


Figure 14. Threshold Voltage of V<sub>RES</sub>

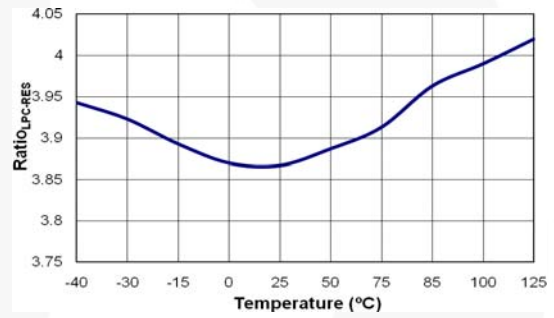


Figure 15. Ratio between LPC and RES

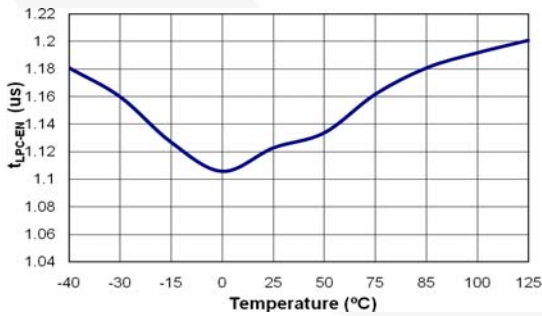


Figure 16. Minimum LPC Enable Time

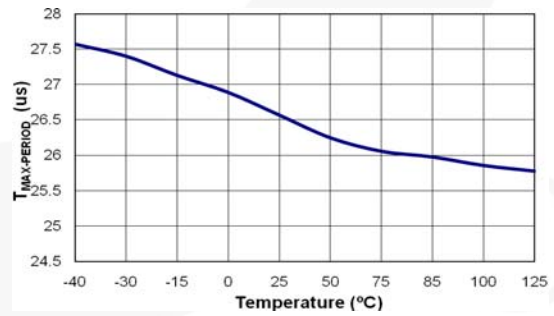


Figure 17. Maximum Time between LPC Rising Edge to Gate Falling Edge



## Functional Description

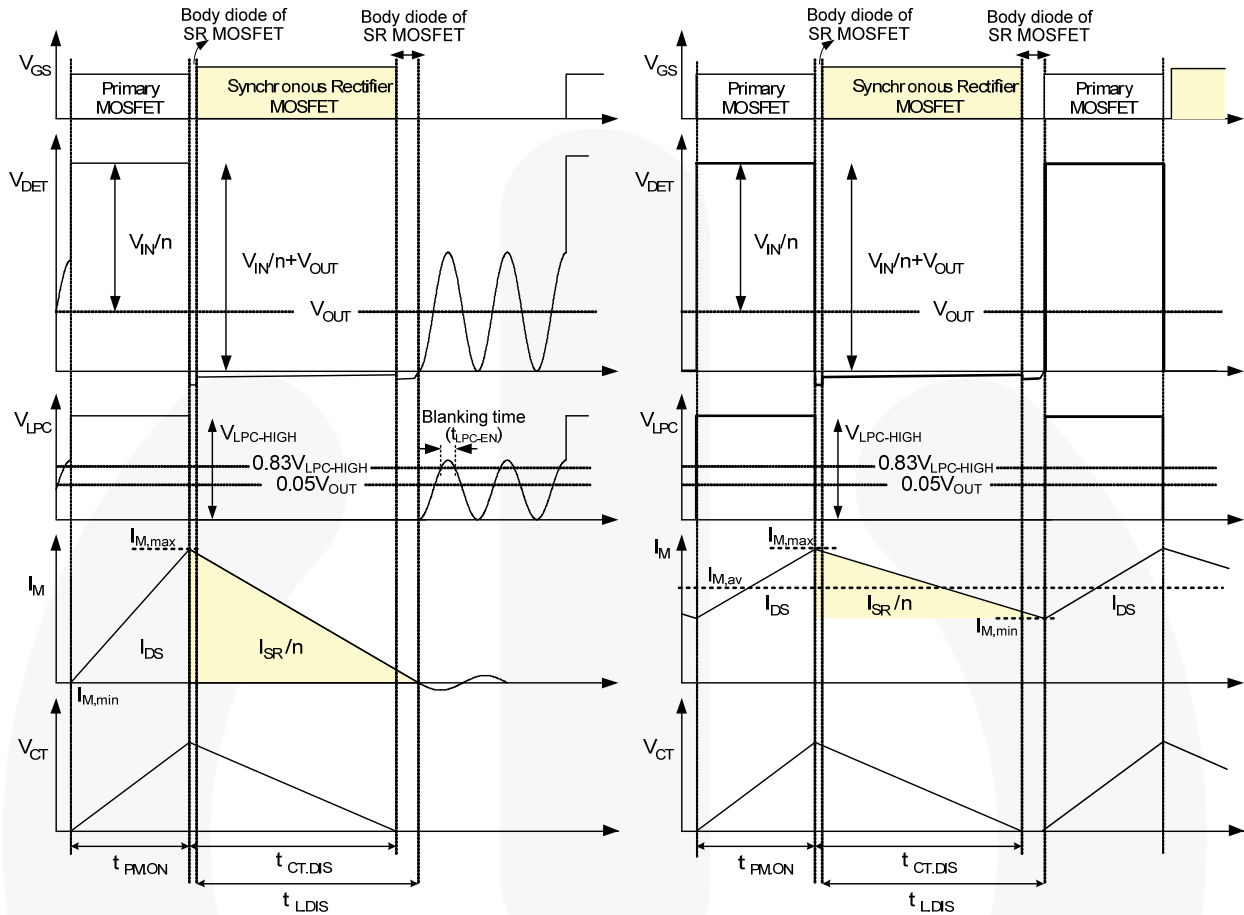


Figure 18. Typical Waveforms of Linear-Predict Timing Control in CCM and DCM/QR Flyback

### Linear Predict Timing Control

The SR MOSFET turn-off timing is determined by linear-predict timing control and the operation principle is based on the volt-second balance theorem. The volt-second balance theorem states that the inductor average voltage is zero during a switching period in steady state, so the charge voltage and charge time product is equal to the discharge voltage and discharge time product. In flyback converters, the charge voltage on the magnetizing inductor is input voltage ( $V_{IN}$ ), while the discharge voltage is  $nV_{OUT}$ , as the typical waveforms show in Figure 18. The following equation can be drawn:

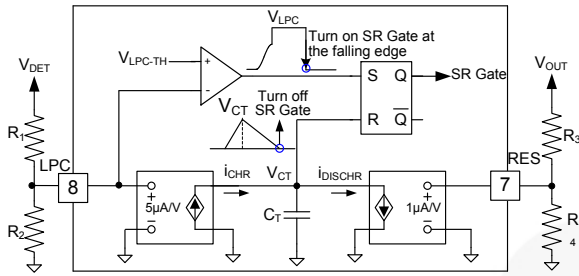
$$V_{IN} \cdot t_{PM,ON} = n \cdot V_{OUT} \cdot t_{L,DIS} \quad (1)$$

where  $t_{PM,ON}$  is inductor charge time and  $t_{L,DIS}$  is inductor discharge time.

FAN6204 uses the LPC and RES pins with two sets of voltage dividers to sense DET voltage ( $V_{DET}$ ) and output voltage ( $V_{OUT}$ ), respectively; so  $V_{IN}/n$ ,  $t_{PM,ON}$ , and  $V_{OUT}$  can be obtained. As a result,  $t_{L,DIS}$ , which is the on-time of SR MOSFET, can be predicted by Equation 1. As shown in Figure 18, the SR MOSFET is turned on when the SR MOSFET body diode starts conducting and DET voltage drops to zero. The SR MOSFET is turned off by linear-predict timing control.

### Circuit Realization

The linear-predict timing-control circuit generates a replica ( $V_{CT}$ ) of magnetizing current of flyback transformer using internal timing capacitor ( $C_T$ ), as shown in Figure 19. Using the internal capacitor voltage, the inductor discharge time ( $t_{L,DIS}$ ) can be detected indirectly, as shown in Figure 18. When  $C_T$  is discharged to zero, the SR controller turns off the SR MOSFET.



**Figure 19. Simplified Linear-Predict Block**

The voltage-second balance equation for the primary-side inductance of the flyback converter is given in Equation 1. Inductor current discharge time is given as:

$$t_{L.DIS} = \frac{V_{IN} \cdot t_{PM.ON}}{n \cdot V_{OUT}} \quad (2)$$

The voltage scale-down ratio between RES and LPC is defined as K below:

$$K = \frac{R_4 / (R_3 + R_4)}{R_2 / (R_1 + R_2)} \quad (3)$$

During  $t_{PM.ON}$ , the charge current of  $C_T$  is  $i_{CHR} - i_{DICH}$ , while during  $t_{L.DIS}$ , the discharge current is  $i_{DICH}$ . As a result, the current-second balance equation for internal timing capacitor ( $C_T$ ) can be derived from:

$$\left(\frac{5}{K} \cdot \left(\frac{V_{IN}}{n} + V_{OUT}\right) - V_{OUT}\right) \cdot t_{PM.ON} = V_{OUT} \cdot t_{CT.DIS} \quad (4)$$

Therefore, the discharge time of  $C_T$  is given as:

$$t_{CT.DIS} = \frac{\left(\frac{5}{K} \cdot \left(\frac{V_{IN}}{n} + V_{OUT}\right) - V_{OUT}\right) \cdot t_{PM.ON}}{V_{OUT}} \quad (5)$$

When the voltage scale-down ratio between RES and LPC (K) is five (5), the discharge time of  $C_T$  ( $t_{CT.DIS}$ ) is the same as inductor current discharge time ( $t_{L.DIS}$ ). However, considering the tolerance of voltage divider resistors and internal circuit, the scale-down ratio (K) should be larger than five (5) to guarantee that  $t_{CT.DIS}$  is shorter than  $t_{L.DIS}$ . It is typical to set K around 5~5.5.

Referring to Figure 18; when LPC voltage is higher than  $V_{LPC-EN}$  over a blanking time ( $t_{LPC-EN}$ ) and lower than  $V_{LPC-TH-HIGH}$  ( $0.05V_{OUT}$ ), then SR MOSFET can be triggered. Therefore,  $V_{LPC-EN}$  must be larger than  $V_{LPC-TH-HIGH}$  or the SR MOSFET cannot be turned on. When designing the voltage divider of LPC,  $R_1$  and  $R_2$  should be considered as:

$$0.83 \cdot \frac{R_2}{R_1 + R_2} \cdot \left(\frac{V_{IN.MIN}}{n} + V_{OUT}\right) > 0.05V_{OUT} + 0.3 \quad (6)$$

On the other hand, the linear operation range of LPC and RES (1~4V) should be considered as:

$$\frac{R_2}{R_1 + R_2} \cdot \left(\frac{V_{IN.MAX}}{n} + V_{OUT}\right) < 4 \quad (7)$$

$$\frac{R_4}{R_3 + R_4} \cdot V_{OUT} < 4 \quad (8)$$

## CCM Operation

The typical waveforms of CCM operation in steady state are shown as Figure 18. When the primary-side MOSFET is turned on, the energy is stored in  $L_m$ . During the on-time of the primary-side MOSFET ( $t_{PM.ON}$ ), the magnetizing current ( $I_M$ ) increases linearly from  $I_{M,min}$  to  $I_{M,max}$ . Meanwhile, internal timing capacitor ( $C_T$ ) is charged by current source ( $i_{CHR} - i_{DICH}$ ) proportional to  $V_{IN}$ , so  $V_{CT}$  also increases linearly.

When the primary-side MOSFET is turned off, the energy stored in  $L_m$  is released to the output. During the inductor discharge time ( $t_{L.DIS}$ ), the magnetizing current ( $I_M$ ) decreases linearly from  $I_{M,max}$  to  $I_{M,min}$ . At the same time, the internal timing capacitor ( $C_T$ ) is discharged by current source ( $i_{DICH}$ ) proportional to  $V_{OUT}$ , so  $V_{CT}$  also decreases linearly. To guarantee the proper operation of SR, it is important to turn off SR MOSFET just before SR current reaches  $I_{M,min}$  so that the body diode of SR MOSFET is naturally turned off.

## DCM / QR Operation

In DCM / QR operation, when primary-side MOSFET is turned off, the energy stored in  $L_m$  is fully released to the output at the turn-off timing of primary-side MOSFET. Therefore, the DET voltage continues resonating until the primary-side MOSFET is turned on, as depicted in Figure 18. While DET voltage is resonating, DET voltage and LPC voltage drop to zero by resonance, which can trigger the turn-on of the SR MOSFET. To prevent fault triggering of the SR MOSFET in DCM operation, blanking time is introduced to LPC voltage. The SR MOSFET is not turned on even when LPC voltage drops below  $0.05V_{OUT}$  unless LPC voltage stays above  $0.83V_{LPC-HIGH}$  longer than the blanking time ( $t_{LPC-EN}$ ). The turn-on timing of the SR MOSFET is inhibited by gate inhibit time ( $t_{INHIBIT}$ ), once the SR MOSFET turns off, to prevent fault triggering.

## mWSaver™ Technology

### Green-Mode Operation

To minimize the power consumption at light-load condition, the SR circuit is disabled when the load decreases. As illustrated in Figure 20, the discharge times of inductor and internal timing capacitor decrease as load decreases. If the discharge time of the internal timing capacitor is shorter than  $t_{GREEN-ON}$  (around  $4.8\mu s$ ) for more than three cycles, the SR circuit enters Green Mode. Once FAN6204 enters Green Mode, the SR MOSFET stops switching and the major internal block is shut down to further reduce operating current of the SR controller. In Green Mode, the operating current reduces to 1.1mA. This allows power supplies to meet the most stringent power conservation requirements. When the discharge time of the internal capacitor is longer than  $t_{GREEN-OFF}$  (around  $5.35\mu s$ ) for more than seven cycles, the SR circuit is enabled and resumes the normal operation, as shown in Figure 21.

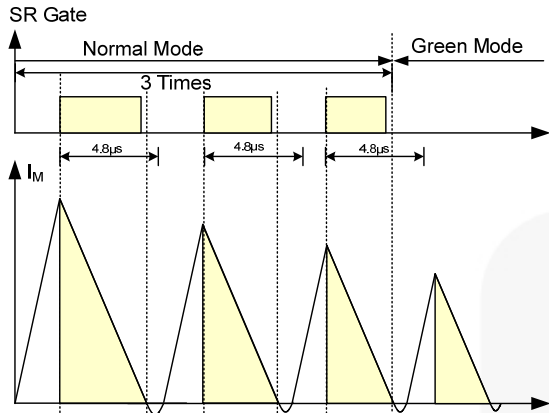


Figure 20. Entering Green Mode

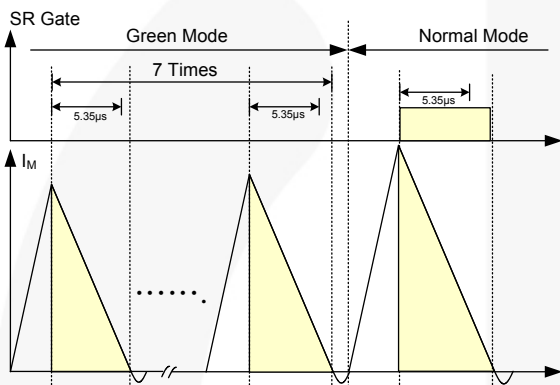


Figure 21. Resuming Normal Operation

### Causal Function

Causal function is utilized to limit the time interval ( $t_{SR-MAX}$ ) from the rising edge of  $V_{LPC}$  to the falling edge of the SR gate.  $t_{SR-MAX}$  is limited to 97% of previous switching period, as shown in Figure 22. When the system operates at fixed frequency, whether voltage-second balance theorem can be applied or not, causal function can guarantee reliable operation.

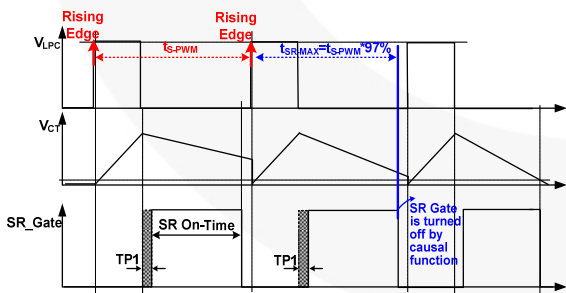


Figure 22. Causal Function Operation

### Fault Causal Timing Protection

Fault causal timing protection is utilized to disable the SR gate under some abnormal conditions. Once the switching period ( $t_{S-PWM}(n)$ ) is longer than 120% of previous switching period ( $t_{S-PWM}(n-1)$ ), SR gate is disabled and enters Green Mode, as shown in Figure 23. Since the rising edge of  $V_{LPC}$  among switching

periods ( $t_{S-PWM}$ ) is tracked for causal function, the accuracy of switching period is important. Therefore, if the detected switching period has a serious variation under some abnormal conditions, the SR gate should be terminated to prevent fault trigger.

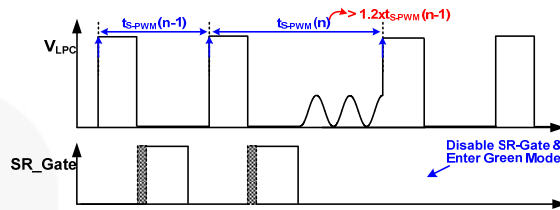


Figure 23. Fault Causal Timing Protection

### Gate Expand Limit Protection

Gate expand limit protection controls on-time expansion of the SR MOSFET. Once the discharge time of the internal timing capacitor ( $t_{DIS,CT}$ ) is longer than 115% of previous on time of the SR MOSFET ( $t_{ON-SR}(n-1)$ );  $t_{ON-SR}(n)$  is limited to 115% of  $t_{ON-SR}(n-1)$ , as shown in Figure 24. When output load changes rapidly from light load to heavy load, voltage-second balance theorem may not be applied. In this transient state, gate expand limit protection is activated to prevent overlap between SR gate and PWM gate.

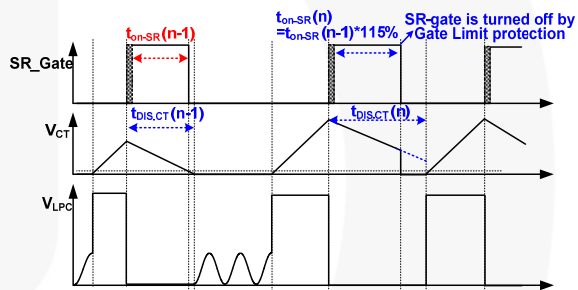


Figure 24. Gate Expand Limit Protection

### RES Dropping Protection

RES dropping protection prevents  $V_{RES}$  dropping too much within a cycle. The  $V_{RES}$  is sampled as a reference voltage,  $V_{RES}'$ , on  $V_{LPC}$  rising edge. Once  $V_{RES}$  drops below 90% of  $V_{RES}'$  for longer than a debounce time ( $t_{RES-DROP}$ ), the SR gate is turned off immediately, as shown in Figure 25. When output voltage drops rapidly within a switching cycle, voltage-second balance may not be applied, RES dropping protection is activated to prevent overlap.

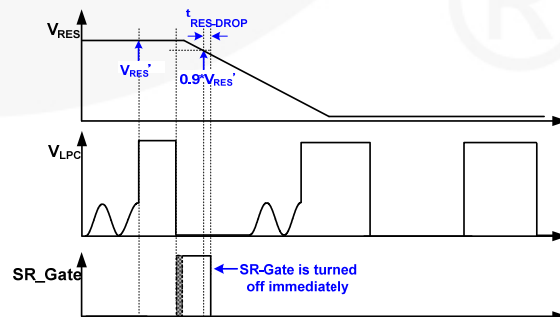


Figure 25.  $V_{RES}$  Dropping Protection

### LPC Pin Open / Short Protection

**LPC-Open Protection:** If  $V_{LPC}$  is higher than  $V_{LPC-DIS}$  (4.2V) for longer than debounce time  $t_{LPC-HIGH}$ , FAN6204 stops switching immediately and enters Green Mode.  $V_{LPC}$  is clamped at 6V to avoid LPC pin damage.

**LPC-Short Protection:** If  $V_{LPC}$  is pulled to ground and the charging current of timing capacitor ( $C_T$ ) is near zero, SR gate is not output.

### RES Pin Open / Short Protection

**RES-Open Protection:** If  $V_{RES}$  is pulled to HIGH level, the gate signal is extremely small and FAN6204 enters Green Mode. In addition,  $V_{RES}$  is clamped at 6V to avoid RES pin damage.

**RES-Short Protection:** If  $V_{RES}$  is lower than  $V_{RES-EN}$  (0.7V) for longer than debounce time  $t_{RES-LOW}$ , FAN6204 stops switching immediately and enters Green Mode.

### Under-Voltage Lockout (UVLO)

The power ON and OFF  $V_{DD}$  threshold voltages are fixed at 4.8V and 4.5V, respectively. With an ultra-low  $V_{DD}$  threshold voltage, the FAN6204 can be used in various output voltage applications.

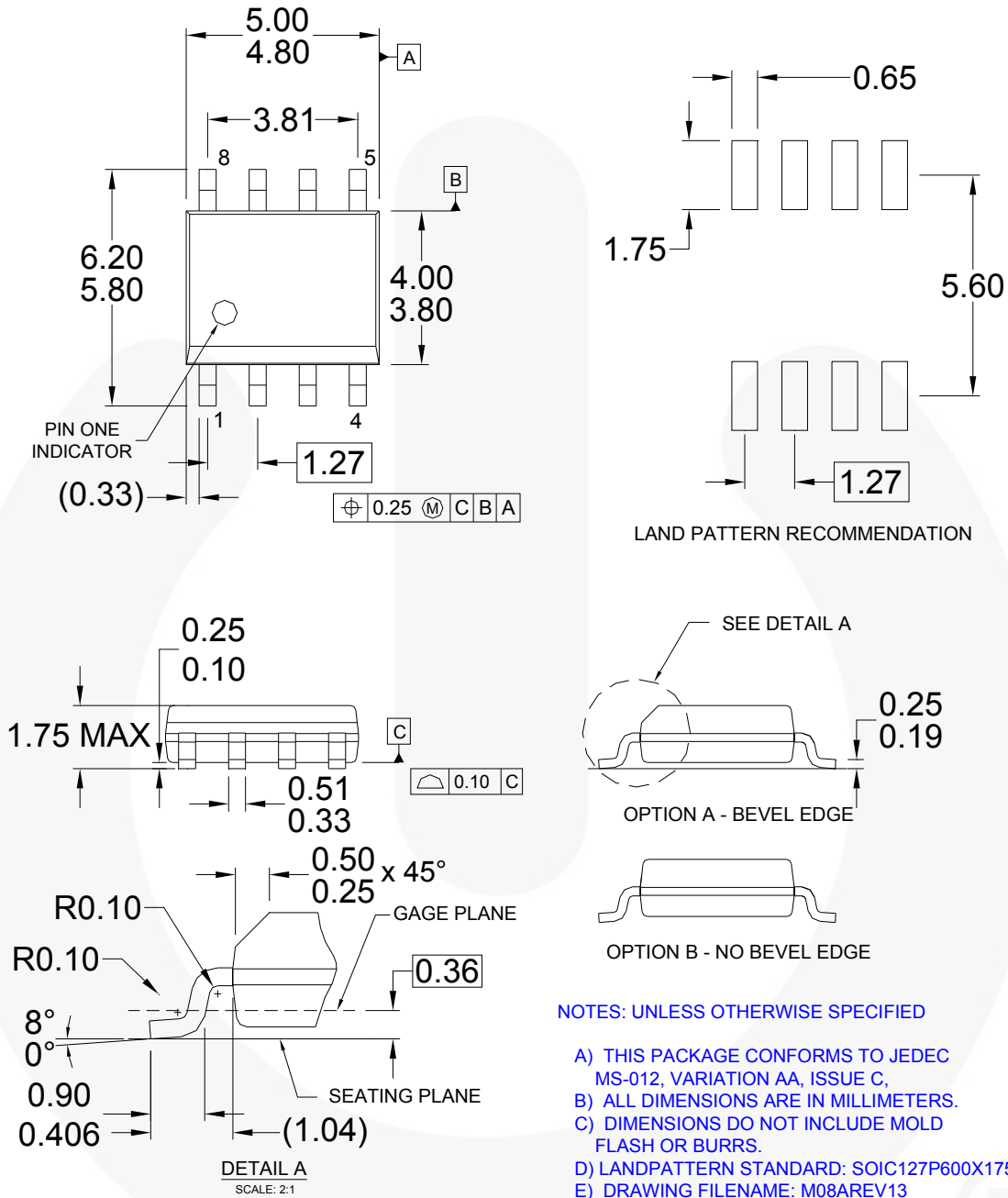
### $V_{DD}$ Pin Over-Voltage Protection (OVP)

Over-voltage conditions are usually caused by an open feedback loop.  $V_{DD}$  over-voltage protection prevents damage on the SR MOSFET. When the voltage on VDD pin exceeds 27.5V, the SR controller stops switching the SR MOSFET.

### Over-Temperature Protection (OTP)

To prevent SR gate from fault triggering in high temperatures, internal over-temperature protection is integrated in FAN6204. Once the temperature is over 140°C, SR gate is disabled until the temperature drops below 120°C.

### Physical Dimensions



**Figure 26. 8-Pin, Small Outline Package (SOP)**




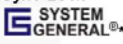
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Rev. I62