800mA, Single Cell Li-Ion and Li-Pol Battery Charger With Automatic Adaptor and USB Detection

Check for Samples: bq24050, bq24052, bq24055

FEATURES

- CHARGING
  - 1% Charge Voltage Accuracy
  - 10% Charge Current Accuracy
  - Pin Selectable USB 100mA and 500mA Maximum Input Current Limit
  - Programmable Termination and Precharge Threshold
- PROTECTION
  - 30V Input Rating; with 6.6V Input Overvoltage Protection
  - Input Voltage Dynamic Power Management
  - 125°C Thermal Regulation; 150°C Thermal Shutdown Protection
  - OUT Short-Circuit Protection and ISET short detection
  - Operation over JEITA Range via Battery NTC - ½ Fast-Charge-Current at Cold, 4.06V at Hot
  - Fixed 10 Hour Safety Timer
- SYSTEM
  - Auto Input Source Detection (D+,D– Pins)
    - No Device Transceiver Required
    - USB Friendly
  - Automatic Termination and Timer Disable Mode (TTDM) for Absent Battery Pack With Thermistor
  - Status Indication – Charging/Done
  - Available in Small 2×2mm^2 DFN-10 or 2×3mm^2 DFN-12 Packages

APPLICATIONS

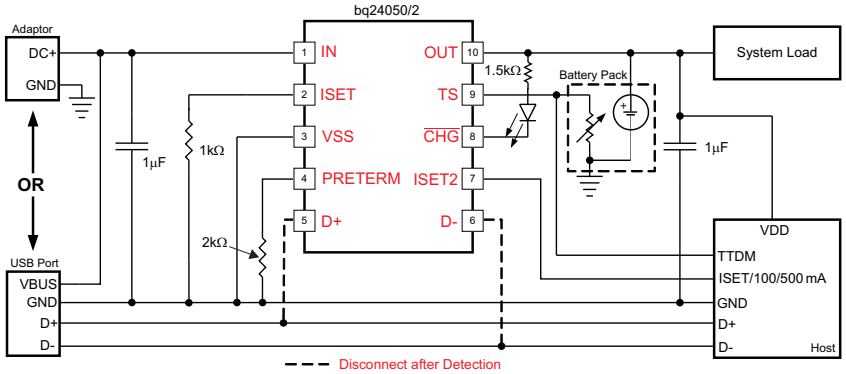
- Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices

DESCRIPTION

The bq2405x series of devices are highly integrated Li-Ion and Li-Pol linear chargers devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

The bq2405x has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. (Description continued on next page)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The precharge current and termination current threshold are programmed via an external resistor. The fast charge current value is also programmable via an external resistor.

AVAILABLE OPTIONS

$V_{O(REG)}$	V_{OVP}	R_{NTC}	$\overline{PG}$	PACKAGE	DEVICES	MARKING
4.2 V	6.6 V	10 kΩ	No	10 PIN 2 × 2mm^2 DFN	bq24050	CVC
4.2 V	6.6 V	100 kΩ	No	10 PIN 2 × 2mm ^{2} DFN	bq24052	CGT
4.2 V	6.6 V	10 kΩ	Yes	12 PIN 2 × 3mm ^{2} DFN	bq24055	CGU

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
	Input Voltage	IN (with respect to VSS)		–0.3 to 30	V
		OUT (with respect to VSS)		–0.3 to 7	V
		PRE-TERM, ISET, ISET2, TS, $\overline{CHG}$, $\overline{PG}$, D+, D–, (with respect to VSS)		–0.3 to 7	V
	Input Current	IN		1.25	A
	Output Current (Continuous)	OUT		1.25	A
	Output Sink Current	$\overline{CHG}$		15	mA
ESD	Electrostatic discharge (IEC61000-4-2)(2)	IN, OUT, TS	1µF between IN and GND, 1µF between TS and GND, 2µF between OUT and GND, x5R Ceramic or equivalent	8 contact 15 Air	kV
T_J	Junction temperature			–40 to 150	°C
T_{STG}	Storage temperature			–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) The test was performed on IC pins that may potentially be exposed to the customer at the product level. The bq2405x IC requires a minimum of the listed capacitance, external to the IC, to pass the ESD test. The D+ D- lines require clamp diodes such as CM1213A-02SR from CMD to protect the IC for this testing.

PACKAGE DISSIPATION RATINGS(1) (2)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR $T_A > 25°C$
2 × 2 mm^2	60°C/W	8.8°C/W	1.66W	16.6mW/°C
2 × 3 mm^2	58°C/W	5.3°C/W	1.72W	17.2mW/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2×3 via matrix

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	NOM	UNIT
V_{IN}	IN voltage range	3.5	28	V
	IN operating voltage range, Restricted by V_{DPM} and V_{OVP}	4.45	6.45	V
I_{IN}	Input current, IN pin		0.8	A
I_{OUT}	Current, OUT pin		0.8	A
T_J	Junction temperature	0	125	°C
$R_{PRE-TERM}$	Programs precharge and termination current thresholds	1	10	kΩ
R_{ISET}	Fast-charge current programming resistor	0.675	49.9	kΩ
R_{TS}	10k NTC thermistor range without entering TTDM, bq24050/55	1.66	258	kΩ
	100k NTC thermistor range without entering TTDM, bq24052	24	885	kΩ

(1) Operation with V_{IN} less than 4.5V or in drop-out may result in reduced performance.

ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out Exit	V_{IN}: 0V → 4V Update based on sim/char	3.15	3.3	3.45	V
V_{HYS_UVLO}	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 4V→0V, $V_{UVLO\_FALL} = V_{UVLO\_RISE} – V_{HYS-UVLO}$	175	230	280	mV
V_{IN-DT}	Input power good detection threshold is $V_{OUT} + V_{IN-DT}$	(Input power good if $V_{IN} > V_{OUT} + V_{IN-DT}$); V_{OUT} = 3.6V, V_{IN}: 3.5V → 4V	30	80	145	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6V, V_{IN}: 4V → 3.5V		31		mV
$t_{DGL(\overline{PG}\_PWR)}$	Deglitch time on exiting sleep.	Time measured from V_{IN}: 0V → 5V 1µs rise-time to $\overline{PG}$ = low, V_{OUT} = 3.6V		45		µs
$t_{DGL(\overline{PG}\_NO-PWR)}$	Deglitch time on $V_{HYS-INDT}$ power down. Same as entering sleep.	Time measured from V_{IN}: 5V → 3.2V 1µs fall-time to $\overline{PG}$ = High Z, V_{OUT} = 3.6V		29		ms
V_{OVP}	Input over-voltage protection threshold	V_{IN}: 5V → 7V (50/52/55)	6.5	6.65	6.8	V
$t_{DGL(OVP-SET)}$	Input over-voltage blanking time	V_{IN}: 5V → 12V		113		µs
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11V → 5V		95		mV
$t_{DGL(OVP-REC)}$	Deglitch time exiting OVP	Time measured from V_{IN}: 12V → 5V 1µs fall-time to $\overline{PG}$ = LO		30		µs
V_{IN-DPM}	USB/Adaptor low input voltage protection. Restricts Iout at V_{IN-DPM}	Feature active in USB mode; Limit Input Source Current to 50mA; V_{OUT}=3.5V; R_{ISET} = 825Ω	4.34	4.4	4.46	V
		Feature active in Adaptor mode; Limit Input Source Current to 50mA; V_{OUT}=3.5V; R_{ISET} = 825Ω	4.24	4.3	4.36	
$I_{IN-USB-CL}$	USB input I-Limit 100mA	ISET2 = Float; R_{ISET} = 825Ω	85	92	100	mA
	USB input I-Limit 500mA	ISET2 = High; R_{ISET} = 825Ω	430	462	500	
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest Resistor value considered a fault (short). Monitored for Iout>90mA	Riset: 600Ω → 250Ω, Iout latches off. Cycle power to Reset. USB100 mode.	280		500	Ω
t_{DGL_SHORT}	Deglitch time transition from ISET short to Iout disable	Clear fault by cycling IN or TS		1		ms
I_{OUT_CL}	Maximum OUT current limit Regulation (Clamp)	V_{IN} = 5V, V_{OUT} = 3.6V, V_{ISET2} =Low, Riset: 600Ω → 250Ω, Iout latches off after $t_{DGL-SHORT}$	1.05		1.4	A
BATTERY SHORT PROTECTION						
$V_{OUT(SC)}$	OUT pin short-circuit detection threshold/ precharge threshold	V_{OUT}:3V → 0.5V, no deglitch	0.75	0.8	0.85	V
$V_{OUT(SC-HYS)}$	OUT pin Short hysteresis	Recovery ≥ $V_{OUT(SC)} + V_{OUT(SC-HYS)}$; Rising, no Deglitch		77		mV
$I_{OUT(SC)}$	Source current to OUT pin during short-circuit detection		10	15	20	mA

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT pin	V_{IN} = 0V			1	µA
$I_{OUT(DONE)}$	OUT pin current, charging terminated	V_{IN} = 6V, V_{OUT} > $V_{OUT(REG)}$			6	µA
$I_{IN(STDBY)}$	Standby current into IN pin	TS = LO, V_{IN} ≤ 6V			125	µA
I_{CC}	Active supply current, IN pin	TS = open, V_{IN} = 6V, TTDM – no load on OUT pin, V_{OUT} > $V_{OUT(REG)}$, IC enabled		0.8	1	mA
BATTERY CHARGER FAST-CHARGE						
$V_{OUT(REG)}$	Battery regulation voltage	V_{IN} =5.5V, I_{OUT} =25mA, $V_{TS-45°C}$≤ V_{TS} ≤ $V_{TS-0°C}$	4.16	4.20	4.23	V
$V_{O\_HT(REG)}$	Battery hot regulation Voltage	V_{IN} =5.5V, I_{OUT} =25mA, $V_{TS-60°C}$≤ V_{TS} ≤ $V_{TS-45°C}$	4.02	4.06	4.1	V
$I_{OUT(RANGE)}$	Programmed Output “fast charge” current range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}, V_{IN} = 5V, ISET2=Lo, R_{ISET} = 675 to 10.8kΩ	10		800	mA
$V_{DO(IN-OUT)}$	Drop-Out, VIN – VOUT	Adjust VIN down until I_{OUT} = 0.5A, V_{OUT} = 4.15V, R_{ISET} = 675 , ISET2=Lo (Adaptor Mode); Tj ≤ 100°C		325	500	mV
I_{OUT}	Output “fast charge” formula	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}, V_{IN} = 5V, ISET2=Lo		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor	R_{ISET} = K_{ISET} /I_{OUT} 50 < I_{OUT} < 800 mA	510	540	570	AΩ
		R_{ISET} = K_{ISET} /I_{OUT} 25 < I_{OUT} < 50 mA	480	527	600	AΩ
		R_{ISET} = K_{ISET} /I_{OUT} 10 < I_{OUT} < 25 mA	350	520	680	AΩ
PRECHARGE – SET BY PRETERM PIN						
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			70		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			32		ms
$I_{PRE-TERM}$	Refer to the Termination Section					
$\%_{PRECHG}$	Pre-Charge Current Level, Default Setting	V_{OUT} < V_{LOWV}; **$R_{PRE-TERM}$ = High Z** (≥13kΩ); R_{ISET} = 1k	18	20	22	$\%I_{OUT-CC}$
	Pre-charge current formula	$R_{PRE-TERM}$ = $K_{PRE-CHG}$ (Ω/%) × $\%_{PRE-CHG}$ (%)		$R_{PRE-TERM}/K_{PRE-CHG}$		
$K_{PRE-CHG}$	% Pre-charge Factor	V_{OUT} < V_{LOWV}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2k to 10kΩ; R_{ISET} = 1080Ω , $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 20 to 100%	90	100	110	Ω/%
		V_{OUT} < V_{LOWV}, V_{IN} = 5V, $R_{PRE-TERM}$ = 1k to 2kΩ; R_{ISET} = 1080Ω, $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10% to 20%	84	100	117	Ω/%
TERMINATION – SET BY PRE-TERM PIN						
$\%_{TERM}$	Termination Current Threshold, Default Setting	V_{OUT} > V_{RCH}; **$R_{PRE-TERM}$ = High Z** (≥13kΩ); R_{ISET} = 1k	9	10	11	$\%I_{OUT-CC}$
	Termination Current Threshold Formula	$R_{PRE-TERM}$ = K_{TERM} (Ω/%) × %TERM (%)		$R_{PRE-TERM}/ K_{TERM}$		
K_{TERM}	% Term Factor	V_{OUT} > V_{RCH}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2k to 10kΩ ; R_{ISET} = 750Ω; K_{TERM} × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10 to 50%	182	200	216	Ω/%
		V_{OUT} > V_{RCH}, V_{IN} = 5V, $R_{PRE-TERM}$ = 1k to 2kΩ ; R_{ISET} = 750Ω; K_{TERM} × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 5 to 10%	174	199	224	Ω/%
$I_{PRE-TERM}$	Current for programming the term. and pre-chg with resistor. $I_{Term-Start}$ is the initial PRE-TERM curent.	$R_{PRE-TERM}$ = 2k, V_{OUT} = 4.15V	71	75	81	µA
%TERM	Termination current formula			R_{TERM}/ K_{TERM}		%
$t_{DGL(TERM)}$	Deglitch time, termination detected			29		ms
$I_{Term-Start}$	Elevated PRE-TERM current for, $t_{Term-Start}$, during start of charge to prevent recharge of full battery,		80	85	92	µA
$t_{Term-Start}$	Elevated termination threshold initially active for $t_{Term-Start}$			1.25		min

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold – Normal Temp	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT}: 4.25V → V_{RCH}	$V_{O(REG)}$-0.120	$V_{O(REG}$ -0.095	$V_{O(REG)}$-0.070	V
	Recharge detection threshold – Hot Temp	V_{IN} = 5V, V_{TS} = 0.2V, V_{OUT}: 4.15V → V_{RCH}	$V_{O\_HT(REG)}$ -0.130	$V_{O\_HT(REG)}$ -0.105	$V_{O\_HT(REG)}$ -0.080	V
$t_{DGL1(RCH)}$	Deglitch time, recharge threshold detected	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT}: 4.25V → 3.5V in 1µs; $t_{DGL1(RCH)}$ is time to ISET ramp		29		ms
$t_{DGL2(RCH)}$	Deglitch time, recharge threshold detected in OUT-Detect Mode	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT} = 3.5V inserted; $t_{DGL2(RCH)}$ is time to ISET ramp		3.6		ms
BATTERY DETECT ROUTINE (NOTE: In Hot Mode $V_{O(REG)}$ becomes $V_{O\_HT(REG)}$)						
V_{REG-BD}	VOUT Reduced regulation during battery detect	V_{IN} = 5V, V_{TS} = 0.5V, Battery Absent	$V_{O(REG)}$-0.450	$V_{O(REG}$ -0.400	$V_{O(REG)}$-0.350	V
$I_{BD-SINK}$	Sink current during V_{REG-BD}		7		10	mA
$t_{DGL(HI/LOW REG)}$	Regulation time at V_{REG} or V_{REG-BD}			25		ms
V_{BD-HI}	High battery detection threshold	V_{IN} = 5V, V_{TS} = 0.5V, Battery Absent	$V_{O(REG)}$-0.150	$V_{O(REG)}$-0.100	$V_{O(REG)}$-0.050	V
V_{BD-LO}	Low battery detection threshold	V_{IN} = 5V, V_{TS} = 0.5V, Battery Absent	V_{REG-BD} +0.050	V_{REG-BD} +0.100	V_{REG-BD} +0.150	V
BATTERY CHARGING TIMERS AND FAULT TIMERS						
t_{PRECHG}	Pre-charge safety timer value	Restarts when entering Pre-charge; Always enabled when in pre-charge.	1700	1940	2250	s
t_{MAXCH}	Charge safety timer value	Clears fault or resets at UVLO, TS ("CE") disable, OUT Short, exiting LOWV and Refresh	34000	38800	45000	s
BATTERY-PACK NTC MONITOR (Note 1); TS pin: bq24050/5: 10k NTC; bq24052: 100k NTC; See TS section for thermistor information						
$I_{NTC-10k}$	NTC bias current; 10k NTC thermsistor, bq24050/5	V_{TS} = 0.3V	48	50	52	µA
$I_{NTC-100k}$	NTC bias current; 100k NTC thermsistor, bq24052	V_{TS} = 0.3V	4.8	5	5.2	µA
$I_{NTC-DIS-10k}$	bq24050/5 bias current when Charging is disabled.	V_{TS} = 0V	27	30	34	µA
$I_{NTC-DIS-100k}$	bq24052 bias current when Charging is disabled.	V_{TS} = 0V	4.4	5	5.8	µA
$I_{NTC-FLDBK-10k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM, bq24050/5	V_{TS}: Set to 1.525V	4	5	6.5	µA
$I_{NTC-FLDBK-100k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM, bq24052	V_{TS}: Set to 1.525V	1.1	1.5	1.9	µA
$V_{TTDM(TS)}$	Termination and timer disable mode Threshold – Enter	V_{TS}: 0.5V → 1.7V; Timer Held in Reset	1550	1600	1650	mV
$V_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7V → 0.5V; Timer Enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS}= Open (Float)	1800	1950	2000	mV
$t_{DGL(TTDM)}$	Deglitch exit TTDM between states			57		ms
	Deglitch enter TTDM between states			8		µs
$V_{TS\_I-FLDBK}$	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6uA) takes place near this spec threshold. V_{TS}: 1.425V → 1.525V		1475		mV

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

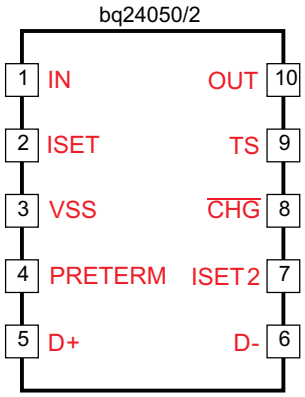
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{TS}	Optional Capacitance – ESD			0.22		µF
$V_{TS\text{-}0°C}$	bq24050/2/5 Low temperature CHG Pending	Low Temp Charging to Pending; V_{TS}: 1V → 1.5V	1205	1230	1255	mV
$V_{HYS\text{-}0°C}$	Hysteresis at 0°C	Charge pending to low temp charging; V_{TS}: 1.5V → 1V		86		mV
$V_{TS\text{-}10°C}$	Low temperature, half charge	Normal charging to low temp charging; V_{TS}: 0.5V → 1V	765	790	815	mV
$V_{HYS\text{-}10°C}$	Hysteresis at 10°C	Low temp charging to normal CHG; V_{TS}: 1V → 0.5V		35		mV
$V_{TS\text{-}45°C}$	High temperature at 4.1V	Normal charging to high temp CHG; V_{TS}: 0.5V → 0.2V	263	278	293	mV
$V_{HYS\text{-}45°C}$	Hysteresis at 45°C	High temp charging to normal CHG; V_{TS}: 0.2V → 0.5V		10.7		mV
$V_{TS\text{-}60°C}$	High temperature Disable	High temp charge to pending; V_{TS}: 0.2V → 0.1V	170	178	186	mV
$V_{HYS\text{-}60°C}$	Hysteresis at 60°C	Charge pending to high temp CHG; V_{TS}: 0.1V → 0.2V		11.5		mV
$t_{DGL(TS\_10C)}$	Deglitch for TS thresholds: 10C.	Normal to Cold Operation: V_{TS}: 0.6V → 1V		50		ms
		Cold to Normal Operation: V_{TS}: 1.0V → 0.6V		12		
$t_{DGL(TS)}$	Deglitch for TS thresholds: 0/45/60C.	Battery charging		30		ms
$V_{TS\text{-}EN\text{-}10k}$	Charge Enable Threshold, (10k NTC)	V_{TS}: 0V → 0.175V;	80	88	96	mV
$V_{TS\text{-}DIS\_HYS\text{-}10k}$	HYS below $V_{TS\text{-}EN\text{-}10k}$ to Disable, (10k NTC)	V_{TS}: 0.125V → 0V;		12		mV
$V_{TS\text{-}EN\text{-}100k}$	Charge Enable Threshold, (100k NTC)	V_{TS}: 0V → 0.175V	140	150	160	mV
$V_{TS\text{-}DIS\_HYS\text{-}100k}$	HYS below $V_{TS\text{-}EN\text{-}100k}$ to Disable, (100k NTC)	V_{TS}: 0.125V → 0V;		50		mV
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF\text{-}HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON ISET2						
V_{IL}	Logic LOW input voltage	Sink more than 8µA			0.4	V
V_{IH}	Logic HIGH input voltage	Source more than 8µA	1.4			V
I_{IL}	Sink current required for LO		2		9	µA
I_{IH}	Source current required for HI		1.1		8	µA
V_{FLT}	ISET2 Float Voltage		650	900	1200	mV

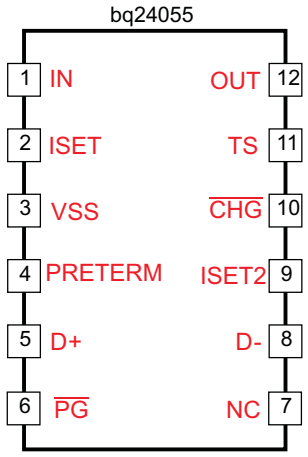
ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D+/D– DETECTION – bq24050/2/5						
t_{DPDM}	DetectionTime from start of D+/D- detection to latched output	t=0 at D– pulled-up > 0.5V or D+ pulled up externally, >0.8V		65		ms
V_{D+}	Bias at D+, during detection routine	Can source at least 200µA	0.475	0.6	0.7	V
I_{D+}	Current Limit at D+ pin, during detection routine	V_{D+} = 0V			1.5	mA
$I_{D–}$	Current Sink at D- pin, during detection routine	V_{D-}= 0.5V	50	100	150	µA
I_{D+_LEAK}	D+ leakage when not in detection mode	V_{D+} = 5V			1	µA
$I_{D–\_LEAK}$	D– leakage when not in detection mode	V_{D-}= 5V			1	µA
$V_{DPDM\_0.4V}$	D– Comparator Threshold Rising		0.35		0.45	V
$V_{DPDM\_HYS\_0.4V}$	D– Comparator Hysteresis			42		mV
$V_{DPDM\_0.8V}$	D+/D– Comparator Threshold Rising		0.75		0.875	V
$V_{DPDM\_HYS\_0.8V}$	D+/D– Comparator Hysteresis			42		mV
LOGIC LEVELS ON $\overline{CHG}$ AND $\overline{PG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5mA			0.4	V
I_{lkg}	Leakage current into IC	$V_{\overline{CHG}}$ = 5V, $V_{\overline{PG}}$ = 5V			1	µA

PIN CONFIGURATION





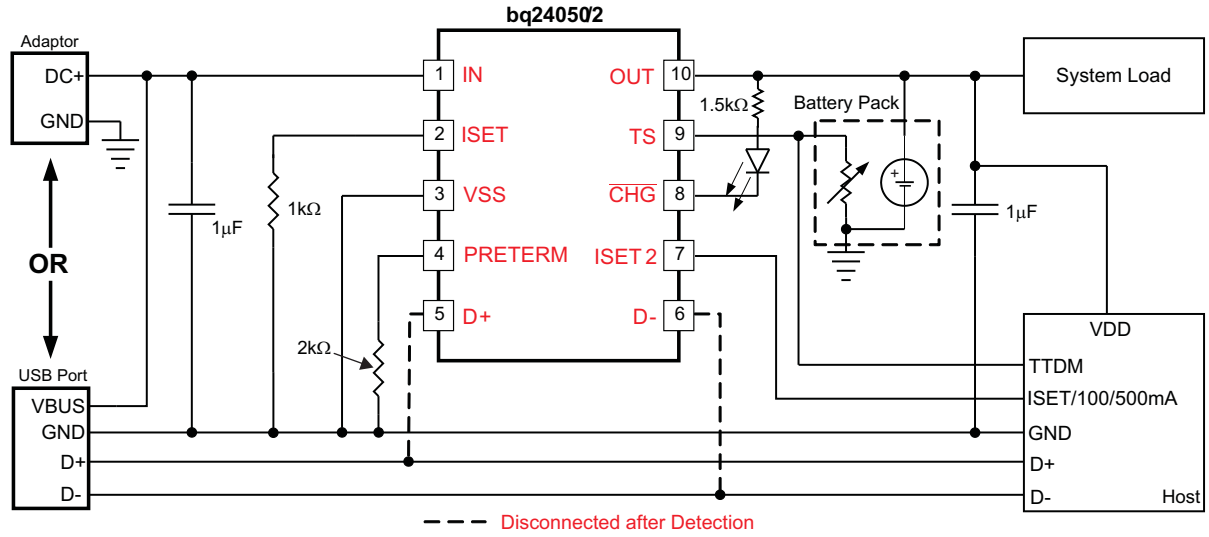
PIN FUNCTIONS

NAME	bq24050/2	bq24055	I/O	DESCRIPTION
IN	1	1	I	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1µF to 10µF, connect from IN to V_{SS}.
OUT	10	12	O	Battery Connection. System Load may be connected. Average load should not be excessive, allowing battery to charge within the 10 hour safety timer window. Expected range of bypass capacitors 1µF to 10µF.
PRE-TERM	4	4	I	Programs the Current Termination Threshold (5 to 50% of Iout which is set by ISET) and Sets the Pre-Charge Current to twice the Termination Current Level. Expected range of programming resistor is 1k to 10kΩ (2k: I_{OUT}/10 for term; I_{OUT}/5 for precharge)
ISET	2	2	I	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is 10.8k (50mA) to 675 Ω (800mA).
ISET2	7	9	I	Programming the Input/Output Current Limit for the USB or Adaptor source: High = 500mAmax, Low = ISET, FLOAT = 100mA max. D+D– Detection initially sets the charge threshold and requires ISET2 to change states to take control.
TS	9 (1)	11	I	Temperature sense pin connected to '50/55 –10k at 25C NTC thermistor, '52 – 100k NTC at 25°C, in the battery pack. Floating TS Pin or pulling High puts part in TTDM and disable TS monitoring, Timers and Termination. Pulling pin Low disables the IC (CE function). If NTC sensing is not needed, connect this pin to VSS through an external '50/55-10kΩ /'52-100kΩ resistor. A '50/55-250kΩ/'52-880kΩ from TS to ground will prevent IC entering TTDM when battery with thermistor is removed.
VSS	3	3	–	Ground terminal
$\overline{CHG}$	8	10	O	Low (FET on) indicates charging and Open Drain (FET off) indicates no Charging or Charge complete.
$\overline{PG}$	–	6	O	Low (FET on) indicates the input voltage is above UVLO and the OUT (battery) voltage and less than V_{OVP}
D+	5	5	I	USB port D+ input connection
D–	6	8	I	USB port D– input connection
NC	–	7	NA	Do not make connection to this pin (internal use) – Do not route through this pin
Thermal PAD and Package	Pad 2x2mm^2	Pad 2x3mm^2	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

(1) Spins have different pin definitions

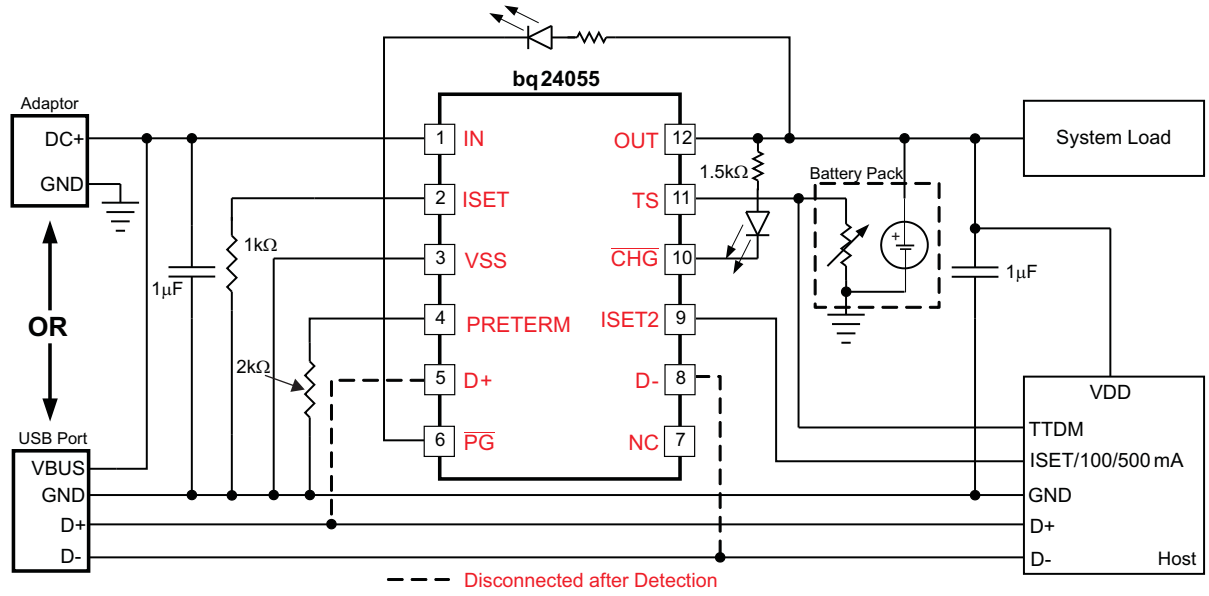
Typical Application Circuit: bq24050/2

$I_{OUT\_FAST\_CHG}$ = 540mA; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA

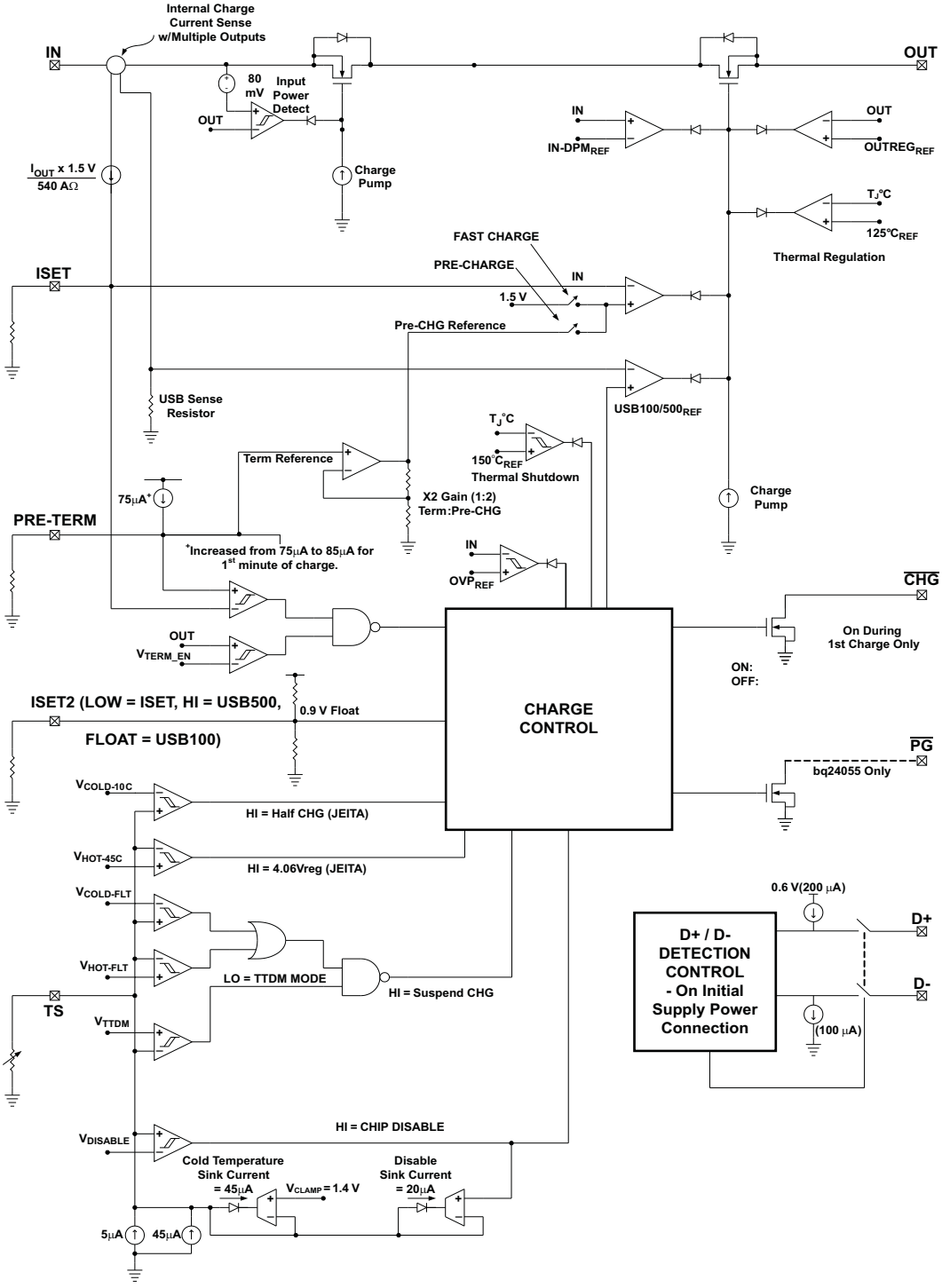


Typical Application Circuit: bq24055

$I_{OUT\_FAST\_CHG}$ = 540mA; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA



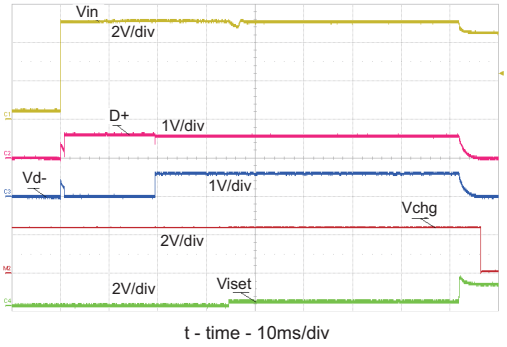
FUNCTIONAL BLOCK DIAGRAM



TYPICAL OPERATIONAL CHARACTERISTICS

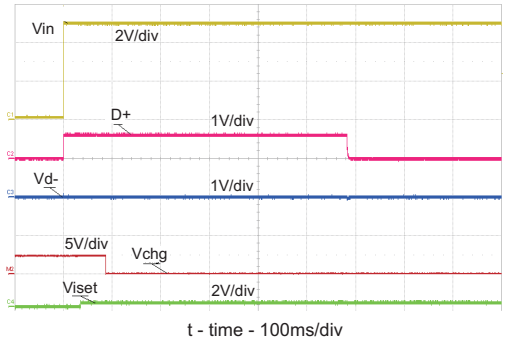
SETUP: bq24055 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)
R_{ISET} = 1k; $I_{OUT\_FAST\_CHG}$ = 540mA; R_{PAC_TERM} = 2k; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA

Power UP, DOWN, OVP, Disable and Enable Waveforms



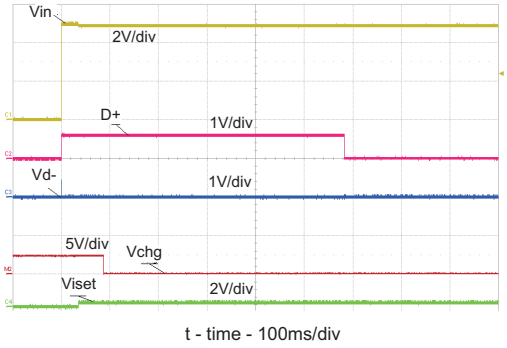
Detected D- line pulled to 0.6V and the detection routine is started.

Figure 1. D+ D- Detection for Adaptor Hot Plug



No signal detected on D+ or D-. After 500ms, the detection routine is forced to run.

Figure 2. D+ D- Detection for Unknown Source Hot Plug



(Device transceiver is "dead") After 500ms, the detection routine is forced to run.

Figure 3. D+ D- Detection for USB Hot Plug no Pullup

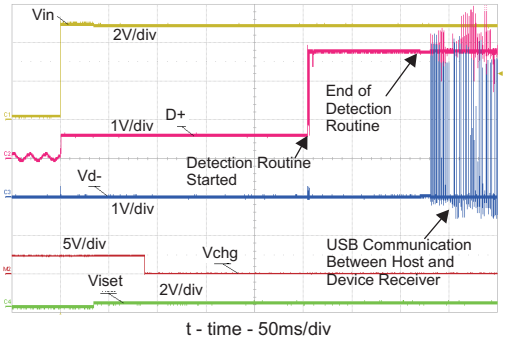


Figure 4. D+ D- Detection for USB Hot Plug with Pullup

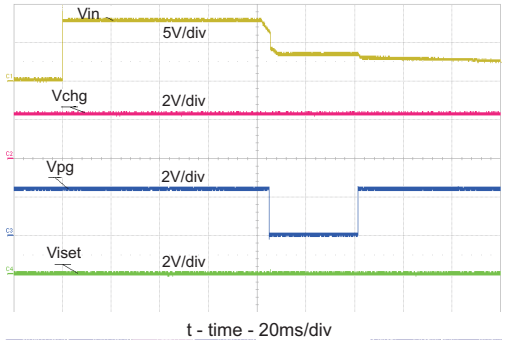


Figure 5. OVP 8V Adaptor – Hot Plug

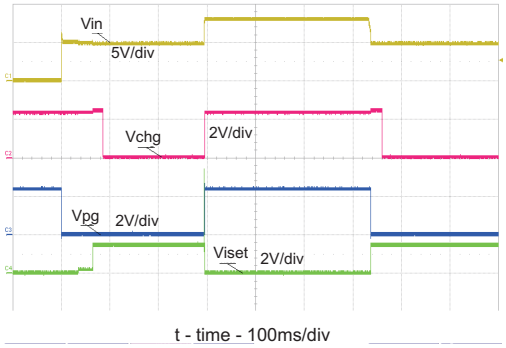
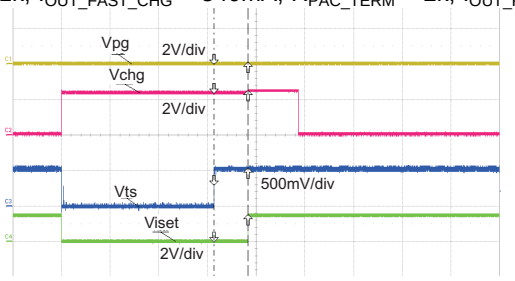


Figure 6. OVP from Normal Operation – V_{IN} = 0V→5V→8V→5V

TYPICAL OPERATIONAL CHARACTERISTICS (continued)

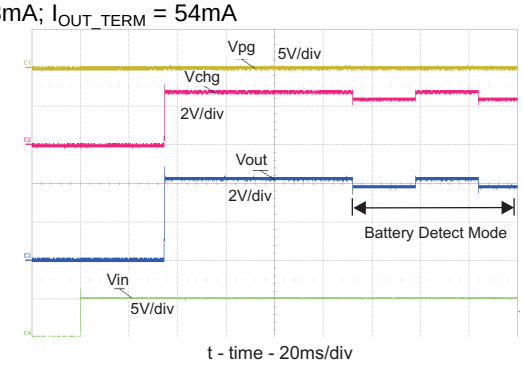
SETUP: bq24055 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)

R_{ISET} = 1k; $I_{OUT\_FAST\_CHG}$ = 540mA; R_{PAC_TERM} = 2k; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA



10kΩ resistor from TS to GND. 10kΩ is shorted to disable the IC.

Figure 7. TS Enable and Disable



Fixed 10kΩ resistor, between TS and GND.

Figure 8. Hot Plug Source w/No Battery – Battery Detection

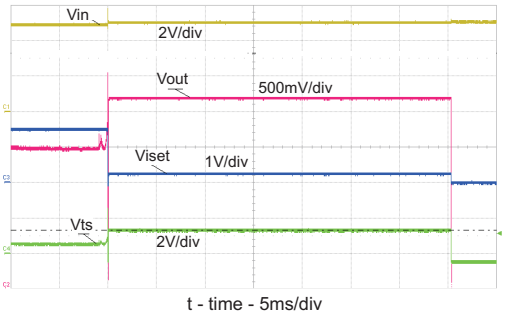


Figure 9. Battery Removal – GND Removed 1st, 42-Ω Load

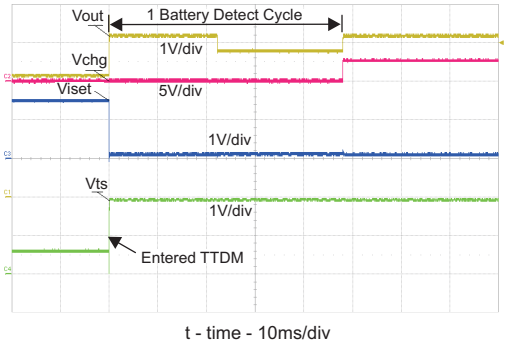
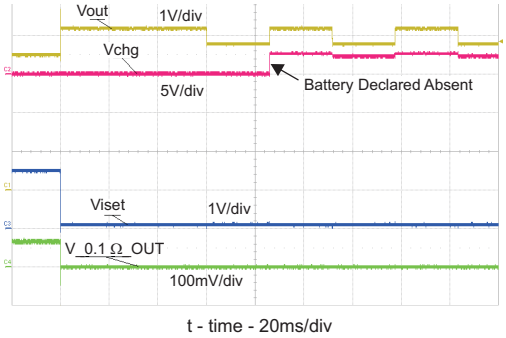


Figure 10. Battery Removal with OUT and TS Disconnect 1st, With 100–Ω Load



Continuous battery detection when not in TTDM.

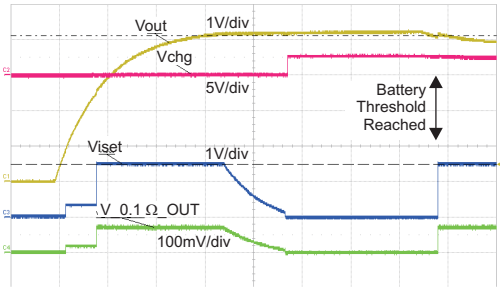
Figure 11. Battery Removal With Fixed TS = 0.5V

TYPICAL OPERATIONAL CHARACTERISTICS (continued)

SETUP: bq24055 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)

R_{ISET} = 1k; $I_{OUT\_FAST\_CHG}$ = 540mA; R_{PAC_TERM} = 2k; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA

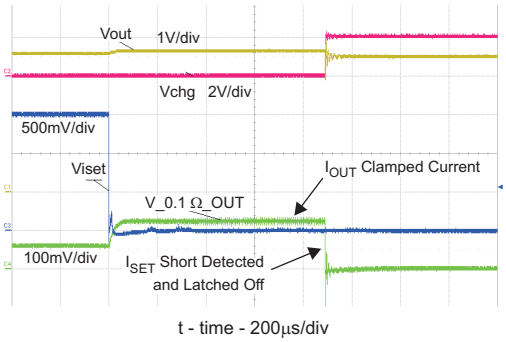
PROTECTION CIRCUITS WAVEFORMS



CH4: Iout (1A/Div)

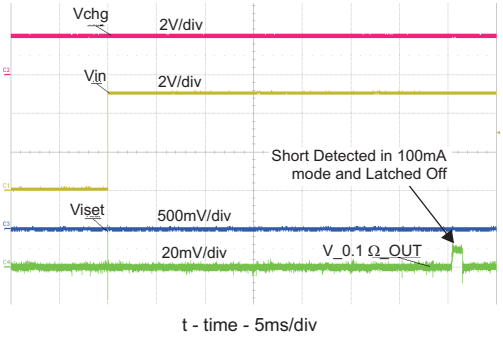
Battery voltage swept from 0V to 4.25V to 3.9V.

Figure 12. Battery Charge Profile



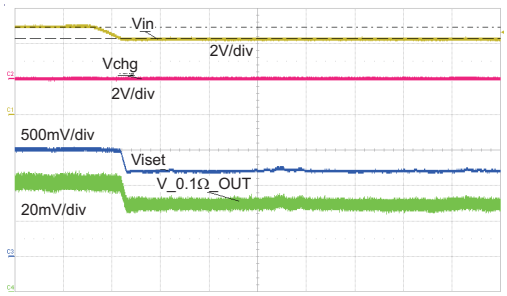
CH4: Iout (1A/Div)

Figure 13. ISET Shorted During Normal Operation



CH4: Iout (0.2A/Div)

Figure 14. ISET Shorted Prior to USB Power Up



CH4: Iout (0.2A/Div)

Figure 15. DPM – Adaptor Current Limits – V_{IN} Regulated to 4.3V

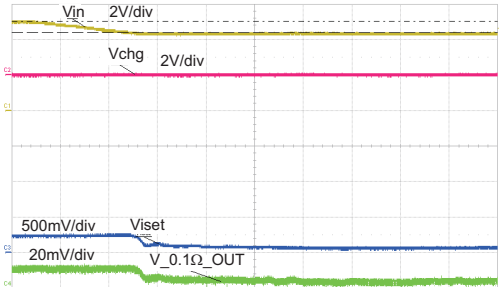
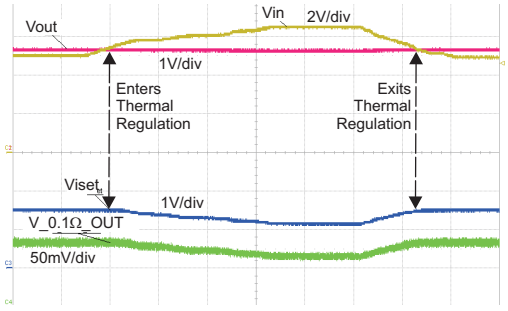


Figure 16. DPM – USB Current Limits – V_{IN} Regulated to 4.4V



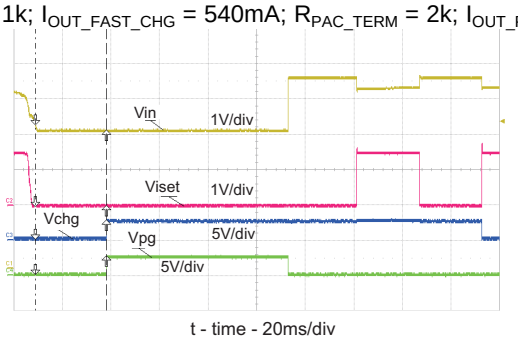
The IC temperature rises to 125°C and enters thermal regulation. Charge current is reduced to regulate the IC at 125°C. VIN is reduced, the IC temperature drops, the charge current returns to the programmed value.

Figure 17. Thermal Reg. – V_{IN} Increases

TYPICAL OPERATIONAL CHARACTERISTICS (continued)

SETUP: bq24055 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)

R_{ISET} = 1k; $I_{OUT\_FAST\_CHG}$ = 540mA; R_{PAC_TERM} = 2k; $I_{OUT\_PRE\_CHG}$ = 108mA; I_{OUT_TERM} = 54mA



Vin swept from 5V to 3.9V to 5V, Vbat = 4V

Figure 18. Entering and Exiting Sleep Mode

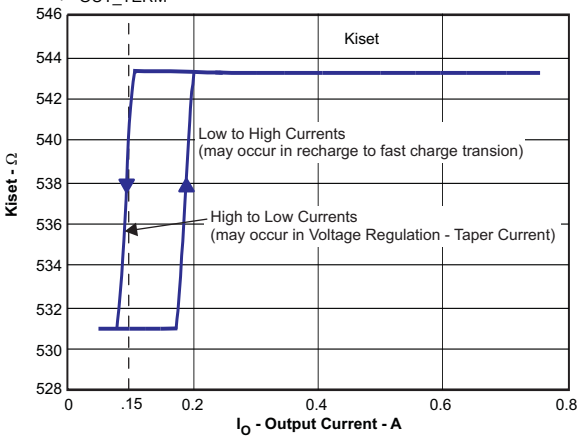


Figure 19. Kiset for Low and High Currents

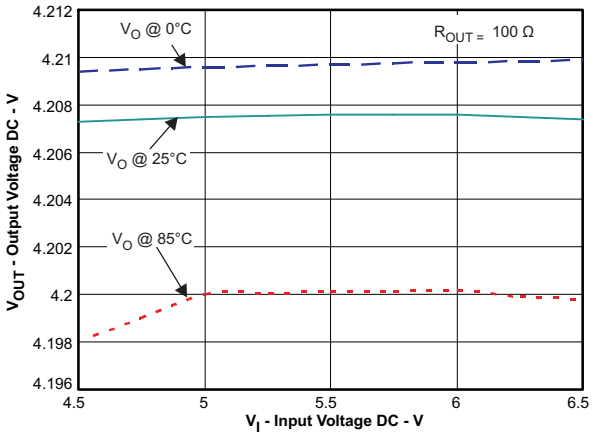


Figure 20. Line Regulation

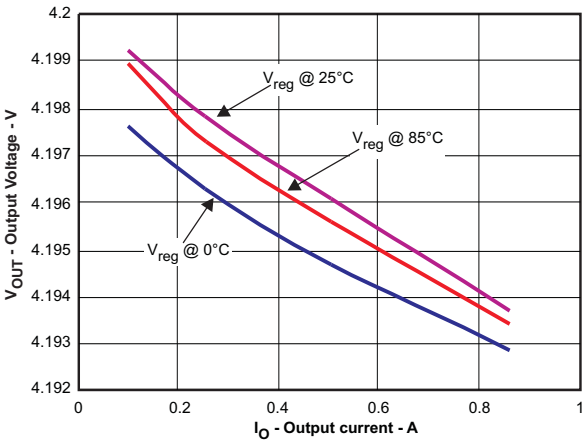


Figure 21. Load Regulation Over Temperature

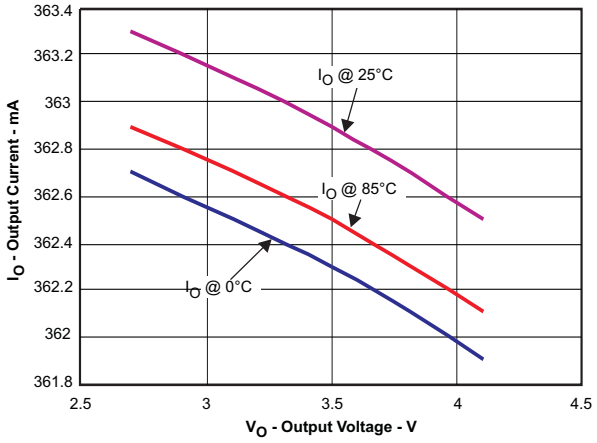


Figure 22. Current Regulation Overtemperature

FUNCTIONAL GENERAL DESCRIPTION

The bq2405x is a highly integrate family of 2×2 or 2×3mm single cell Li-Ion and Li-Pol chargers. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: Pre-charge to recover a fully discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current, pre-charge current and termination. This charger is designed to work with a USB connection or Adaptor (DC out). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: JEITA Temperature Standard, Overvoltage Protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5VDC power source the D+, D– detection routine is run to determine if the source is an Adaptor or a USB port. This feature is useful, when the battery is discharged (USB transceiver dead) or there is no transceiver, by early detection of an adaptor, thus allowing initial charging at the adaptor level. ISET and OUT short checks are performed in parallel with the detection routine to assure a proper charge cycle.

If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of precharge current can be programmed using the PRE-TERM pin which programs a percent of fast charge current (10 to 100%) as the precharge current. This feature is useful when the system load is connected across the battery “stealing” the battery current. The precharge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. The PRE-TERM pin is a dual function pin which sets the precharge current level and the termination threshold level. The termination "current threshold" is always half of the precharge programmed current level.

Once the battery voltage has charged to the V_{LOWV} threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET pin. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C the IC enters thermal regulation, slow the timer clock by half and reduce the charge current as needed to keep the temperature from rising any further. Figure 23 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC’s junction temperature is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The charge termination can be disabled if desired. The $\overline{CHG}$ pin is low (LED on) during the first charge cycle only and turns off once the charge termination threshold is reached, regardless if termination is enabled or disabled.

The TS pin monitors the voltage across the pack thermistor and implements the JEITA standard. This allows for reduced voltage regulation at hot temperatures and reduced charge currents at low temperatures. The TS pin incorporates a chip disable feature when pulled low and an Termination and Timer Disable Mode (TTDM) feature when left floating or pulled high.

Further details are mentioned in the Operating Modes section.

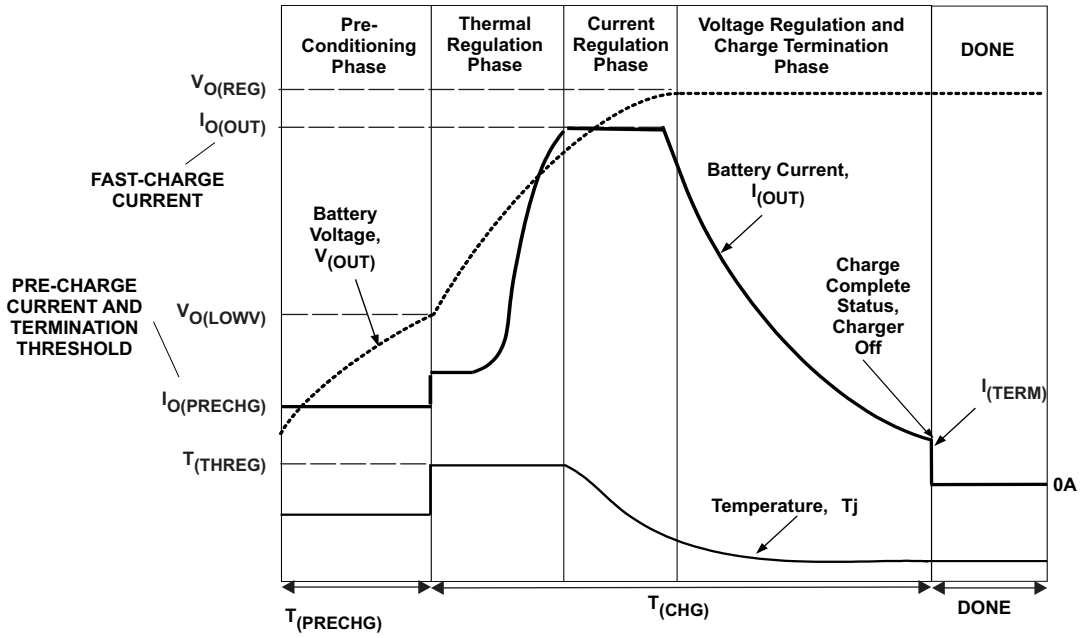


Figure 23. Charging Profile with Thermal Regulation

DETAILED FUNCTIONAL DESCRIPTION

Power-Down, or Undervoltage Lockout (UVLO):

The bq2405x family is in power down mode if the IN pin voltage is less than UVLO. The part is considered "dead" and all the pins are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active mode depending on the OUT pin (battery) voltage.

Power-up

The IC is alive after the IN voltage ramps above UVLO (see sleep mode), resets all logic and timers, and starts to perform the D+D– detection along with many of the continuous monitoring routines. The D+/D– detection typically take less than 100ms, but can take as long as 600ms if there is no activity on the D+ or D– lines which indicates the device transceiver nor an adaptor is present. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 100mA, finishes the USB detection routine, sets the input current limit threshold base on the source detected (ISET=adaptor or 100mA=USB), starts the safety timer and enables the $\overline{\text{CHG}}$ pin. See Figure 25

D+, D– Detection:

This detection is designed to give the charger advance notice that an adaptor or USB port is connect for the cases where the battery is discharged and device transceiver is not able to communicate with a USB host or there is not a device transceiver. If an adaptor is detected, then the charger can immediately start charging at the programmed ISET level. Without this early detection, the charger would have to default to the 100mA input current level to make sure it was not over-loading a low power USB port. The detection method monitors the D+, D– communication lines looking for a short between the lines (Adaptor source connected) or pull down resistors on D+, D– (USB source connected) to determine what source is connected (no USB communication takes place). If an adaptor source is detected then the charger will transition from the 100mA startup level to the ISET programmed current level. If a USB port is detected, the input current limit will stay at the 100mA level. If a different charge level is desired, than the one detected, the host has to change the state of the ISET2 pin (signals the internal logic to start using the ISET2 as the program pin) and then set to the desired state.

The D+ and D– pin connections inside the charger are disconnected within 100ms of the D+ or D– lines being pulled high (start of detection), to minimize any interaction between the charger detection pins and the USB normal communications. If the device transceiver is able to communicate with the USB host, communication typically starts after 100ms after the device has pulled the D+ or D– line high indicating it is “on line”, and by then the IC detection is complete and has been disconnected. The device host then may change the ISET2 level or disable the IC by pulling the TS pin low.

Sleep Mode

If the IN pin voltage is between than $V_{OUT}+V_{DT}$ and UVLO, the charge current is disabled, the safety timer counting stops (not reset) and the $\overline{PG}$ and $\overline{CHG}$ pins are high impedance. As the input voltage rises and the charger exits sleep mode, the $\overline{PG}$ pin goes low, the safety timer continues to count, charge is enabled and the $\overline{CHG}$ pin returns to its previous state. See Figure 18

New Charge Cycle

A new charge cycle is started when a good power source is applied, performing a chip disable/enable (TS pin), exiting Termination and Timer Disable Mode (TTDM), detecting a battery insertion or the OUT voltage dropping below the VRCH threshold. The $\overline{CHG}$ pin is active low only during the first charge cycle, therefore exiting TTDM or a dropping below VRCH will not turn on the $\overline{CHG}$ pin FET, if the $\overline{CHG}$ pin is already high impedance.

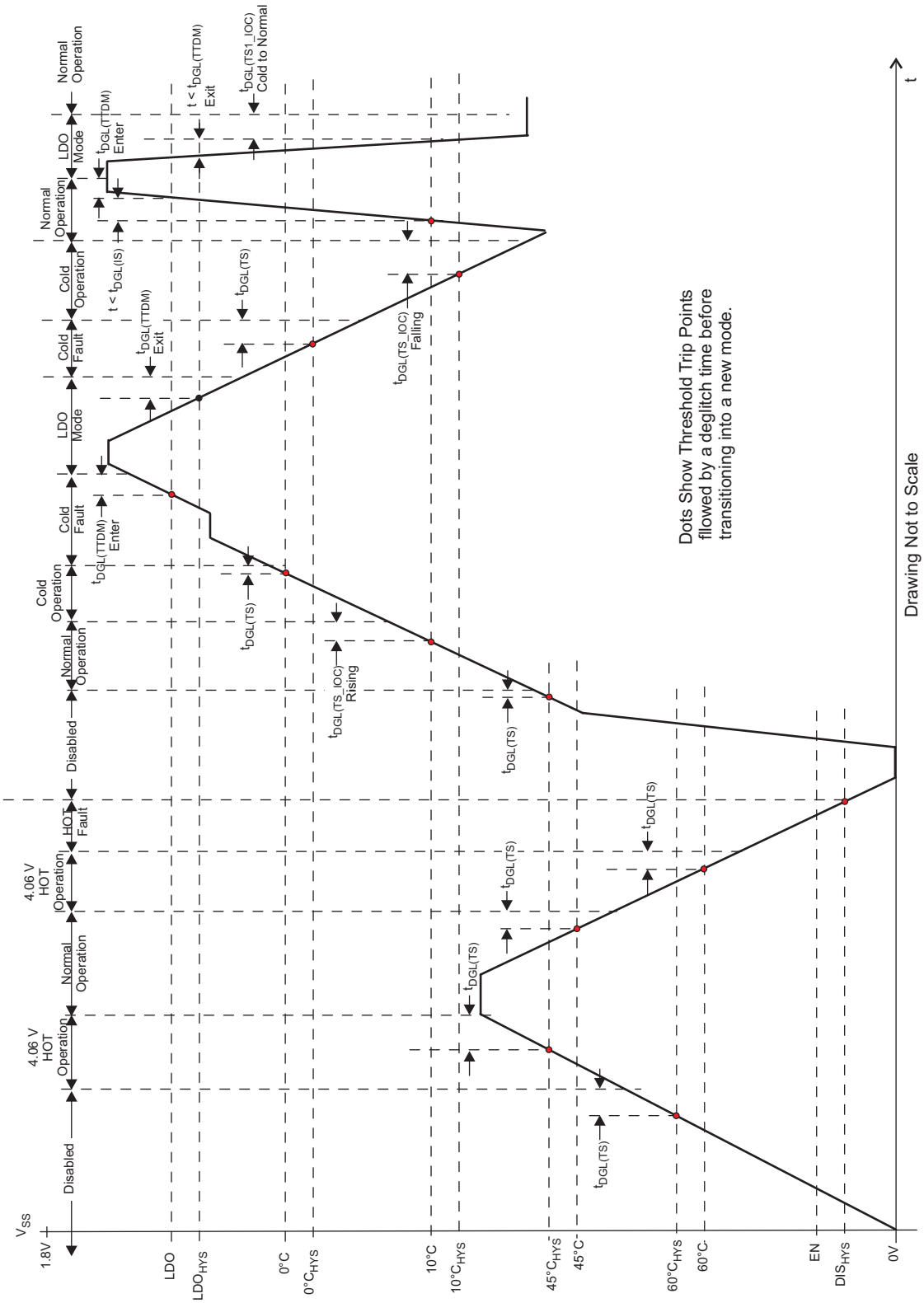


Figure 24. TS Battery Temperature Bias Threshold and Deglitch Timers

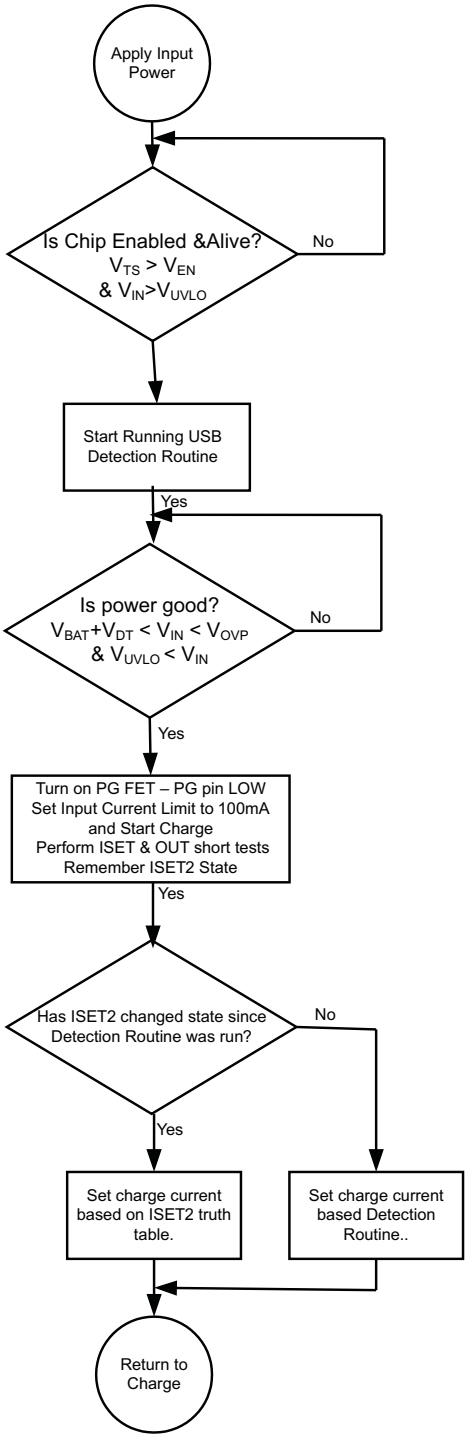


Figure 25. Power-up Flow Diagram

Overvoltage-Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the $\overline{CHG}$ and $\overline{PG}$ pin goes to a high impedance state. Once the overvoltage returns to a normal voltage, the $\overline{PG}$ pin goes low, timer continues, charge continues and the $\overline{CHG}$ pin goes low after a 25ms deglitch.. $\overline{PG}$ pin is optional on some packages.

Power Good Indication ($\overline{PG}$)

After application of a 5V source, the input voltage rises above the UVLO and sleep thresholds (V_{IN}> V_{OUT}+V_{DT}), but is less than OVP (V_{IN}< V_{OVP}), then the $\overline{PG}$ FET turns on and provides a low impedance path to ground. SEE Figure 5, Figure 6, and Figure 18.

CHG Pin Indication

The charge pin has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor.

The charge pin will be high impedance in sleep mode and OVP (if $\overline{PG}$ is high impedance) and return to its previous state once the condition is removed.

Cycling input power, pulling the TS pin low and releasing or entering pre-charge mode will cause the $\overline{CHG}$ pin to reset and is considered the start of a first charge.

$\overline{CHG}$ and $\overline{PG}$ LED Pull-up Source

For host monitoring, a pull-up resistor is used between the "STATUS" pin and the V_{CC} of the host and for a visual indication a resistor in series with an LED is connected between the "STATUS" pin and a power source. If the $\overline{CHG}$ or $\overline{PG}$ source is capable of exceeding 7V, a 6.2V zener should be used to clamp the voltage. If the source is the OUT pin, note that as the battery changes voltage, the brightness of the LEDs vary.

Charging State	$\overline{CHG}$ FET/LED
1st Charge	ON
Refresh Charge	OFF
OVP	
SLEEP	
TEMP FAULT	ON for 1st Charge

V_{IN} Power Good State	$\overline{PG}$ FET/LED
UVLO	OFF
SLEEP Mode	
OVP Mode	
Normal Input (V_{OUT} + V_{DT} < V_{IN} < V_{OUP})	ON
PG is independent of chip disable (bq24055, V_{TS} = 0V)	

Input DPM Mode (V_{IN}-DPM or IN-DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to an excessive load. When the input voltage drops to the V_{IN-DPM} threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than V_{IN-DPM} to power the out pin. This works well with current limited adaptors and USB ports as long as the nominal voltage is above 4.3V and 4.4V respectively. This is an added safety feature that helps protect the source from excessive loads.

OUT

The Charger's OUT pin provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT pin is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

ISET

An external resistor is used to Program the Output Current (50 to 800mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} \div I_{OUT} \quad (0)$$

Where:

I_{OUT} is the desired fast charge current;
K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. Figure 19 shows the transition from low current to higher current. Going from higher currents to low currents, there is hysteresis and the transition occurs around 0.15A.

The ISET resistor is short protected and will detect a resistance lower than ≠340Ω. The detection requires at least 80mA of output current. If a “short” is detected, then the IC will latch off and can only be reset by cycling the power. The OUT current is internally clamped to a maximum current between 1.1A and 1.35A and is independent of the ISET short detection circuitry, as shown in Figure 27. Also, see Figure 13 and Figure 14.

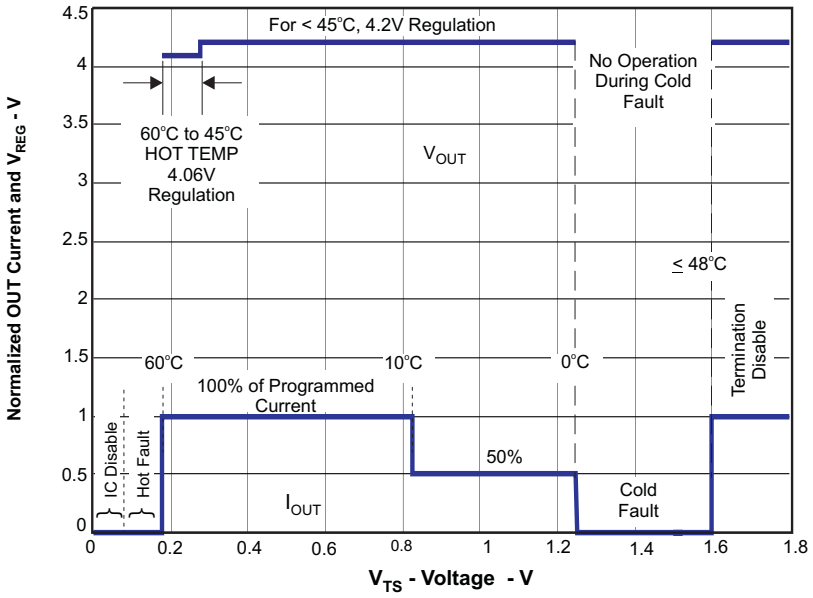


Figure 26. OPERATION OVER TS BIAS VOLTAGE

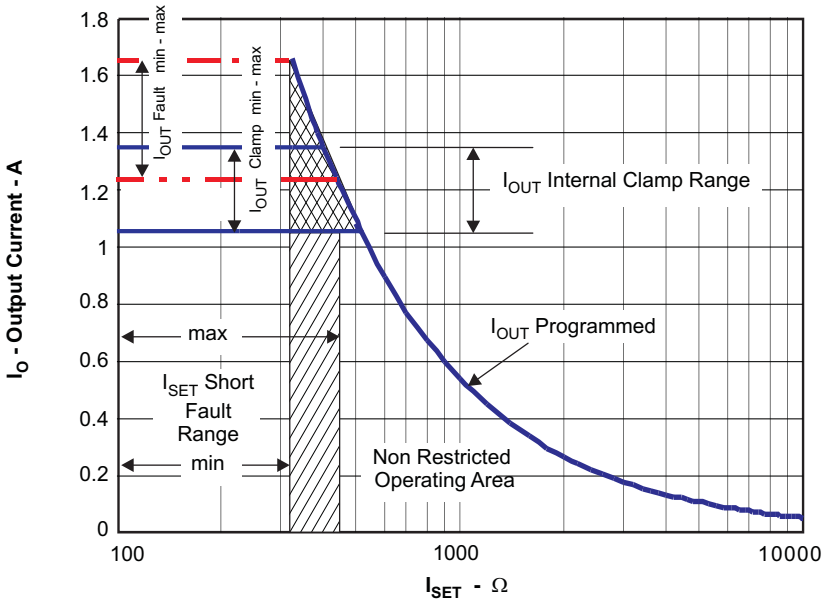


Figure 27. PROGRAMMED / CLAMPED OUT CURRENT

PRE_TERM – Pre-Charge and Termination Programmable Threshold

Pre-Term is used to program both the pre-charge current and the termination current threshold, on the bq24050/2/5. The pre-charge current level is a factor of two higher than the termination current level. The termination can be set between 5 and 50% of the programmed output current level set by ISET. If left floating the termination and pre-charge are set internally at 10/20% respectively. The pre-charge-to-fast-charge, V_{lowv} threshold is set to 2.5V.

$$R_{PRE\text{-}TERM} = \%Term \times K_{TERM} = \%Pre\text{-}CHG \times K_{PRE\text{-}CHG} \quad (0)$$

Where:

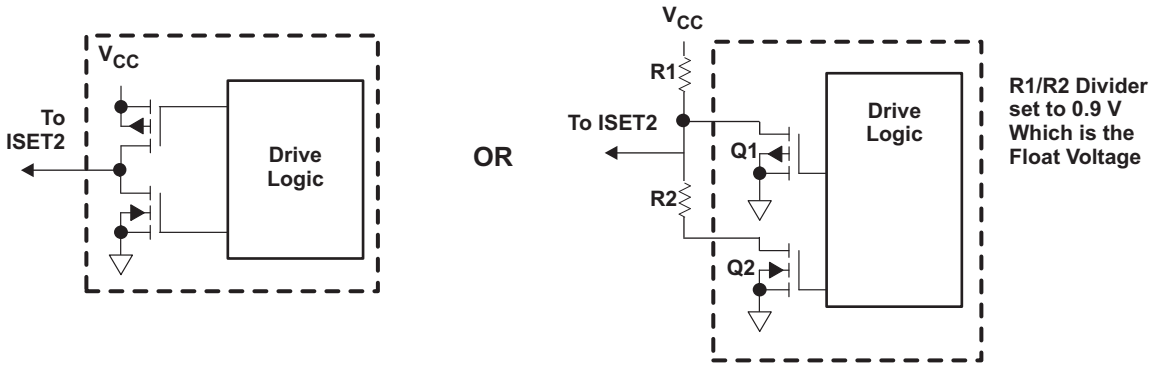
%Term is the percent of fast charge current where termination occurs;
%Pre-CHG is the percent of fast charge current that is desired during precharge;
K_{TERM} and KPRE-CHG are gain factors found in the electrical specifications.

ISET2

Is a 3-state input and programs the Input Current Limit/Regulation Threshold. A low will program a regulated fast charge current via the ISET resistor and is the maximum allowed input/output current for any ISET2 setting, Float will program a 100mA Current limit and High will program a 500mA Current limit. Note that initially the D+/D– detection will latch the charge mode according to the source detected (dedicated charger: ISET; USB Host: at 100mA) until the ISET2 pin has changed states, indicating the processor or transceiver is controlling the pin.

The detection routine registers the input level (Low–High-Z–High) of the ISET2 pin ~532 µs after applying input power (V_{IN} > 3.4 V – UVLO). After the detection routine is complete, which is ~100 ms after a pull-up on the D+ or D– line or after ~570 ms if no pull-up, the IC monitors the ISET2 pin for a change of state. If the state changes (Low–High-Z–High) from the one registered, for more than 5 µs, then the "detected" latched charge mode is released and is then controlled by the ISET2 pin. The completion of the detection routine varies due to the mechanical-plugging action of the USB cable; therefore, it is best to wait ≥ 600 ms after V_{IN} > 3.4 V to take control of the ISET2 pin.

The following illustration shows two configurations for driving the 3-state ISET2 pin:



TS

The TS pin is designed to follow the new JEITA temperature standard for Li-Ion and Li-Pol batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is cut in half and if between 45°C and 60°C the regulation voltage is reduced to 4.1Vmax, see Figure 26. The TS feature is implemented using an internal 50µA current source to bias the thermistor (bq24050/5 designed for use with a 10k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F), and bq24052 with a 100k NTC β = 3540 (Mitsubishi TH05-36104F) or equivalent) connected from the TS pin to V_{SS}. If this feature is not needed, a fixed 10k can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS pin low to disable charge.

The TS pin has two additional features, when the TS pin is pulled low or floated/driven high. A low disables charge (similar to a CE feature) and a high puts the charger in TTDM.

Above 60°C or below 0°C the charge is disable. Once the thermistor reaches ≠–10°C the TS current folds back to keep a cold thermistor (between –10°C and –50°C) from placing the IC in the TTDM mode. If the TS pin is pulled low into disable mode, the current is reduce to ≠30µA, see Figure 24. Since the I_{TS} current is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10k and 100k.

Termination and Timer Disable Mode (TTDM) -TS pin high

The battery charger is in TTDM when the TS pin goes high from removing the thermistor (removing battery pack/floating the TS pin) or by pulling the TS pin up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. If the battery was removed then the $\overline{CHG}$ pin will go to its high impedance state if not already there. If a battery is detected the $\overline{CHG}$ pin does not change states until the current tapers to the termination threshold, where the $\overline{CHG}$ pin goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has pre-charge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the $\overline{CHG}$ LED turns on.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237k resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS pin into TTDM. This creates ≠0.1°C error at hot and a ≠3°C error at cold.

Timers

The pre-charge timer is set to 30 minutes . The pre-charge current, can be programmed to off-set any system load, making sure that the 30 minutes is adequate.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation, IN-DPM or if in USB current limit. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and the $\overline{CHG}$ pin goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power or going into and out of TTDM.

Termination

Once the OUT pin goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold, the $\overline{CHG}$ pin goes high impedance and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present the charge current will terminate. If the battery was removed along with the thermistor, then the TS pin will be driven high and the charge will enter TTDM. If the battery was removed and the TS pin is held in the active region, then the battery detect routine will continue until a battery is inserted.

Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT pin at a useable voltage. Whenever the battery is missing the $\overline{CHG}$ pin should be high impedance.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power-up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine will be disabled while the IC is in TTDM or has a TS fault. See Figure 28 for the Battery Detect Flow Diagram.

Refresh Threshold

After termination, if the OUT pin voltage drops to VRCH (100mV below regulation) then a new charge is initiated, but the $\overline{CHG}$ pin remains at a high impedance (off).

Starting a Charge on a Full Battery

The termination threshold is raised by ≠14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.

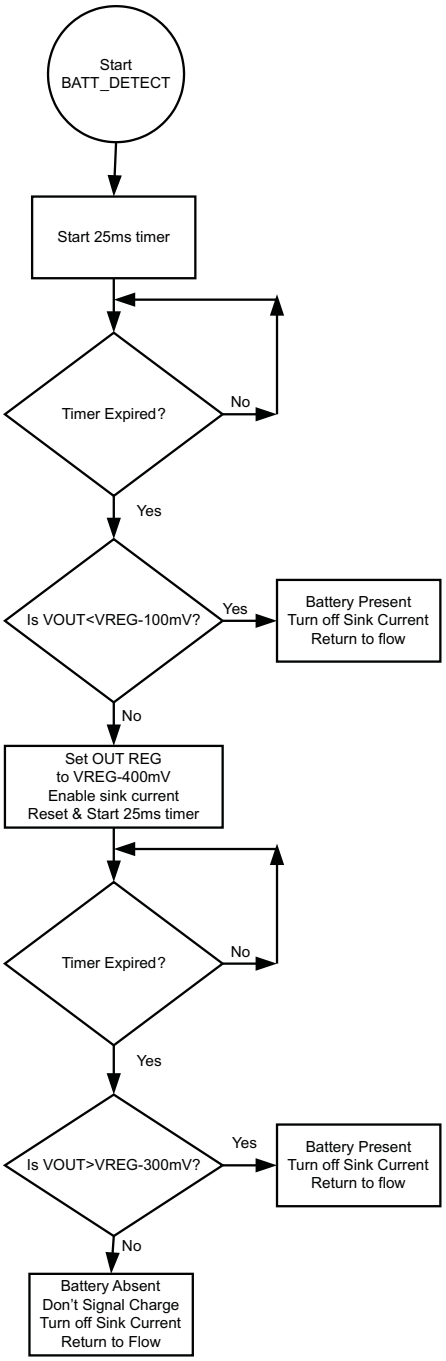
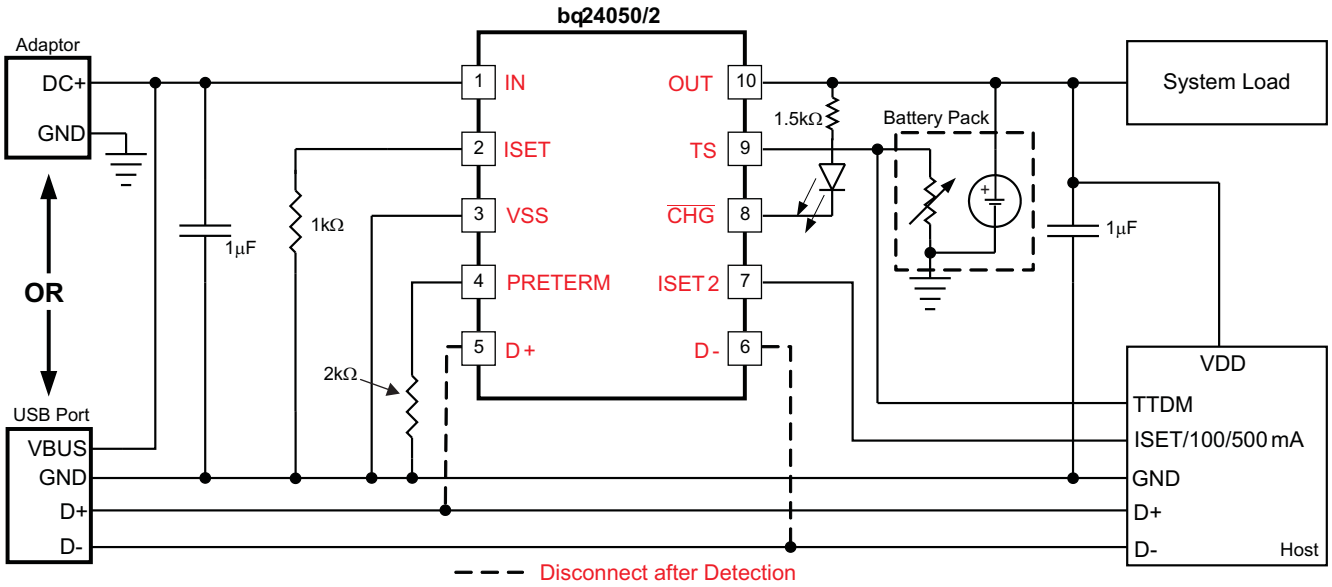


Figure 28. Battery Detect Flow Diagram

bq2405x CHARGER APPLICATION DESIGN EXAMPLE



Requirements

- Supply voltage = 5 V
- Fast charge current: I_{OUT-FC} = 540 mA; ISET-pin 2
- Termination Current Threshold: $\%_{IOUT-FC}$ = 10% of Fast Charge or ≠54mA
- Pre-Charge Current by default is twice the termination Current or ≠108mA
- TS – Battery Temperature Sense = 10k NTC (103AT)

Calculations

Program the Fast Charge Current, ISET:

$R_{ISET} = [K_{(ISET)} / I_{(OUT)}]$
from electrical characteristics table. . . $K_{(SET)}$ = 540AΩ
R_{ISET} = [540AΩ/0.54A] = 1.0 kΩ
Selecting the closest standard value, use a 1kΩ resistor between ISET (pin 16) and V_{SS}.

Program the Termination Current Threshold, ITERM:

$R_{PRE-TERM} = K_{(TERM)} \times \%_{IOUT-FC}$
$R_{PRE-TERM}$ = 200Ω/% × 10% = 2kΩ
Selecting the closest standard value, use a 2kΩ resistor between ITERM (pin 15) and Vss.
One can arrive at the same value by using 20% for a pre-charge value (factor of 2 difference).
$R_{PRE-TERM} = K_{(PRE-CHG)} \times \%_{IOUT-FC}$
$R_{PRE-TERM}$ = 100Ω/% × 20%= 2kΩ

TS Function

Use a 10k NTC thermistor in the battery pack (103AT).

To Disable the temp sense function, use a fixed 10k resistor between the TS (Pin 1) and V_{SS}.

$\overline{CHG}$ and $\overline{PG}$

LED Status: connect a 1.5k resistor in series with a LED between the OUT pin and the $\overline{CHG}$ pin. Connect a 1.5k resistor in series with a LED between the OUT pin and the and $\overline{PG}$ pin.

Processor Monitoring: Connect a pull-up resistor between the processor's power rail and the $\overline{CHG}$ pin. Connect a pull-up resistor between the processor's power rail and the $\overline{PG}$ pin.

SELECTING IN AND OUT PIN CAPACITORS

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input and output pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30V transient (verify tested rating with capacitor manufacturer).

THERMAL PACKAGE

The bq2405x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the VSS pin. Full PCB design guidelines for this package are provided in the *QFN/SON PCB Attachment Application Note* application note (SLUA271). The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = (T_J - T) / P \quad (0)$$

Where:

T_J = chip junction temperature
T = ambient temperature
P = device power dissipation

Factors that can influence the measurement and calculation of θ_{JA} include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion and Li-Pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} - V_{(OUT)}] \times I_{(OUT)} \quad (0)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery discharges, the battery is used for the calculation. The time from full to discharge can be calculated by dividing the Amp-Hour Capacity of the battery by the leakage current. For a 0.75AHr battery and a 10µA leakage current (750mAHr/0.010mA = 75000 Hours), it would take 75k hours or 8.8 years to discharge. In reality, the self discharge of the cell is much faster, so the 10µA leakage would be considered negligible.

Layout Tips

To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq2405x, with short trace runs to both IN, OUT and GND (thermal pad).

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The bq2405x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. It is best to use multiple 10-mill vias in the power pad of the IC and in close proximity to conduct the heat to the bottom ground plane. The bottom ground place should avoid traces that “cut off” the thermal path. The thinner the PCB the less temperature rise. The EVM PCB has a thickness of 0.031 inches and uses 2 oz. (2.8-mill thick) copper on top and bottom, and is a good example of optimal thermal performance.

REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
• Changed the status of the devices From: Product Preview To: Production Data	1

Changes from Revision A (September 2009) to Revision B	Page
• Changed all occurrences of Li-Ion To: Li-Ion and Li-Pol	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24050DSQR	ACTIVE	SON	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		CVC	Samples
BQ24050DSQT	ACTIVE	SON	DSQ	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		CVC	Samples
BQ24052DSQR	ACTIVE	SON	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		CGT	Samples
BQ24052DSQT	ACTIVE	SON	DSQ	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		CGT	Samples
BQ24055DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		CGU	Samples
BQ24055DSST	ACTIVE	WSON	DSS	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		CGU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

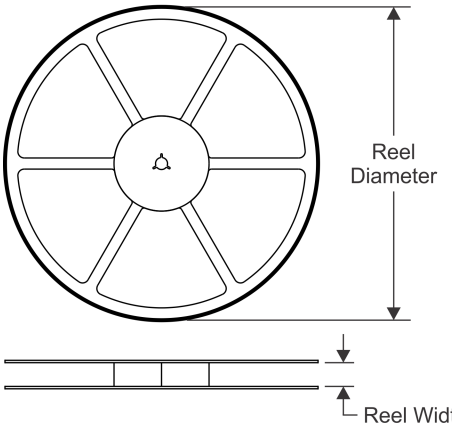
(4) Only one of markings shown within the brackets will appear on the physical device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

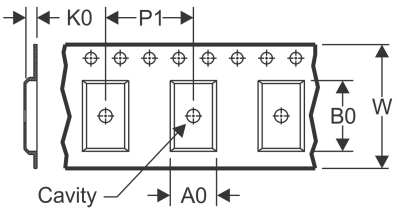
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

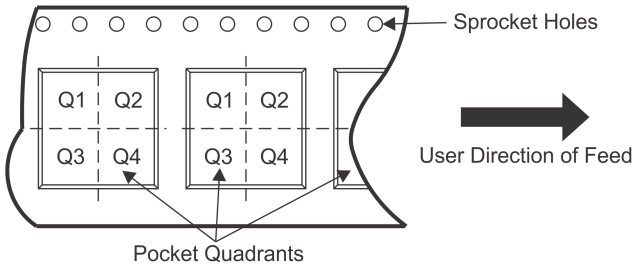


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

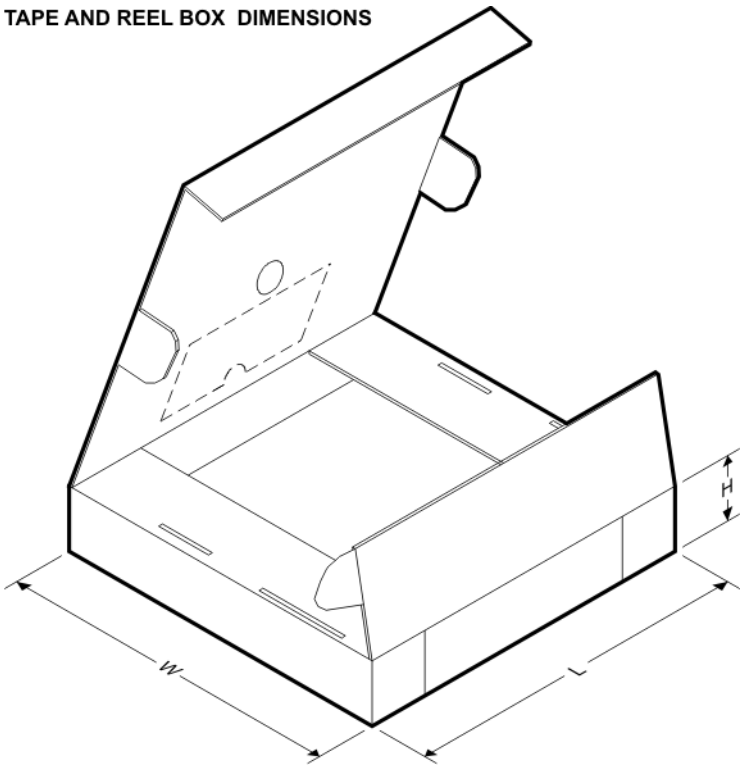
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24050DSQR	SON	DSQ	10	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24050DSQT	SON	DSQ	10	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24052DSQR	SON	DSQ	10	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24052DSQT	SON	DSQ	10	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24055DSSR	WSON	DSS	12	3000	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
BQ24055DSST	WSON	DSS	12	250	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

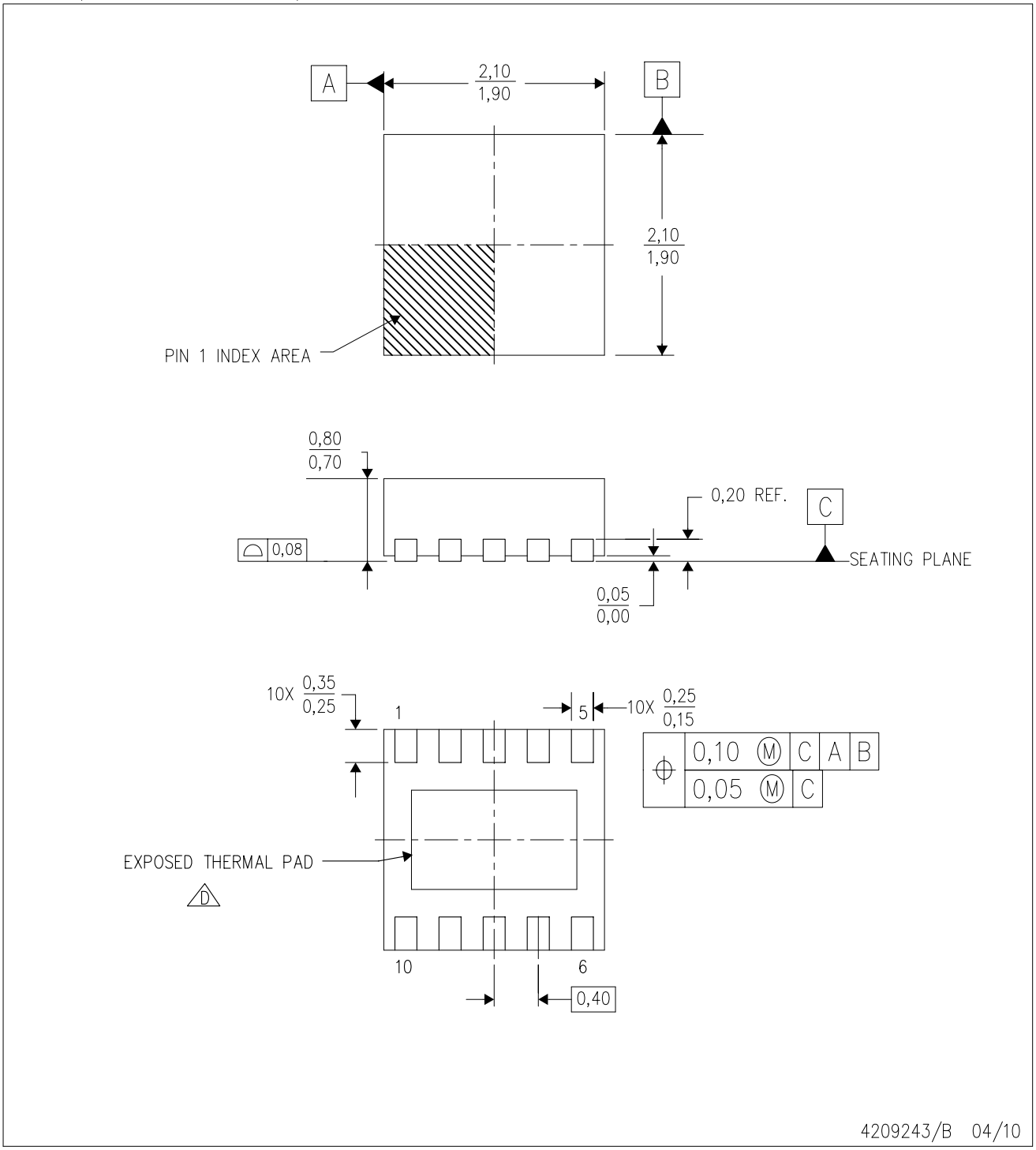
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24050DSQR	SON	DSQ	10	3000	195.0	200.0	45.0
BQ24050DSQT	SON	DSQ	10	250	195.0	200.0	45.0
BQ24052DSQR	SON	DSQ	10	3000	195.0	200.0	45.0
BQ24052DSQT	SON	DSQ	10	250	195.0	200.0	45.0
BQ24055DSSR	WSON	DSS	12	3000	195.0	200.0	45.0
BQ24055DSST	WSON	DSS	12	250	195.0	200.0	45.0

DSQ (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

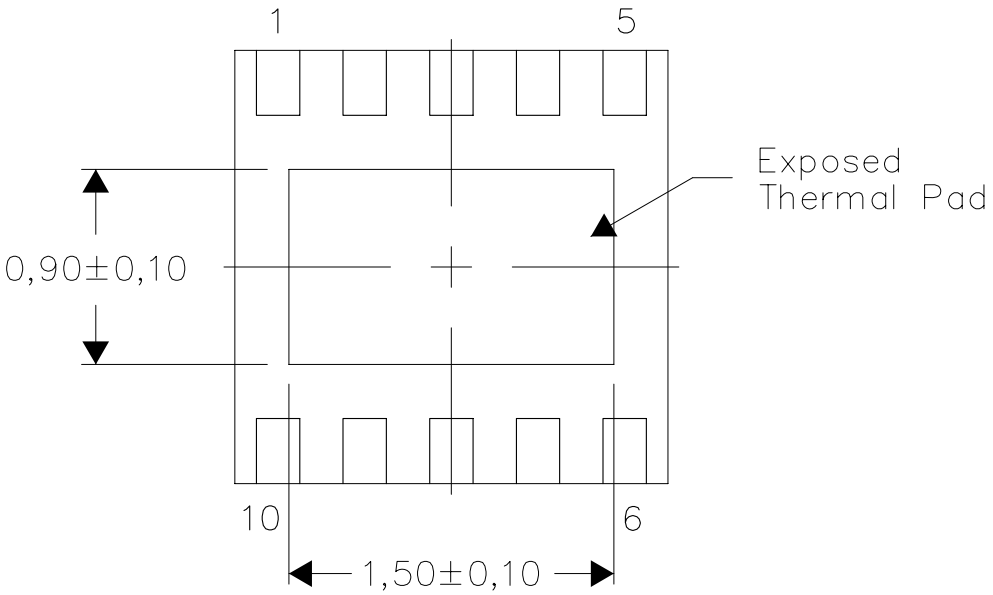
DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



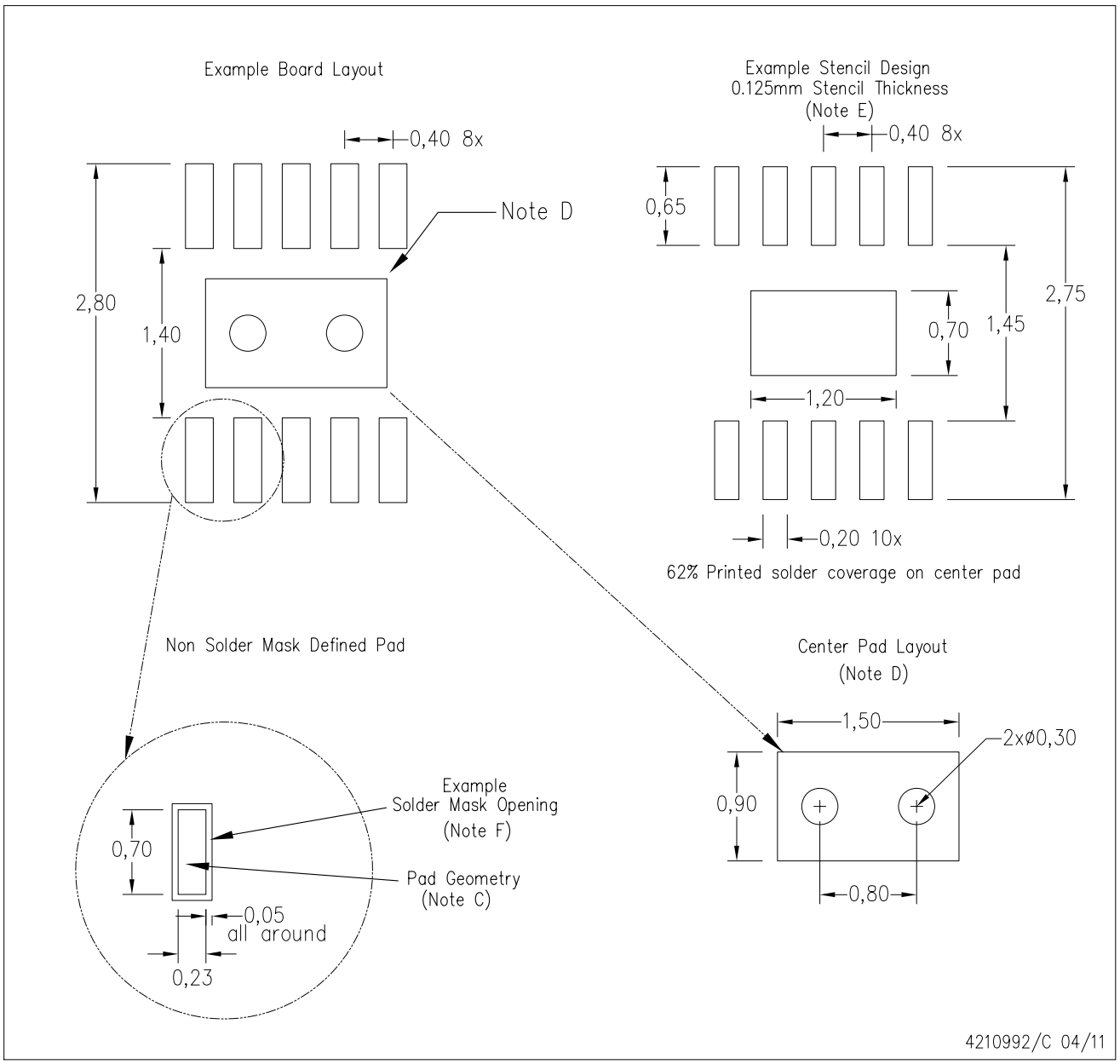
Bottom View

Exposed Thermal Pad Dimensions

4210993/C 04/11

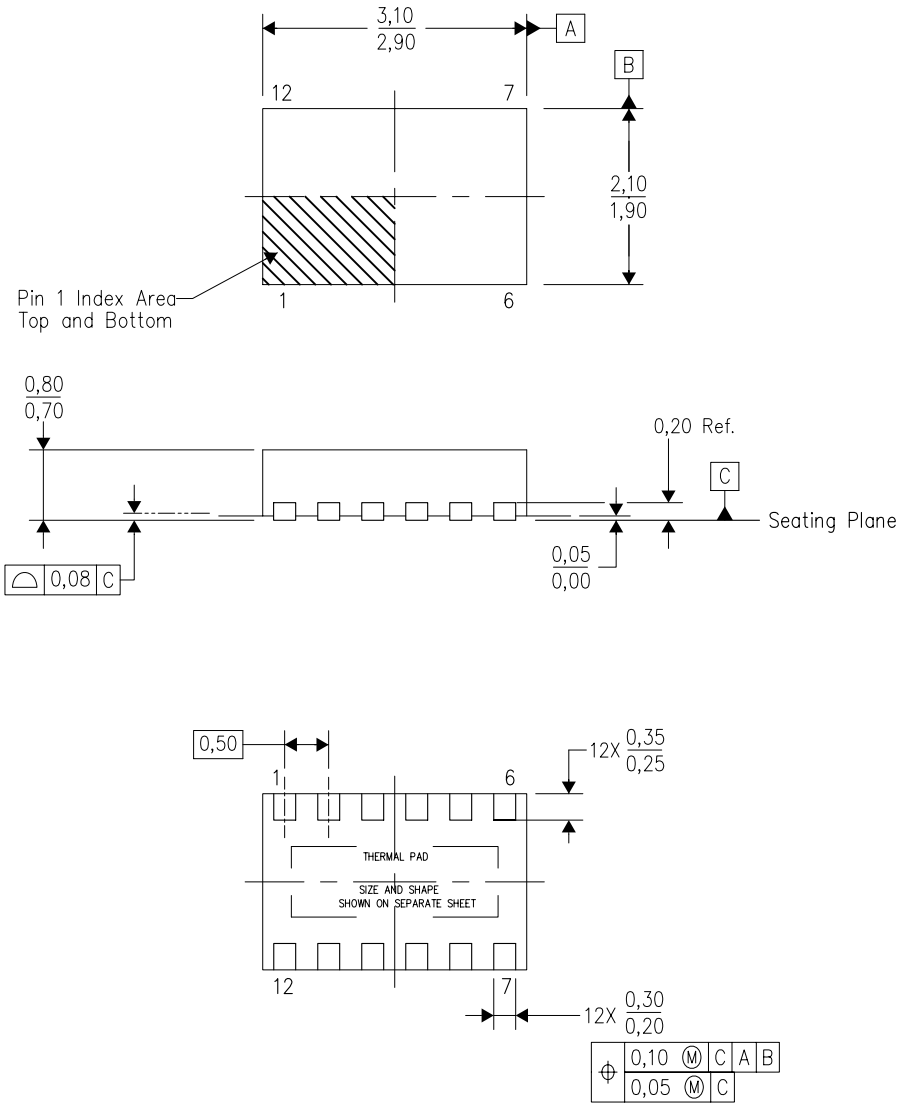
NOTES: A. All linear dimensions are in millimeters

DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4209244/C 07/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

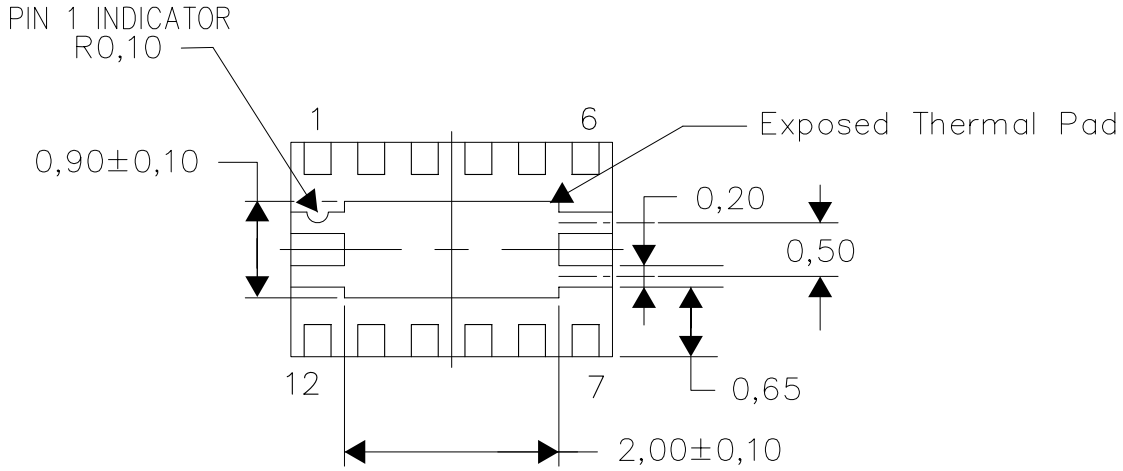
DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



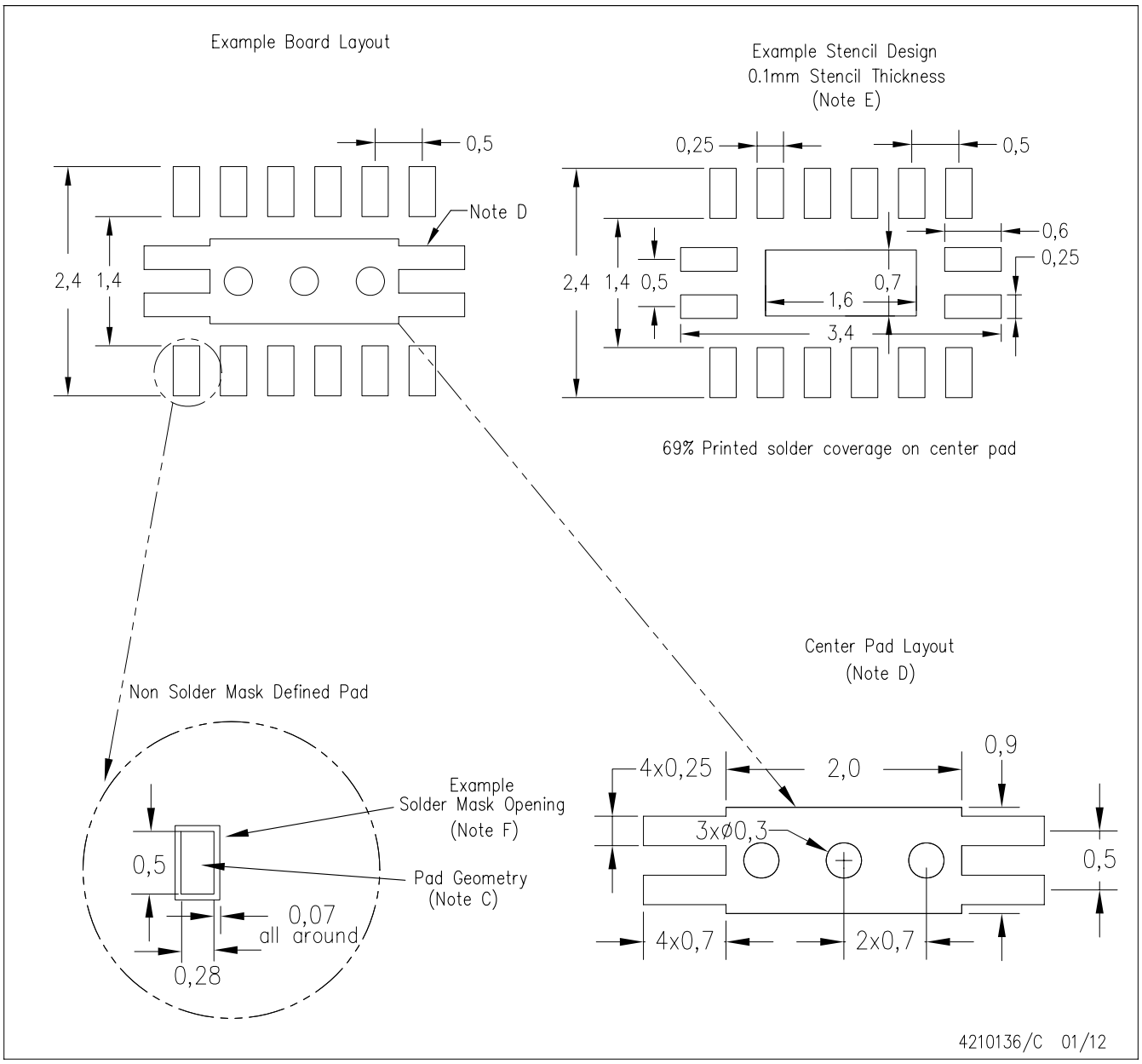
Bottom View

Exposed Thermal Pad Dimensions

4210135–2/C 02/12

NOTE: All linear dimensions are in millimeters

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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