



BCM5682 8-PORT GIGABIT SWITCH ON A CHIP

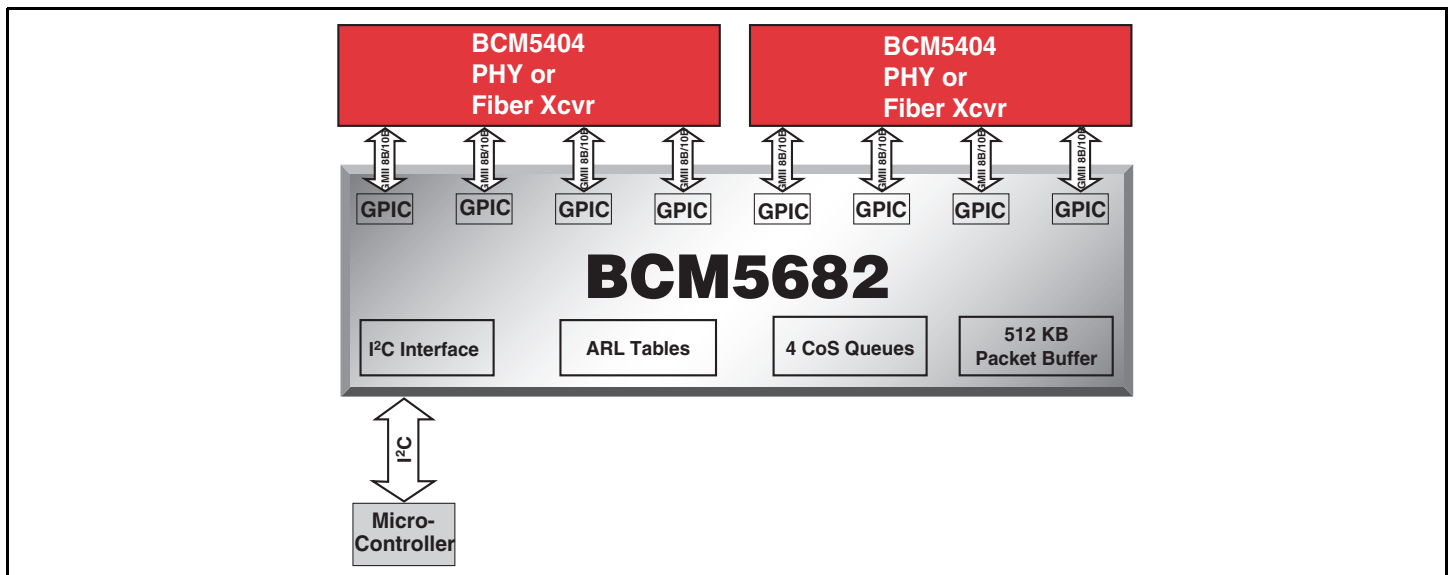
FEATURES

- Switch fabric delivers 12 Mpps (Million packets per second) providing line rate layer 2 forwarding
- Integrated 512 KB data packet data memory
 - Configurable to be static or dynamically allocated, or both
 - Highly efficient data memory packing
 - Efficient multicast handling
- Eight 10/100/1000 Ethernet MACs
 - GMII and TBI interface for direct connection to both Copper and Fiber PHYs
- IEEE 802.1 Support
 - D => Support for Spanning Tree
 - p => Support for Traffic Classification
- 8K MAC address table on-chip
- Flexible link aggregation on any port
- Low-power 3.3/2.5V operation
- 400-pin TBGA package

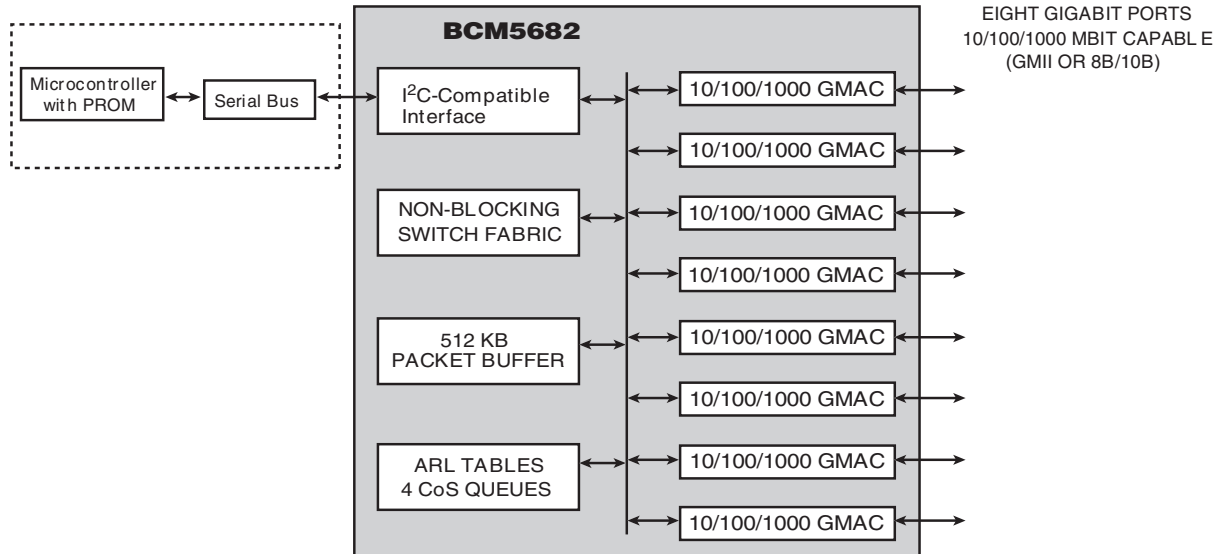
SUMMARY OF BENEFITS

- Represents the highest level of silicon integration achieved for a complete eight-port Gigabit switch, integrating the switch fabric, MACs, address tables and complete packet buffering functions.
- Provides the lowest system cost for stand-alone, unmanaged eight-port Gigabit switches.
- Supports the industry standard I2C interface and comes with reference code for the controller.
- Smart Switch is programmable for:
 - Port VLAN
 - Port Trunking
 - Port configuration
 - Port mirroring
- Supports four levels of CoS; maps to 802.1p priority levels.
- Provides advanced congestion control:
 - Packet flow control with HOL prevention
 - Backpressure support
 - Packet rate control (802.3x)
- At 3 ms, the BCM5682 provides the world's lowest latency for an eight-port Gigabit switch.

Non-Blocking Eight-Port Gigabit Switch



OVERVIEW



The BCM5682 represents the highest level of cost-reduction and integration available for the Gigabit Ethernet market. A Broadcom-based eight-port Gigabit switch reduces today's costs by as much as 50% over competing solutions.

The I2C interface supports both master and slave modes of operation. This interface is designed to support the unmanaged and Smart Switch market, achieving the lowest possible system cost and the highest level of design efficiency and reliability.

The 10/100/1000 Mbit interface enables users to connect at any speed required on a given port. This triple-speed interface automatically negotiates to support legacy devices alongside newer, higher bandwidth devices, all in the same switch.

The PHY interface is compatible with a BCM8002 SERDES for fiber optics, a BCM5401, BCM5402, BCM5404, or BCM5411 Gigabit PHY for 1000TX, or a standard 100TX PHY.

The integrated 512 KB data packet memory eliminates the need for external data packet storage. The memory organization and structure can be optimized to provide a minimum fixed allocation of buffer space per port and a dynamic pool size, to absorb any bursty traffic requirements.

The BCM5682 supports IEEE 802.1p with up to four Class of Service (CoS) queues per egress port, along with traffic class expediting and dynamic multicast filtering.

The chip implements a number of advanced mechanisms for flow control. Two mechanisms, cell-based HOL blocking and packet-based HOL blocking, to prevent Head Of Line blocking on a per-port basis.

A packet aging mechanism discards packets residing in the switch's packet memory. The packet age limit is programmable.

A backpressure mechanism allows flexible flow control on packet transactions. The limit at which backpressure is detected is based on the amount of memory utilized by the packets on an input port. This limit is programmable on a per-port basis.

Another mechanism provides programmable threshold limits to prevent packets from flooding into other parts of the network. Three types of packets can be monitored and separate counters are maintained from each type of packet.

In summary, the highly flexible BCM5682 provides 12 Mpps (line rate) switching along with sophisticated packet flow and prioritization capabilities.

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

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5682-PB05-R 07/08/04

Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com