Video switch for CANAL-Plus decoder
BA7630S / BA7630F

The BA7630S and BA7630F are decoder switching ICs for the scrambled broadcasts in France. The ICs include a 3-input multiplexer, 2-input multiplexers with 6dB amplifiers, and a 9-bit serial-to-parallel converter.
These ICs greatly simplify decoder switching, and can be connected to a control microprocessor using just two lines.

●Applications
Video cassette recorders

●Features
1) All the switching functions required for SECAM CANAL plus decoder integrated onto one chip.
2) Built-in 9-bit serial-to-parallel converter for decoder and TV control reduces number of microprocessor wiring connections required.
3) Inputs have a sync-tip clamp.
4) The switch section can be used independently.
5) Low power consumption off a 5V supply.

●Absolute maximum ratings (Ta = 25°C)

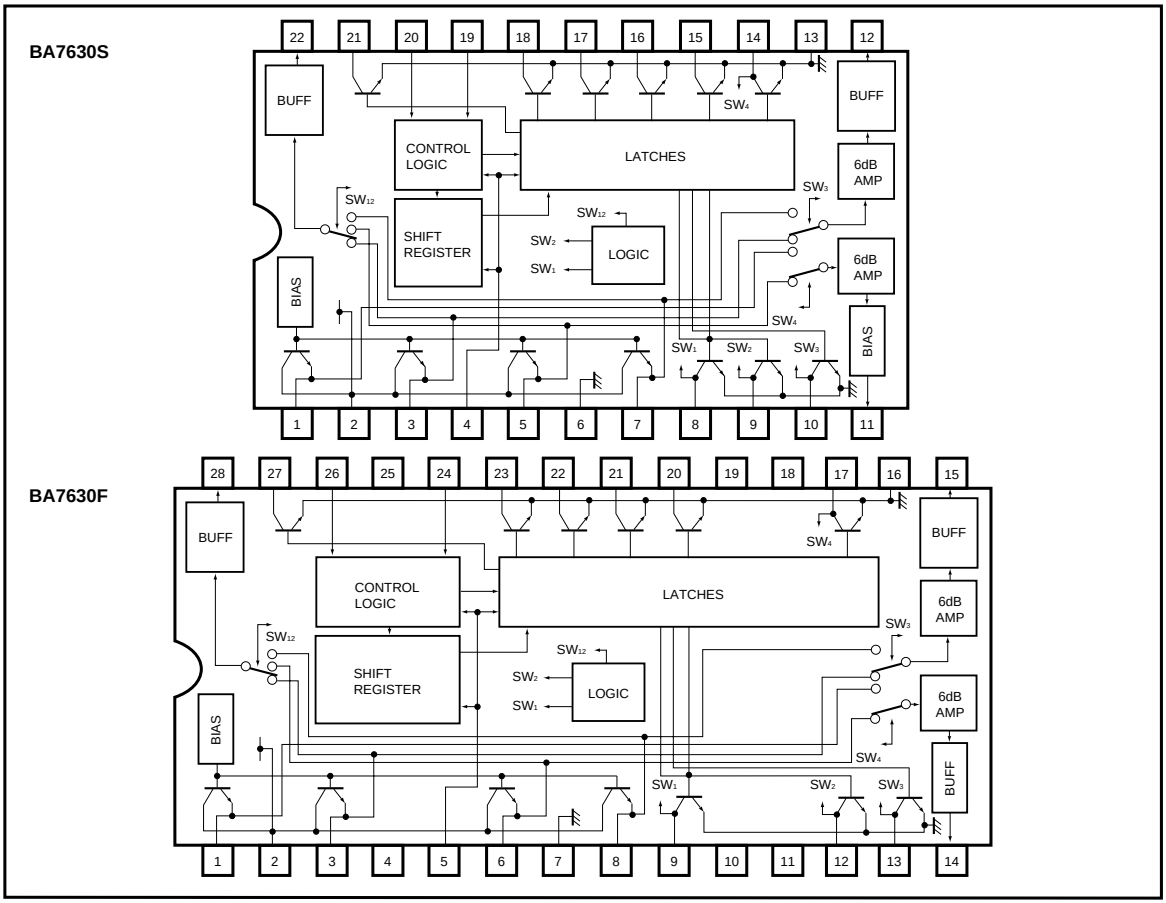
Parameter	Symbol	Limits		Unit
Power supply voltage	V_{CC}	9*1		V
Power dissipation	Pd	BA7630S	500*2	mW
		BA7630F	600*3	
Operating temperature	Topr	– 25 ~ + 70		°C
Storage temperature	Tstg	– 55 ~ + 125		°C

*1 13V for switches 1 to 9.
*2 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.
*3 Reduced by 6.0mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V

●Block diagram



●Pin descriptions

Pin No.	Pin name	Pin No.	Pin name
1	IN 4	12 (15)	OUT 2
2	V_{CC}	13 (16)	GND
3	IN 1	14 (17)	SW 4 IN / OUT
4 (5)	RESET IN	15 (20)	SW 5 OUT
5 (6)	IN 2	16 (21)	SW 6 OUT
6 (7)	GND	17 (22)	SW 7 OUT
7 (8)	IN 3	18 (23)	SW 8 OUT
8 (9)	SW 1 IN / OUT	19 (24)	CLOCK IN
9 (10)	SW 2 IN / OUT	20 (26)	DATA IN
10 (13)	SW 3 IN / OUT	21 (27)	SW 9 OUT
11 (14)	OUT 3	22 (28)	OUT 1

Pin numbers in parentheses are for the BA7630F.

●Electrical characteristics (unless otherwise noted Ta = 25°C and V_{CC} = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Supply current	I_{CC}	—	28	40	mA	—	Fig.1
⟨Analog⟩							
Maximum output level	V_{om}	2.5	2.8	—	V_{P-P}	f = 1kHz, THD = 0.5%	Fig.1
Voltage gain 1	G_{V1}	– 0.5	0	0.5	dB	f = 1MHz, V_{IN} = 1.0V_{P-P}	
Voltage gain 2	G_{V2}	5.5	6.0	6.5	dB	f = 1MHz, V_{IN} = 1.0V_{P-P}	
Frequency characteristic	G_f	– 4.0	– 1.5	+ 1.0	dB	10MHz / 1MHz V_{IN} = 1.0V_{P-P}	
Interchannel crosstalk	C_{TM}	—	– 60	– 45	dB	f = 4.43MHz V_{IN} = 1.0$_{P-P}$	
SW_1 ~ SW_4 switch level	$V_{TH1 \sim 4}$	1.0	2.0	3.0	V	—	
⟨Digital⟩							
"H" input voltage	V_{IH}	3.0	—	—	V	—	Fig.3
"L" input voltage	V_{IL}	—	—	1.0	V	—	
"H" input current	I_{IH}	—	2	10	µA	—	Fig.2
"L" input current	I_{IL}	– 80	– 100	– 150	µA	—	
"H" output leakage current 1	$I_{QH1 \sim 4}$	150	230	350	µA	V_{CC} = 12V	
"H" output leakage current 2	$I_{QH5 \sim 9}$	—	0	50	µA	V_{CC} = 12V	
"L" output voltage	V_{QL}	—	0.1	0.5	V	I_{CC} = 2mA	Fig.1
Maximum clock frequency	$f_{Max.}$	250	500	—	kHz	—	
Setup time	t_{su}	—	0.1	1.0	µs	—	

●Measurement circuits

BA7630S

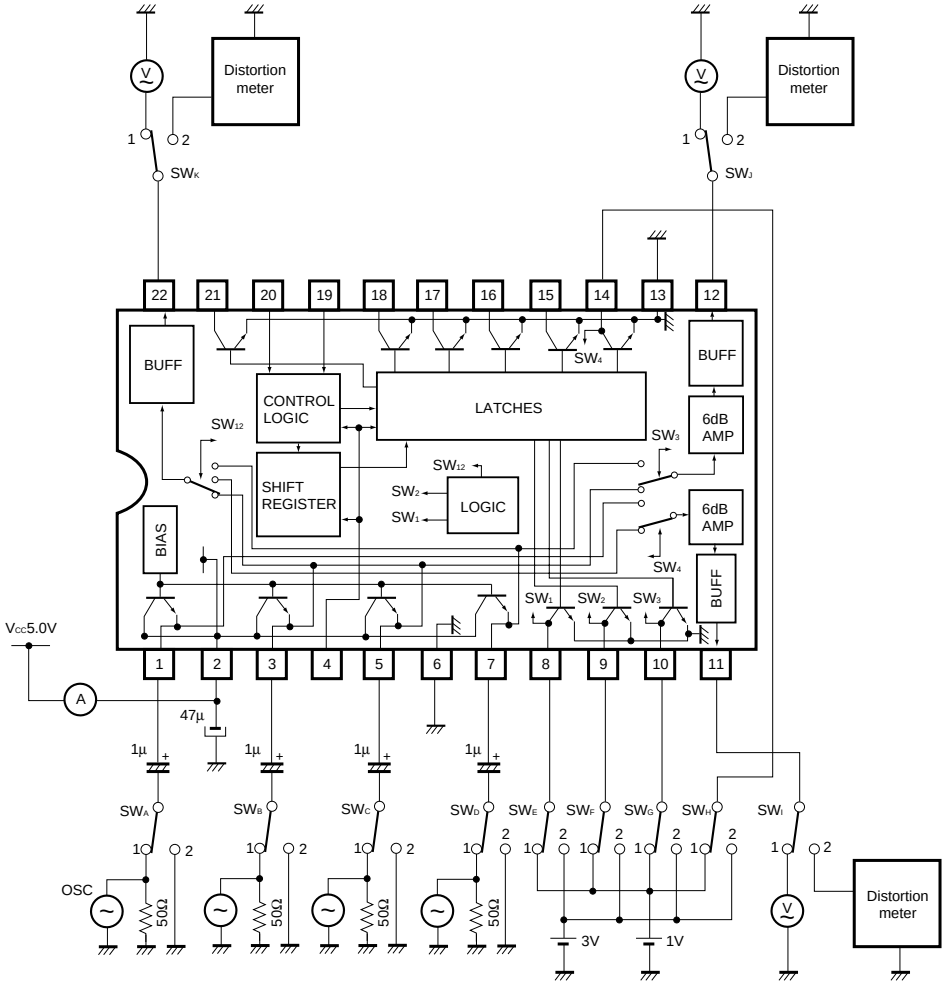


Fig.1

BA7630S

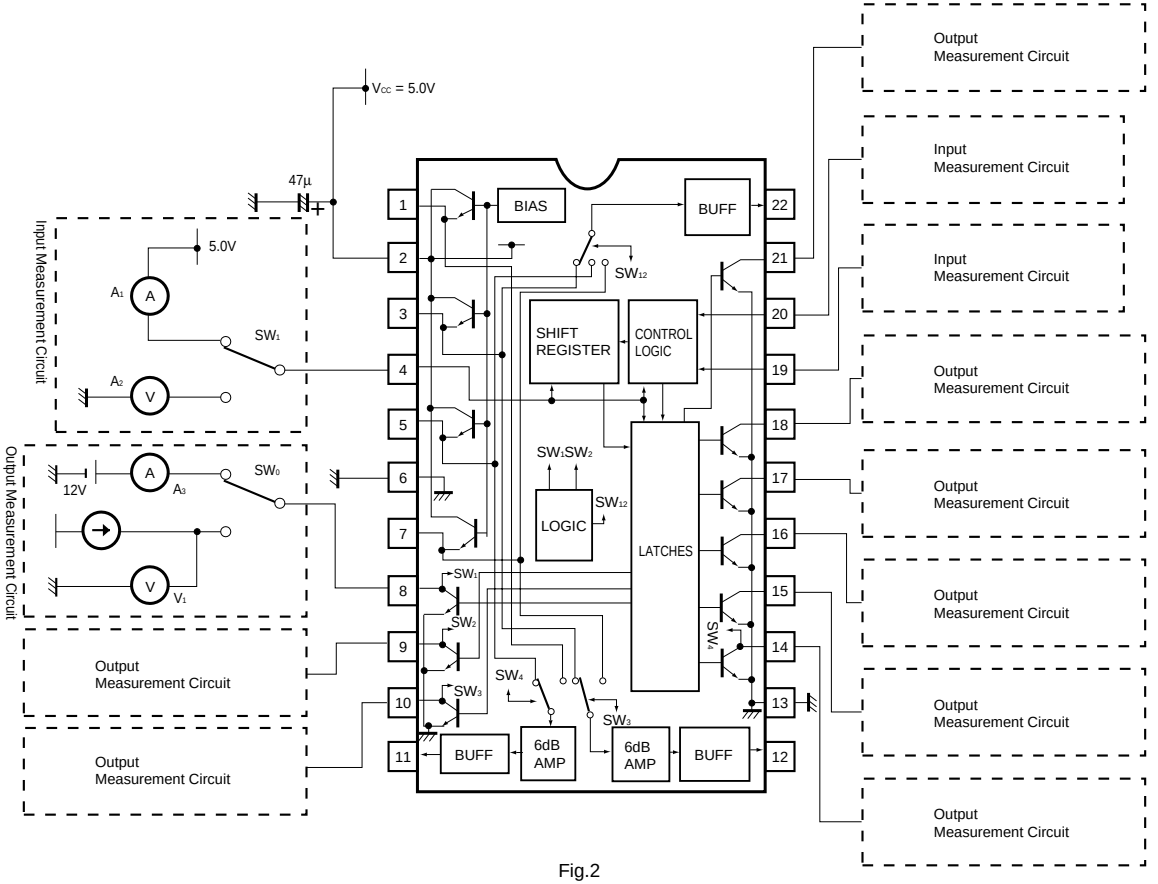


Fig.2

BA7630S

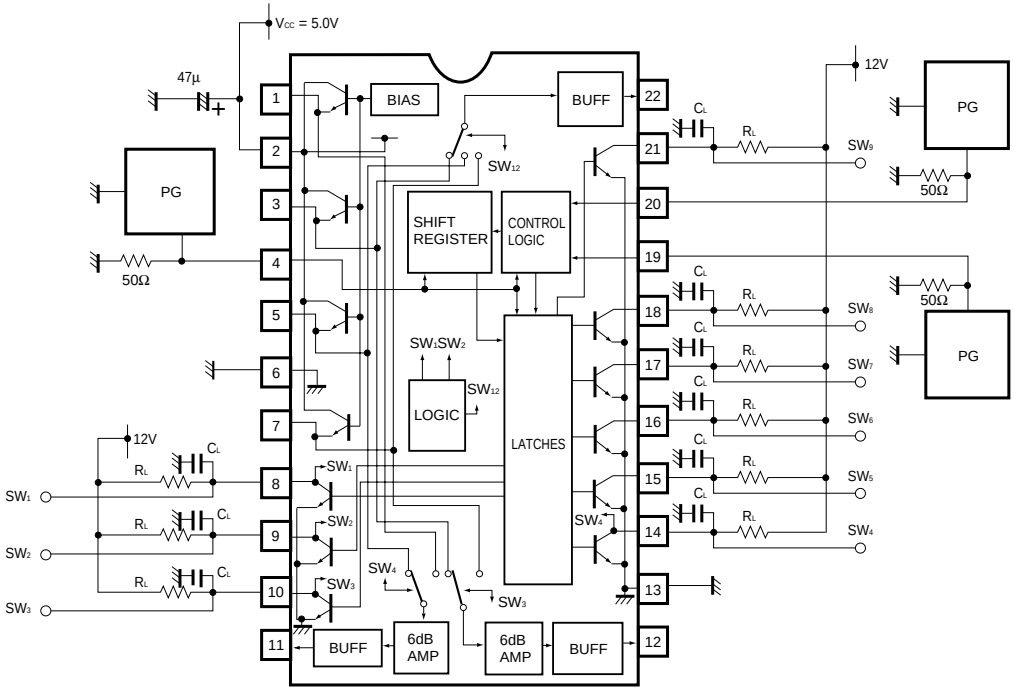


Fig.3

●Measurement conditions

Parameter	Symbol	Switch setting											Measurement method
		SW_A	SW_B	SW_C	SW_D	SW_E	SW_F	SW_G	SW_H	SW_I	SW_J	SW_K	
Current dissipation	I_{CC}	2	2	2	2	2	2	2	2	×	×	×	—
Maximum output level	$V_{om}1$-1 $V_{om}2$-1 $V_{om}3$-1	2 2 2	1 2 2	2 1 2	2 2 1	1 1 2	1 2 ×	× × ×	× × ×	× × ×	× × ×	2 2 2	Note 1
	$V_{om}1$-2 $V_{om}3$-2	2 2	1 2	2 2	2 1	× ×	× ×	2 2	× ×	× ×	2 2	× ×	
	$V_{om}2$-3 $V_{om}4$-3	2 1	2 2	1 2	2 2	× ×	× ×	× ×	1 2	2 2	× ×	× ×	
Voltage gain 1	G_{v1}1-2 G_{v1}3-2 G_{v1}2-3 G_{v1}4-3	2 2 2 1	1 2 2 2	2 2 1 2	2 1 2 2	× × × ×	× × × ×	1 2 × ×	× × 1 2	× × 2 2	1 2 × ×	× × × ×	Note 2
Voltage gain 2	G_{v2}1-1 G_{v2}2-1 G_{v2}3-1	2 2 2	1 2 2	2 1 2	2 2 1	1 1 2	1 2 ×	× × ×	× × ×	× × ×	× × ×	1 1 1	
Frequency characteristics	G_f1-1 G_f2-1 G_f3-1	2 2 2	1 2 2	2 1 2	2 2 1	1 1 2	1 2 ×	× × ×	× × ×	× × ×	× × ×	2 2 2	Note 3
	G_f1-2 G_f3-2	2 2	1 2	2 2	2 1	× ×	× ×	2 2	× ×	× ×	2 2	× ×	
	G_f2-3 G_f4-3	2 1	2 2	1 2	2 2	× ×	× ×	× ×	1 2	2 2	× ×	× ×	
Interchannel crosstalk	C_{TM}1-1-2 C_{TM}1-1-3 C_{TM}2-1-1 C_{TM}2-1-3 C_{TM}3-1-1 C_{TM}3-1-2	2 2 2 2 2 2	2 2 1 2 1 2	1 2 2 2 2 1	2 1 2 1 2 2	1 1 1 1 2 2	1 1 2 2 2 2	× × × × × ×	× × × × × ×	× × × × × ×	× × × × × ×	1 1 1 1 1 1	Note 4
	C_{TM}1-2-3 C_{TM}3-2-1	2 2	2 1	2 2	1 2	× ×	× ×	1 2	× ×	× ×	1 1	× ×	
	C_{TM}2-3-4 C_{TM}4-3-2	1 2	2 2	2 1	2 2	× ×	× ×	× ×	1 2	1 1	× ×	× ×	

The measurements in the above table were made with switching voltage levels for SW_1 to SW_4 of "L" = 1V, and "H" = 3V.

Note 1: Connect distortion meters to the outputs. Adjust the input level so that the output distortion is 0.5% for a f = 1kHz sine wave input.
This output voltage is the maximum output level V_{om} (V_{P-P}).

Note 2: Input a f = 1MHz, $1V_{P-P}$ sine wave. The voltage gain G_V = 20 log V_{OUT} / V_{IN} (dB).

Note 3: Input a f = 1MHz and 10MHz, $1V_{P-P}$ sine wave. The frequency characteristic G_f = 20 log V_{OUT} (f = 10M) / V_{OUT} (f = 1M) (dB).

Note 4: Input a f = 4.43MHz, $1V_{P-P}$ sine wave.
0dB amplifier SW crosstalk is C_{TM0}, and the 6dB amplifier SW crosstalk is C_{TM6}.
C_{TM0} = 20 log V_{OUT} / V_{IN} (dB)
C_{TM6} = 20 log V_{OUT} / V_{IN} + 6 (dB)

●Circuit operation

Digital block truth table

INPUT			OUTPUT	Note
Reset	Clock	Data	SW_1 ····· SW_9	
H	×	×	H ····· H	—
L	L	×	$SW_{1\text{-}O}$ ····· $SW_{9\text{-}O}$	—
L	H	×	$SW_{1\text{-}O}$ ····· $SW_{9\text{-}O}$	—
L	↑	H	$SW_{1\text{-}O}$ ····· $SW_{9\text{-}O}$	Data "L" sent to internal shift register
L	↑	L	$SW_{1\text{-}O}$ ····· $SW_{9\text{-}O}$	Data "H" sent to internal shift register
L	↓	L	$SW_{1\text{-}O}$ ····· $SW_{9\text{-}O}$	Internal shift register data unchanged
L	↓	H	$SW_{1\text{-}N}$ ····· $SW_{9\text{-}N}$	Contents of internal shift register sent to internal latch

Note 1: H: high level
Note 2: L: low level
Note 3: ×: either H or L
Note 4: ↑: L to H transition
Note 5: ↓: H to L transition
Note 6: $SW_{1\text{-}O}$ to $SW_{9\text{-}O}$: SW_1 to SW_9 levels before establishing the input conditions shown in the table.
Note 7: $SW_{1\text{-}N}$ to $SW_{9\text{-}N}$
nearest clock ↓ transition.

Analog truth table

(1) OUT1 switch

SW_1	SW_2	RESET	SELECT
L	L	H	IN1
L	H	H	IN2
H	L	H	IN3
H	H	H	IN3

(2) OUT2 switch

SW_3	RESET	SELECT
L	H	IN1
H	H	IN3

(3) OUT3 switch

SW_4	RESET	SELECT
L	H	IN2
H	H	IN4

Note: When using the switches independently without the digital block, the RESET pin must be set to "H".

●Digital circuit operation

(1) Introduction

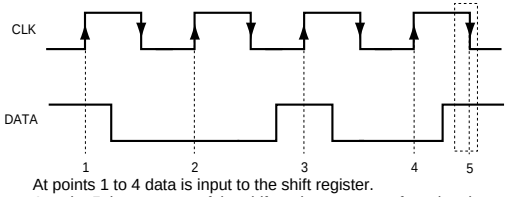
The BA7630S has 9-bit serial-to-parallel converter and latch circuit that has been included to expand the number of microprocessor output ports. The breakdown voltage of the output pins is 13V, so switch them in the range 0 to 12V. In addition to controlling the BA7630S switching block, these outputs can be used to control audio switching, scrambling decoders, and television sets.

(2) Using the serial-to-parallel convertor block

Signal input is basically done using clock and date pulses. As shown in Fig.10, the date is read on the rising edge of the clock pulses. If the date is “H” on the rising edge of the clock pulse, a “L” data bit is input to the shift register, and if the data is “L” on the rising edge of the clock pulse, a “H” data bit is input to the shift register. The shift register is sequentially incremented by the bit corresponding to SW_1. Data in excess of 9 bits is sequentially discarded.

If the data is “H” on a falling edge of the clock, the contents of the shift register are read into the internal latch, and simultaneously output to the output port (the data polarity is inverted on output). This output is maintained until the latch is setup again.

To reset, set the RESET pin to “H”. The internal shift register and latch contents go low (latch output all “H”), for the duration that RESET is held high.



At points 1 to 4 data is input to the shift register.
At point 5 the contents of the shift register are transferred to the latch and simultaneously output.

Fig. 4 CLK and DATA relationship

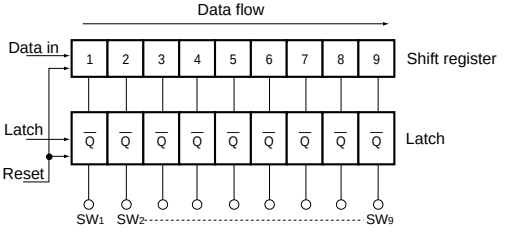


Fig. 5 Digital block

(3) Pulse timing

The pulse timing diagrams are given below.

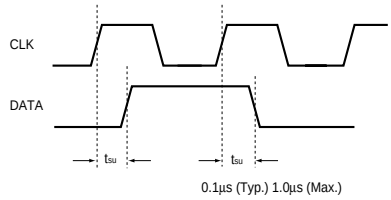


Fig. 6 Clock rising edge and data relationship (setup time)

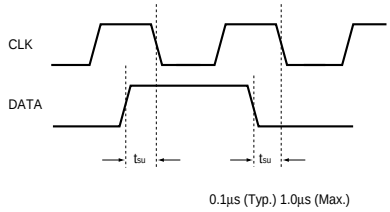


Fig. 7 Clock falling edge and data relationship (setup time)

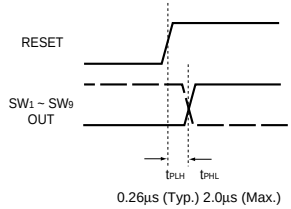


Fig. 8 Reset and output relationship (reset transmission time)

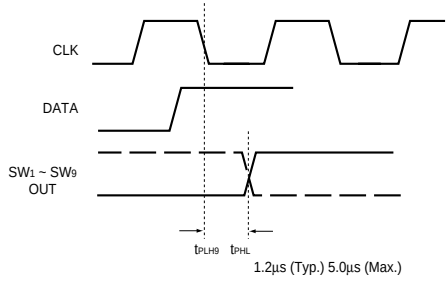


Fig. 9 Clock falling edge and output relationship (latch transmission time)

●Timing chart

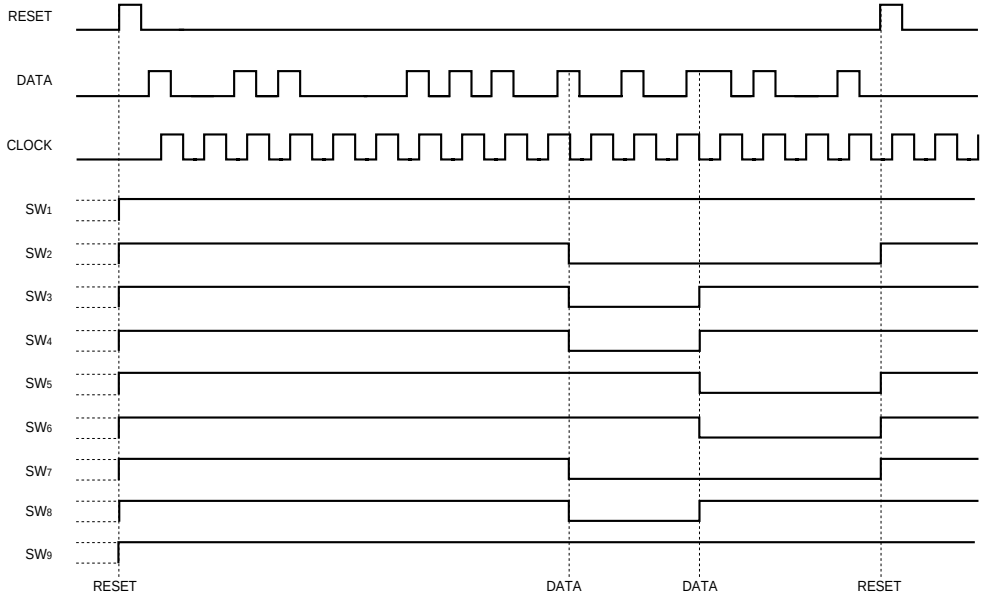
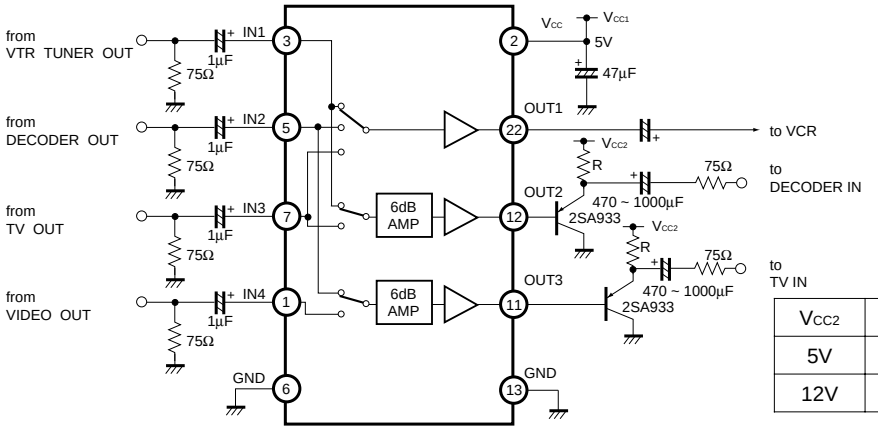


Fig.10

●Application examples

(1) Analog block

BA7630S pin layout



V_{CC2}	R
5V	100
12V	390

Fig.11

(2) Digital block

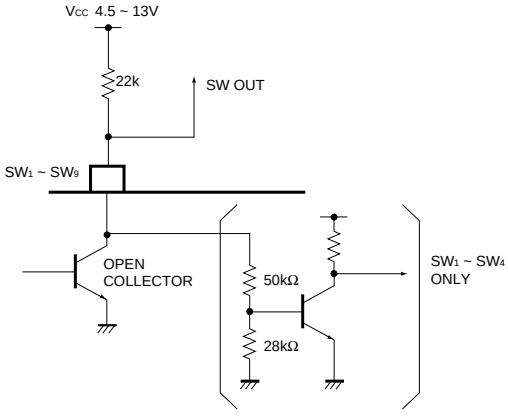


Fig.12

●Electrical characteristic curves

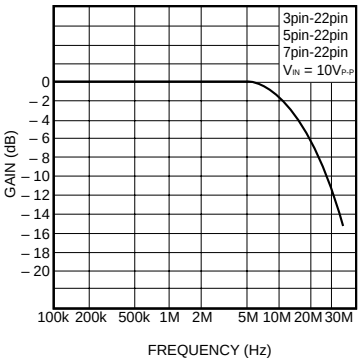


Fig. 13 Frequency characteristic(OUT1)

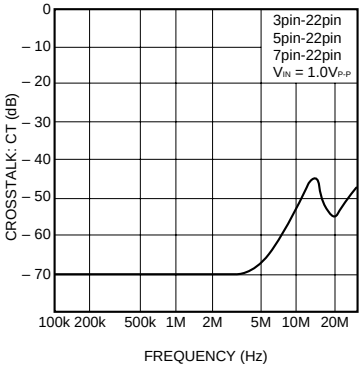


Fig. 14 Crosstalk characteristic (OUT1)

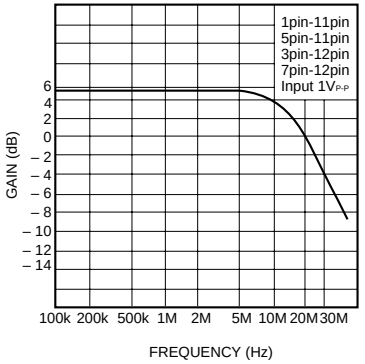


Fig. 15 Frequency characteristic (OUT2 and OUT3)

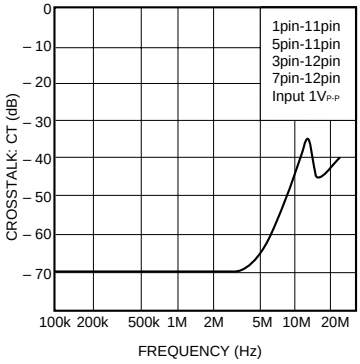
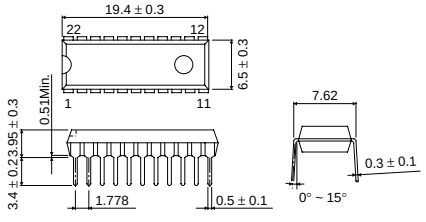


Fig. 16 Crosstalk characteristic (OUT2 and OUT3)

●External dimensions (Units: mm)

BA7630S



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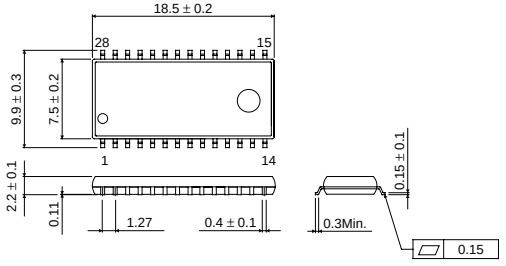

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