SECAM chroma signal processor for VHS VCRs

BA7207AS/BA7207AK

The BA7207AS and BA7207AK are LSI components that incorporate the contain circuitry required for SECAM chroma signal processing. The ICs have both recording and playback systems and each includes a bell filter, a band-pass filter, a limiter amplifier, a multiply-by-four circuit, a divide-by-four circuit, and a sync-gate circuit.

●Applications

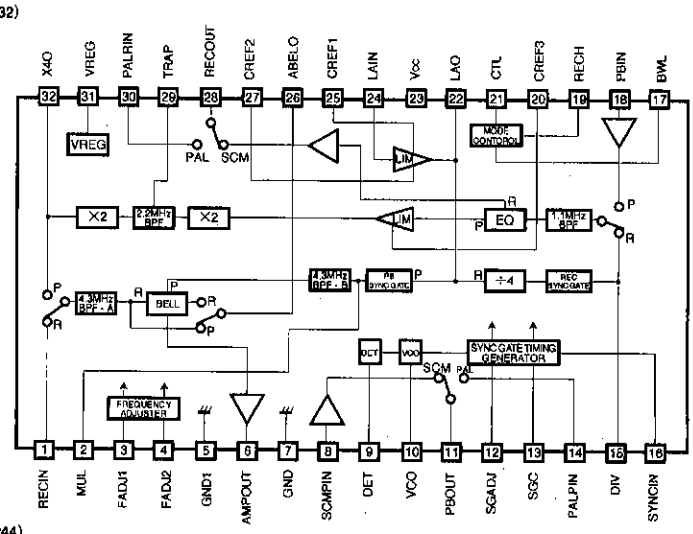
SECAM and VHS format video cassette recorders and camcorders

●Features

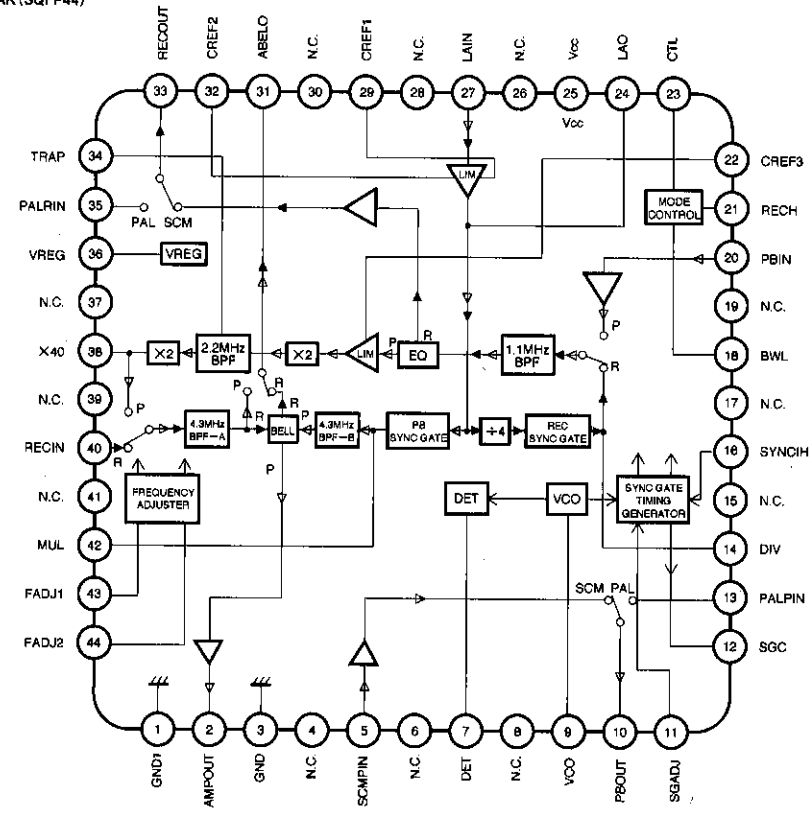
1)All filters required for SECAM chroma signal processing are provided.
2)Built-in chroma killer circuit.
3)Built-in switch circuit for selecting PAL chroma or SECAM chroma for the PB/REC system output.

●Block diagram

BA7027AS (SDIP32)



BA7207AK (SQFP44)



●Absolute maximum ratings (Ta=25℃)

Parameter		Symbol	Limits	Unit
Power supply voltage		Vcc	7	V
Power dissipation	BA7207AS	Pd	1400 (SDIP32) *1	mW
	BA7207AK		850 (QFP44) *2	
Operating temperature	BA7207AS	Topr	−25~75	℃
	BA7207AK		−25~65	
Storage temperature		Tstg	−55~125	℃

*1 Reduced by 14mW for each increase in Ta of 1°C over 25°C .
*2 When installed on a 70mm x 70mm, t = 1.6mm glass epoxy PCB, reduced by 8.5W for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V

●Pin descriptions

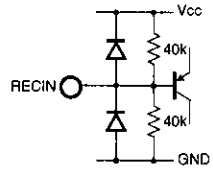
Pin No.	Name	Function
1(40)	RECIN	Recording system input. Input the REC system chroma signal.
2(42)	MUL	PB sync gate output. Test pin. Outputs the chroma signal after it is multiplied by four and passed through the sync gate. Normally connected to Vcc to prevent interference.
3(43)	FADJ1	Filter fo adjustment pin 1. Used to adjust fo for the equalizer, 1.1MHz BPF and 2.2MHz BPF. Connect a resister and variable resistor from this pin to GND.
4(44)	FADJ2	Filter fo adjustment pin 2. Used to adjust fo for the bell filter, 4.3MHz BPF-A and 4.3MHz BPF-B. Connect a resister and variable resistor from this pin to GND.
5(1)	GND1	GND terminal.
6(2)	AMPOUT	PB system preamplifier output. Connect to GND via a variable resistor to adjust the level, and input to pin 8.
7(3)	GND	GND terminal.
8(5)	SCMPIN	PB system output amplifier input. Input the level-adjusted PB system SECAM chroma signal.
9(7)	DET	Phase comparator output. Connect to GND via a RC LPF to obtain the error voltage.
10(9)	VCO	VCO oscillator frequency control pin. The error voltage is input via a resistor. Connected to GND via free-running frequency setting resistor.
11(10)	PBOUT	PB system output. Outputs the PB system chroma signal.
12(11)	SGADJ	Fine adjustment for the sync gate phase. The voltage from a resistor divider is used for fine adjustment of the gate phase of the sync gate. Normally open.
13(12)	SGC	Sync gate timing output. Test pin. Outputs the REC sync gate timing. Normally open.
14(13)	PALPIN	PAL PB system input. Input chroma signal for the PAL PB system.
15(14)	DIV	Divide-by-four divider output. Test pin. Outputs the chroma signal after it has been divided by four. Normally connected to Vcc to prevent interference.
16	SYNCIN	Delayed sync signal input. Input the synchronously-separated composite

Pin No.	Name	Function
17(18)	BWL	Chroma killer mode setting terminal. "L" sets the IC in chroma killer mode.
18(20)	PBIN	PB system input terminal. Input chroma signal for the PB system.
19(21)	RECH	REC/PB mode switch terminal. Set to open or "H" for REC mode, "L" for PB mode.
20(22)	CREF3	Bias terminal for the limiter amplifier before X2. Connect to GND via a capacitor.
21(23)	CTL	SECAM/PAL output switch terminal. Selects the signal output for the REC/PB terminal. Set to open or "H" for SECAM output mode, "L" for PAL mode.
22(24)	LAO	Limiter amplifier output. Test pin. Outputs the amplitude-limited chroma signal. Normally connected to Vcc to prevent interference.
23(25)	Vcc	Power supply.
24(27)	LAIN	Limiter amplifier input. Input the de-emphasised chroma signal.
25(29)	CREF1	Limiter amplifier bias pin 1. Connect to GND via a capacitor.
26(31)	ABELO	REC BELL output terminal. When in REC mode, de-emphasised chroma signal is output via REC BELL. When in PB mode, the PB system chroma signal is output after being multiplied by four.
27(32)	CREF2	Limiter amplifier bias pin 2. Connect to GND via a capacitor.
28(33)	RECOUT	REC system output terminal. REC system chroma signal output.
29(34)	TRAP	TRAP connection terminal. Connect TRAP that rejects spurious signal component after X2 multiplication.
30(35)	PALRIN	PAL REC system input terminal. PAL REC system chroma signal input.
31(36)	VREG	Regulated voltage output. Output for the regulated 2.5V reference voltage used for internal biasing. Connect to GND via a bypass capacitor.
32(38)	X40	X4 multiply output terminal. Test pin. Outputs the chroma signal after it is multiplied by four. Normally connected to Vcc to prevent interference.

* BA7207AK pin numbers are given in brackets.

●Input/output circuits

1pin
(40pin)



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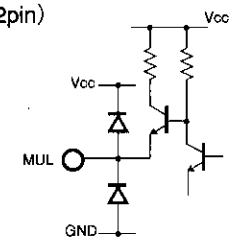

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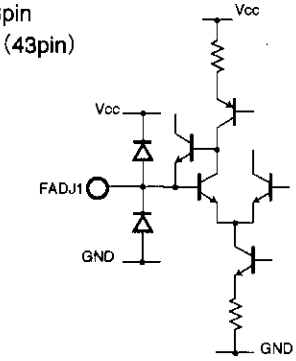

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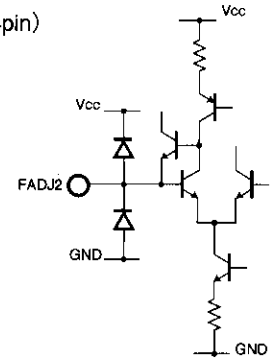

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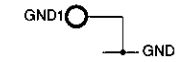

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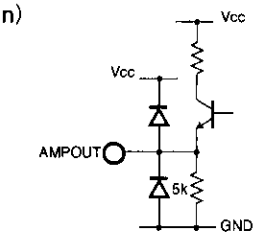

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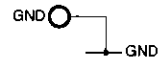

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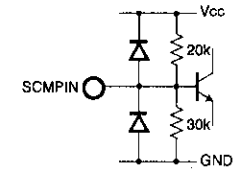

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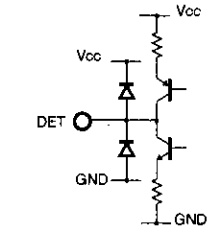

●Input/output circuits

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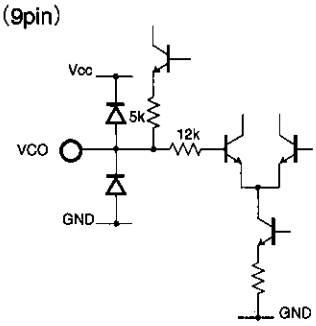

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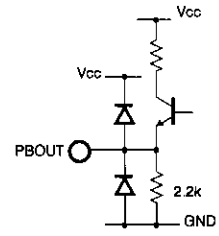

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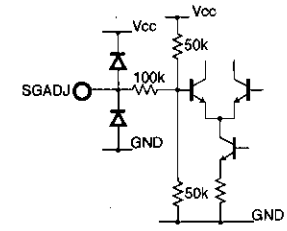

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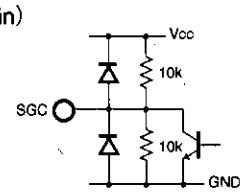

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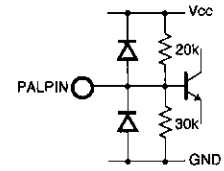

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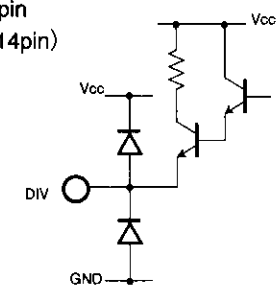

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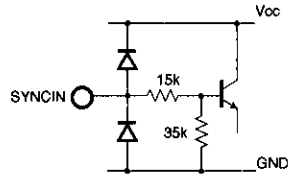

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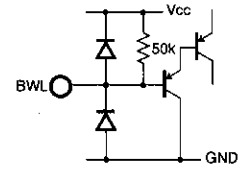

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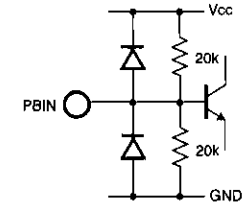

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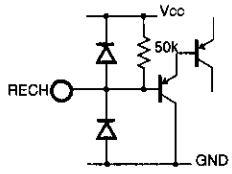

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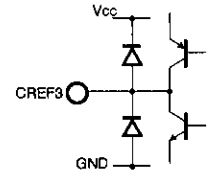

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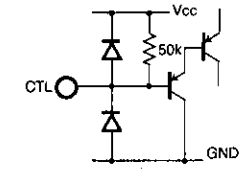

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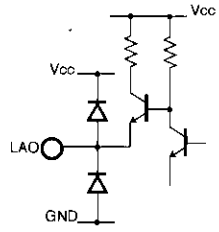

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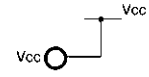

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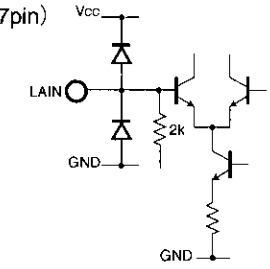

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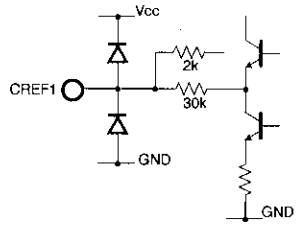

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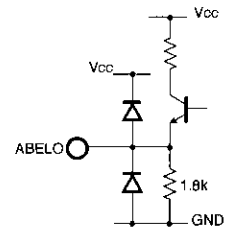

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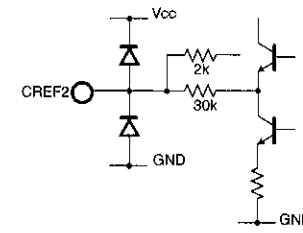

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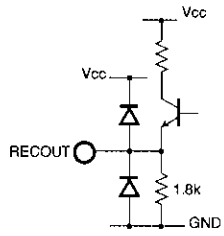

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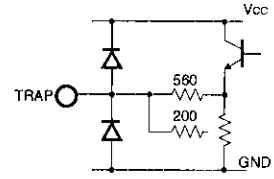

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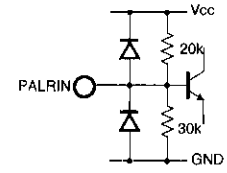

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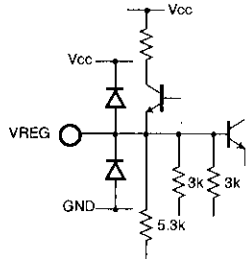

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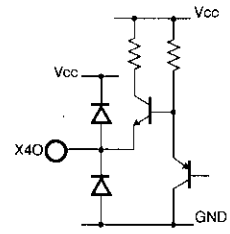


Pin numbers in parentheses are for the BA7207AK.

●Electrical characteristics (Unless otherwise specified Ta=25℃ V_{CC}=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
〈Total device〉							
REC mode circuit current	I_{REC}	39.2	56.0	72.8	mA	REC mode	Fig.1
PB mode circuit current	I_{PB}	46.9	67.0	87.1	mA	PB mode	Fig.1
Regulator voltage	V_{REG}	2.38	2.53	2.68	V		Fig.1
〈Sync-gate block〉							
VCO free-running frequency	fosc	13.8	15.625	17.4	kHz		Fig.1
Capture range "H"	CR_H	1.8	—	—	kHz	Delayed sync input	Fig.1
Capture range "L"	CR_L	—	—	−1.8	kHz	Delayed sync input	Fig.1
Lock range "H"	LR_H	2.2	—	—	kHz	Delayed sync input	Fig.1
Lock range "L"	LR_L	—	—	−2.2	kHz	Delayed sync input	Fig.1
〈REC system〉							
RECOUT output amplitude	V_{REC}	187.5	250.0	312.5	mVpp	Cyan level (cyan frequency)	Fig.1
Unwanted spectrum rejection							
4MHz component	HD_{R4}	—	—	−25	dB	V_1=170mV$_{PP}$, 4.286MHz	Fig.1
3MHz component	HD_{R3}	—	—	−25	dB	V_1=170mV$_{PP}$, 4.286MHz	Fig.1
2MHz component	HD_{R2}	—	—	−25	dB	V_1=170mV$_{PP}$, 4.286MHz	Fig.1
Output switch voltage gain	G_{RS}	−1	0	1	dB	V_{30}=0.3V$_{PP}$, 627kHz	Fig.1
Output switch frequency characteristic	f_{RS}	−1	0	1	dB	V_{30}=0.3V$_{PP}$, 5MHz / 100kHz	Fig.1
Output switch crosstalk 1	CT_{R1}	—	−60	—	dB	V_{18}=25mV$_{PP}$, 1.0715MHz	Fig.1
Output switch crosstalk 2	CT_{R2}	—	−60	—	dB	V_{30}=0.3V$_{PP}$, 627kHz	Fig.1
〈PB system〉							
PB output amplitude	V_{PB}	202.5	270.0	337.5	mV$_{PP}$	Cyan level (cyan frequency)	Fig.1
Unwanted spectrum rejection							
3MHz component	HD_{P3}	—	—	−35	dB	V_{18}=25mV$_{PP}$, 1.0715MHz	Fig.1
2MHz component	HD_{P2}	—	—	−35	dB	V_{18}=25mV$_{PP}$, 1.0715MHz	Fig.1
1MHz component	HD_{P1}	—	—	−35	dB	V_{18}=25mV$_{PP}$, 1.0715MHz	Fig.1
Output switch voltage gain 1	G_{P1}	5	6	7	dB	V_8=0.3V$_{PP}$, 4.3MHz	Fig.1
Output switch frequency characteristic 1	f_{P1}	−1	0	1	dB	V_8=0.3V$_{PP}$, 5MHz / 100kHz	Fig.1
Output switch crosstalk 1	CT_{P1}	—	−60	—	dB	V_8=0.3V$_{PP}$, 4.3MHz	Fig.1
Output switch voltage gain 2	G_{P2}	−1	0	1	dB	V_{14}=0.3V$_{PP}$, 4.43MHz	Fig.1
Output switch frequency characteristic 2	f_{P2}	−1	0	1	dB	V_{14}=0.3V$_{PP}$, 5MHz / 100kHz	Fig.1
Output switch crosstalk 2	CT_{P2}	—	−60	—	dB	V_{14}=0.3V$_{PP}$, 4.43MHz	Fig.1
RECIN crosstalk	CT_{RIN}	—	−40	−30	dB	V_1=0.5V$_{PP}$, 4.286MHz	Fig.1
Control system							
"H" level voltage	V_H	2.5	—	—	V	14, 17, 19, 21, 30 pin (13,18,21,23,35pin) *	Fig.1
"L" level voltage	V_L	—	—	1.5	V	14, 17, 19, 21, 30 pin (13,18,21,23,35pin) *	Fig.1

* BA7207AK pin numbers are given in brackets.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
〈Filter block〉							
1.1MHz BPF characteristic							
1.1MHz voltage gain	G_{F11}	−2.8	0.7	4.2	dB	V_{18}=25mV$_{P-P}$, 1.0715MHz	Fig.1
0.5MHz voltage gain	G_{F12}	−6.5	−3.0	0.5	dB	V_{18}=25mV$_{P-P}$, 0.5MHz	Fig.1
3.2MHz voltage gain	G_{F13}	−	−35.0	−26.0	dB	V_{18}=25mV$_{P-P}$, 3.2145MHz	Fig.1
4.3MHz BPF-A characteristic							
4.3MHz voltage gain	G_{F31}	−11.3	−7.8	−4.3	dB	V_1=500mV$_{P-P}$, 4.286MHz	Fig.1
3.2MHz voltage gain	G_{F32}	−16.1	−12.6	−9.1	dB	V_1=500mV$_{P-P}$, 3.2MHz	Fig.1
5.5MHz voltage gain	G_{F33}	−14.0	−10.5	−7.0	dB	V_1=500mV$_{P-P}$, 5.5MHz	Fig.1
REC BELL + 4.3MHz BPF - A characteristic							
4.3MHz voltage gain	G_{RB1}	−0.7	2.8	6.3	dB	V_1=170mV$_{P-P}$, 4.286MHz	Fig.1
4.1MHz voltage gain	G_{RB2}	−7.0	−3.5	0	dB	V_1=170mV$_{P-P}$, 4.1MHz	Fig.1
4.5MHz voltage gain	G_{RB3}	−7.2	−3.7	−0.2	dB	V_1=170mV$_{P-P}$, 4.5MHz	Fig.1
PB BELL + 4.3MHz BPF - A characteristic							
4.3MHz voltage gain	G_{PB1}	−20.9	−17.4	−13.9	dB	V_1=800mV$_{P-P}$, 4.286MHz	Fig.1
4.1MHz voltage gain	G_{PB2}	−16.2	−12.7	−9.2	dB	V_1=800mV$_{P-P}$, 4.1MHz	Fig.1
4.5MHz voltage gain	G_{PB3}	−15.3	−11.8	−8.3	dB	V_1=800mV$_{P-P}$, 4.5MHz	Fig.1
REC EQ +1.1MHz BPF characteristic							
1.1MHz voltage gain	G_{RE1}	−4.0	−0.5	3.0	dB	V_{18}=95mV$_{P-P}$, 1.0715MHz	Fig.1
1.0MHz voltage gain	G_{RE2}	4.1	7.6	11.1	dB	V_{18}=95mV$_{P-P}$, 1.0MHz	Fig.1
1.2MHz voltage gain	G_{RE3}	6.7	10.2	13.7	dB	V_{18}=95mV$_{P-P}$, 1.2MHz	Fig.1
PB EQ +1.1MHz BPF characteristic							
1.1MHz voltage gain	G_{PE1}	2.5	6.0	9.5	dB	V_{18}=25mV$_{P-P}$, 1.0715MHz	Fig.1
1.0MHz voltage gain	G_{PE2}	−5.1	−1.6	1.9	dB	V_{18}=25mV$_{P-P}$, 1.0MHz	Fig.1
1.2MHz voltage gain	G_{PE3}	−8.9	−5.4	−1.9	dB	V_{18}=25mV$_{P-P}$, 1.2MHz	Fig.1

●Guaranteed design items (Unless otherwise specified Ta=25℃, Vcc=5.0V, delayed sync input)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
REC sync-gate phase	T_{DR}	1.3	2.4	3.5	μS	DIV (pin 14/pin 15), REC mode
PB sync-gate phase	T_{DP}	0.5	1.6	2.7	μS	MUL (pin 2/pin 42), PB mode
REC sync-gate amplitude	T_{WR}	4.9	5.2	5.5	μS	DIV (pin 15/pin 14), REC mode
PB sync-gate amplitude	T_{WP}	6.1	6.4	6.7	μS	MUL (pin 2/pin 42), PB mode

The pin numbers in brackets are for the BA7207AS and the BA7207AK respectively.

●Reference design data

(Unless otherwise specified Ta=25℃, Vcc=5.0V, f0 (REC BELL)=4.286MHz, f0 (PB EQ)=1.0715MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
〈1.1MHzBPF〉						
1.1MHz gain	G_{F11}	—	1.0	—	dB	V_{IN}=0.3V_{P-P}, 1.0715MHz
0.5MHz suppression ratio	G_{F12}	—	−4.0	—	dB	V_{IN}=0.3V_{P-P}, 0.5MHz
3.2MHz suppression ratio	G_{F13}	—	−30.0	—	dB	V_{IN}=0.3V_{P-P}, 3.2145MHz
Groupe delay time	D_{F1}	370	420	470	nS	V_{IN}=0.3V_{P-P}, 1.0715MHz
〈2.2MHzBPF〉						
2.2MHz gain	G_{F21}	—	−6.0	—	dB	V_{IN}=0.3V_{P-P}, 2.143MHz
1.1MHz suppression ratio	G_{F22}	—	−25.0	—	dB	V_{IN}=0.3V_{P-P}, 1.0715MHz
3.2MHz suppression ratio	G_{F23}	—	−25.0	—	dB	V_{IN}=0.3V_{P-P}, 3.2145MHz
Groupe delay time	D_{F2}	180	230	280	nS	V_{IN}=0.3V_{P-P}, 2.143MHz
〈4.3MHz BPF - A〉						
4.3MHz gain	G_{F31}	—	7.0	—	dB	V_{IN}=0.1V_{P-P}, 4.286MHz
3.2MHz suppression ratio	G_{F32}	—	−3.0	—	dB	V_{IN}=0.1V_{P-P}, 3.2MHz
5.5MHz suppression ratio	G_{F33}	—	−3.0	—	dB	V_{IN}=0.1V_{P-P}, 5.5MHz
Groupe delay time	D_{F3}	160	210	260	nS	V_{IN}=0.1V_{P-P}, 4.286MHz
〈4.3MHz BPF - B〉						
4.3MHz gain	G_{F41}	—	9.0	—	dB	V_{IN}=0.1V_{P-P}, 4.286MHz
3.5MHz suppression ratio	G_{F42}	—	−3.0	—	dB	V_{IN}=0.1V_{P-P}, 3.5MHz
5.2MHz suppression ratio	G_{F43}	—	−3.0	—	dB	V_{IN}=0.1V_{P-P}, 5.2MHz
Groupe delay time	D_{F4}	250	300	350	nS	V_{IN}=0.1V_{P-P}, 4.286MHz
〈REC BELL〉						
4.3MHz gain	G_{RB1}	—	19.5	—	dB	V_{IN}=0.3V_{P-P}, 4.286MHz
4.1MHz suppression ratio	G_{RB2}	—	−5.0	—	dB	V_{IN}=0.3V_{P-P}, 4.1MHz
4.5MHz suppression ratio	G_{RB3}	—	−5.5	—	dB	V_{IN}=0.3V_{P-P}, 4.5MHz
〈PB BELL〉						
4.3MHz gain	G_{PB1}	—	−19.5	—	dB	V_{IN}=0.3V_{P-P}, 4.286MHz
4.1MHz gain	G_{PB2}	—	5.0	—	dB	V_{IN}=0.3V_{P-P}, 4.1MHz
4.5MHz gain	G_{PB3}	—	5.5	—	dB	V_{IN}=0.3V_{P-P}, 4.5MHz
Center frequency ratio	df_{OB}	−1	0	1	%	$df_{OB}=(f_{O(PB)}-f_{O(REC)})\ /\ f_{O(REC)}$
〈PB EQ〉						
1.1MHz gain	G_{RE1}	—	19.5	—	dB	V_{IN}=0.3V_{P-P}, 1.0715MHz
1.0MHz suppression ratio	G_{RE2}	—	−8.0	—	dB	V_{IN}=0.3V_{P-P}, 1.0MHz
1.2MHz suppression ratio	G_{RE3}	—	−11.0	—	dB	V_{IN}=0.3V_{P-P}, 1.2MHz
〈REC EQ〉						
1.1MHz gain	G_{PE1}	—	−19.5	—	dB	V_{IN}=0.3V_{P-P}, 1.0715MHz
1.0MHz gain	G_{PE2}	—	8.0	—	dB	V_{IN}=0.3V_{P-P}, 1.0MHz
1.2MHz gain	G_{PE3}	—	11.0	—	dB	V_{IN}=0.3V_{P-P}, 1.2MHz
Center frequency ratio	df_{OE}	−1	0	1	%	$df_{OE}=(f_{O(REC)}-f_{O(PB)})\ /\ f_{O(PB)}$

●Measurement circuit

BA7207AS (SDIP32)

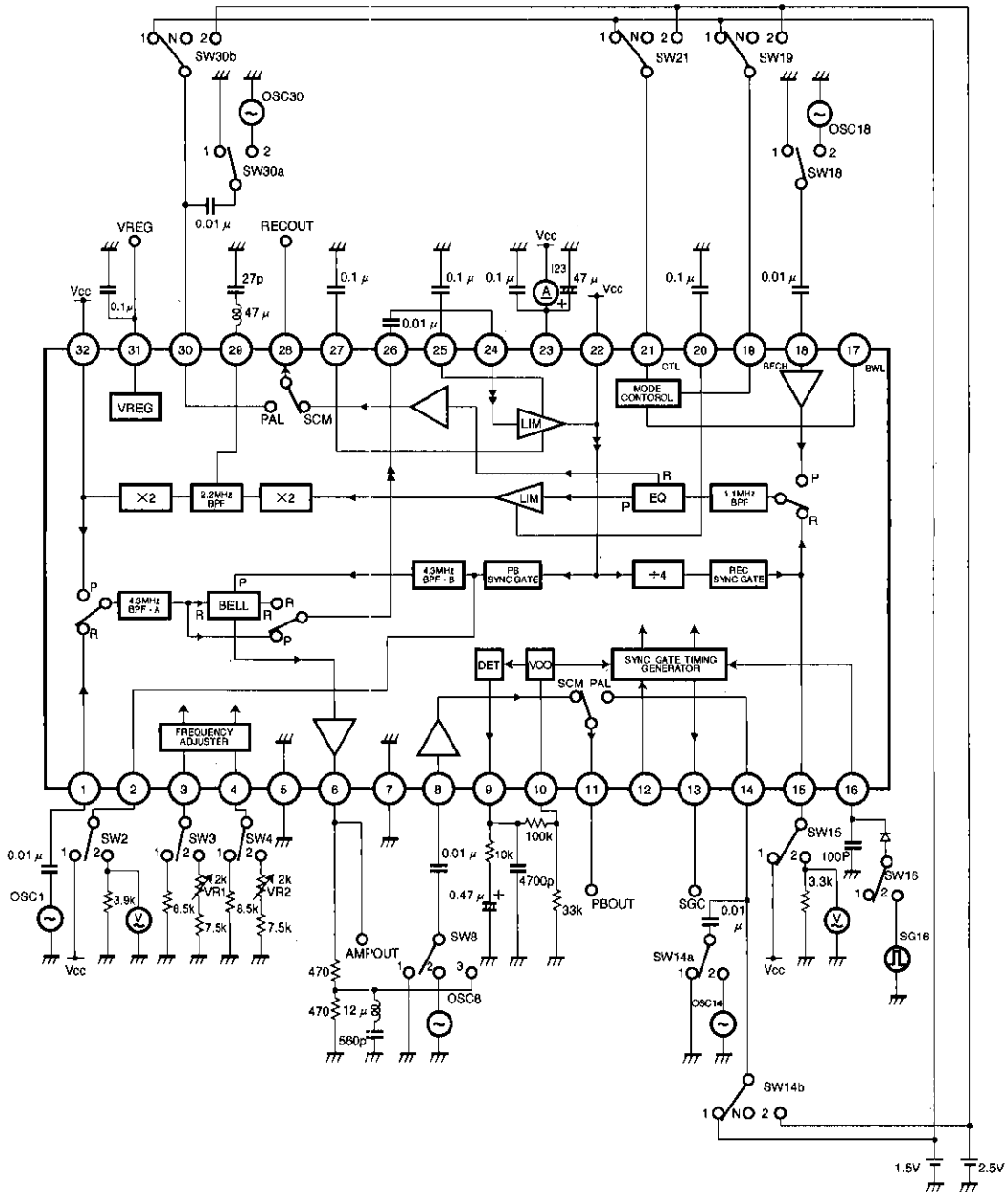


Fig.1

BA7207AK (QFP44)

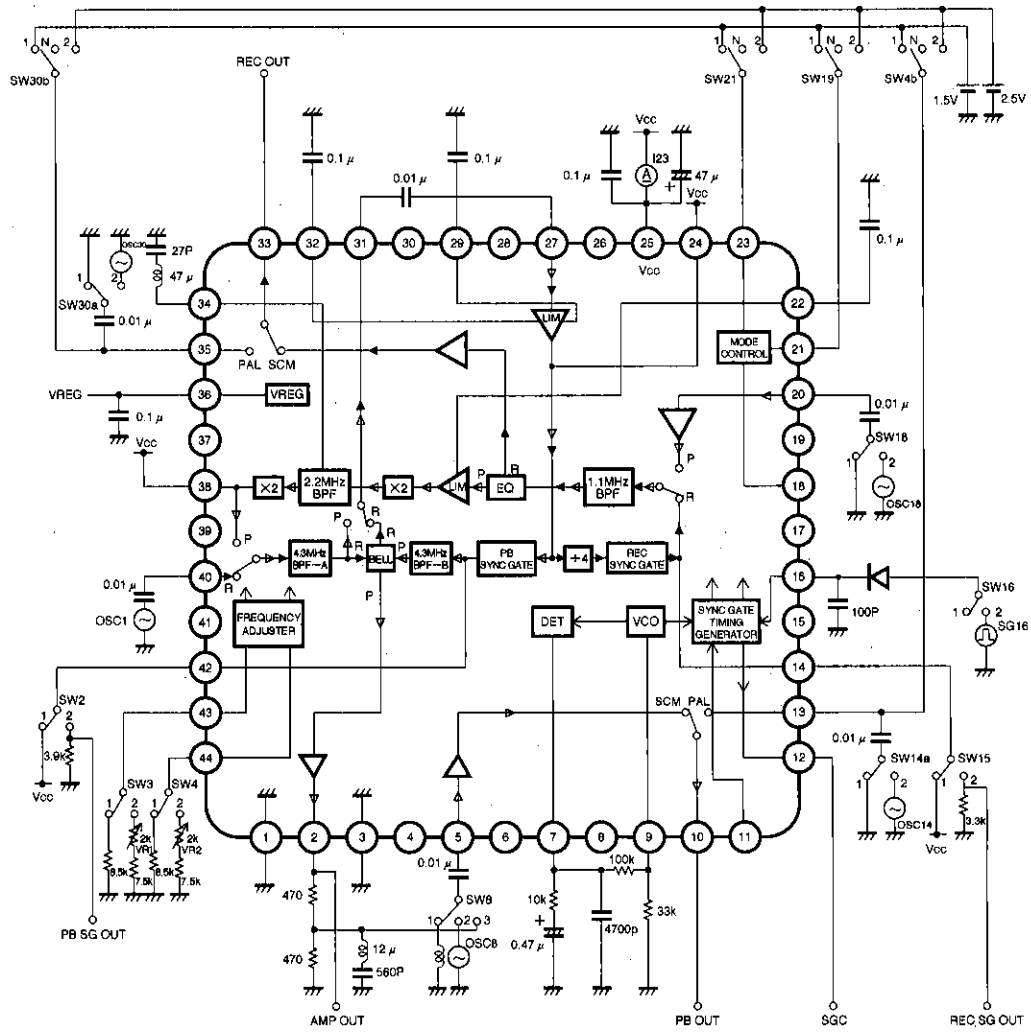


Fig.2

●Circuit operation

Recording system (REC)

The input to REC IN is passed through the 4.3MHz BPF–A to remove unwanted frequency components, and is flattened by REC BELL which has an anti–bell characteristic. The flattened signal is wave–shaped by the limiter amplifier, and processed by the divide–by–four and sync gate circuits. Finally, unwanted frequency components are removed by the 1.1MHz BPF and the REC EQ prepares the signal for recording playback and the signal is output on REC OUT. Refer to Fig. 3.

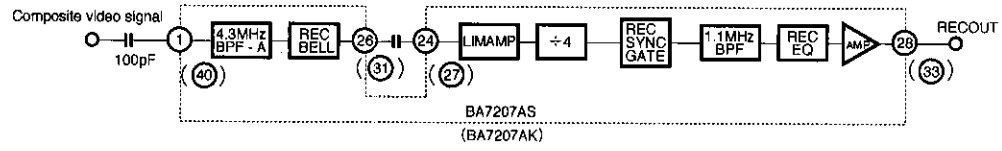


Fig.3

Playback system (PB)

The input to PB IN is passed through the 1.1MHz BPF to remove unwanted frequency components, and is flattened by the PB EQ circuit. The amplitude of the flattened signal fixed by the 1st–stage limiter amplifier, and the frequency is multiplied by four by the multiplier circuit. Unwanted frequency components generated by the multiplier circuit are removed by the 2.2MHz BPF and 4.3MHz BPF–A. The signal is wave–shaped by the limiter amplifier, and has gate applied to it by the sync gate circuit then is passed through the 4.3MHz BPF–B to remove unwanted frequency components. The PB BELL circuit restores the original bell characteristic and the signal is output on PB OUT. Refer to Fig. 4.

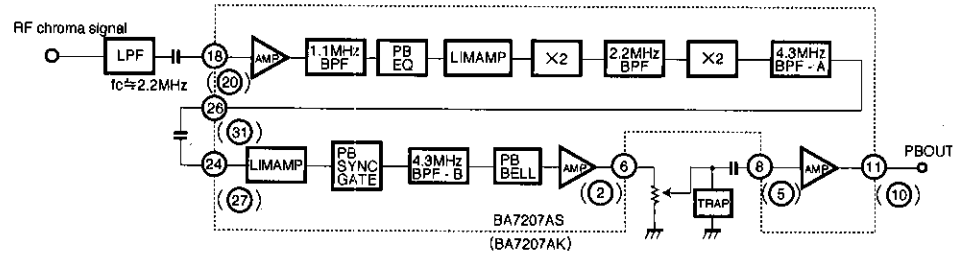


Fig.4

Sync gate timing circuit

REC and PB SYNC gate operation is as follows. The gate closes closes in synchronous with the SYNC IN input pulse during the synchronous signal pulse (SYNC) horizontal scan interval (64 μS period). During vertical retrace (32 μS period), the input pulse period becomes shorter than the horizontal scan interval. This is detected by the built–in vertical synchronous detector circuit which closes the gate. Refer to Fig. 5.

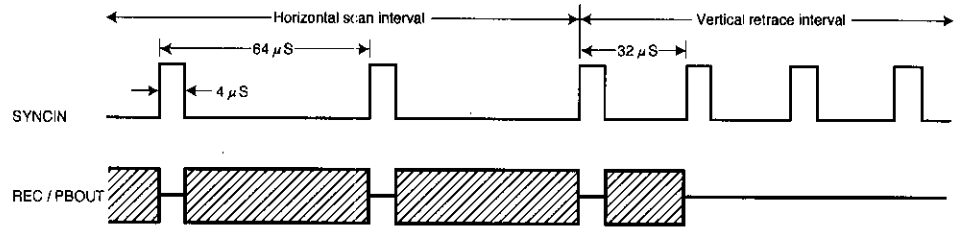
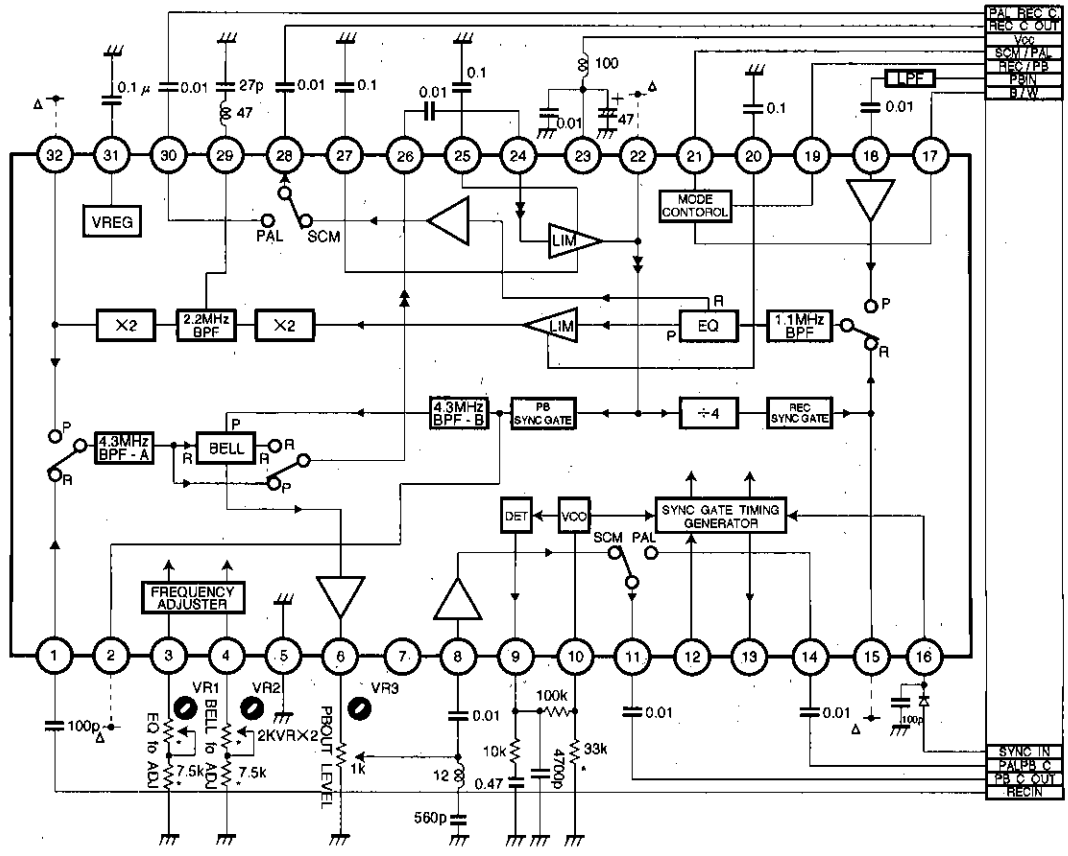


Fig.5

●Application example

BA7207AS (SDIP32)

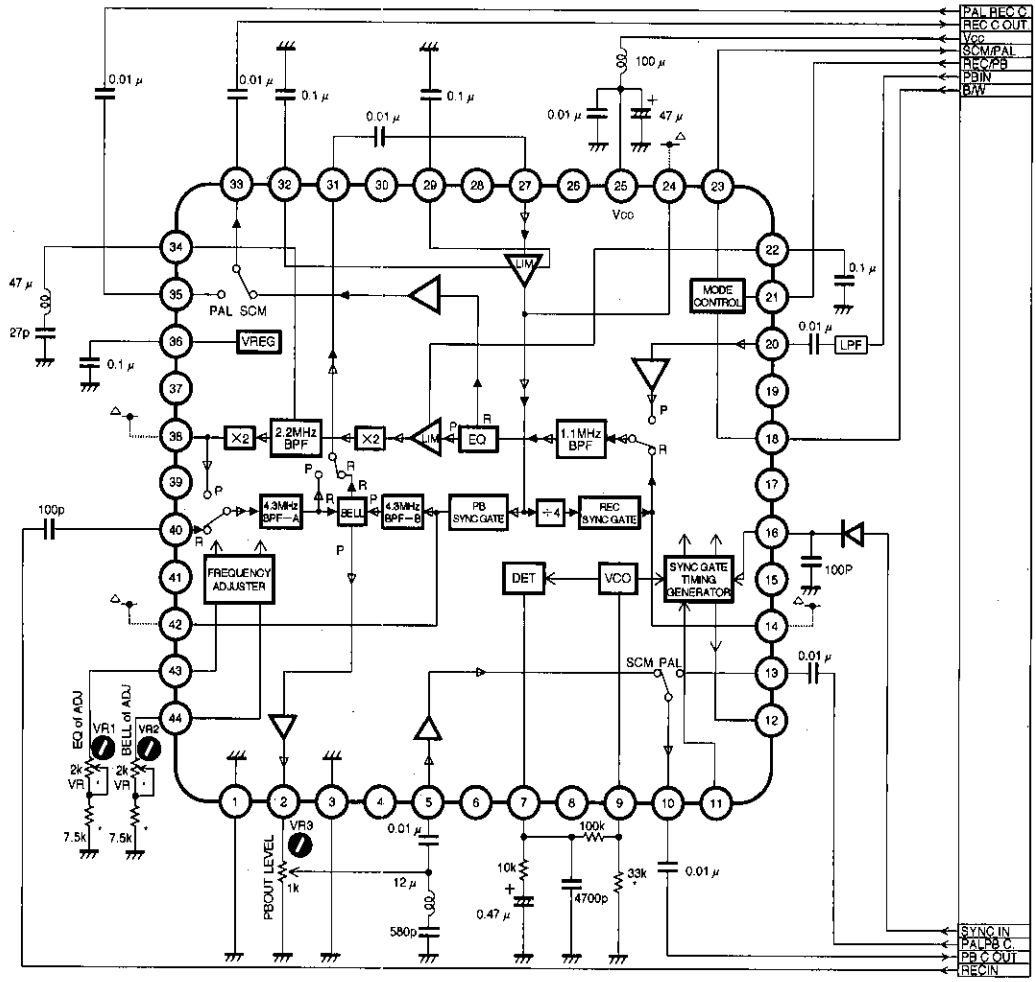


* To cancel the temperature characteristic of the ID, the resistors marked with asterisks should be of the metal film,and have a temperature coefficient ±100mp/℃.

△:Test pin.connect to Vcc if unused.

The 100pF capacitor connected to pin 16 is intended to reduce temperature disper of the gate phase.It should have a static capacitance tolerance of ±10% or lc and a temperature coefficient of ±30ppm(-55℃ to +125℃)A(CG).

Fig.6



* To cancel the temperature characteristic of the ID, the resistors marked with asterisks should be of the metal film,and have a temperature coefficient ±100mp/℃.

△:Test pin.connect to Vcc if unused.

The 100pF capacitor connected to pin 16 is intended to reduce temperature disper of the gate phase.It should have a static capacitance tolerance of ±10% or lc and a temperature coefficient of±30ppm(-55℃ to +125℃)A(CG).

Fig.7

●Control pin logic

	Pin	Low	High (Open)
REC/PB setting switch	RECH (19pin/21pin)	PB	REC
Output select switch	CTL (21pin/23pin)	PAL	SECAM
Chroma killer switch	BWL (17pin/18pin)	Chroma killer	NORMAL

(BA7207AS/BA7207AK)

●Operation notes

1. Equalizer fo adjustment

Set to PB mode and input a 25mVP-P, 1.0715MHz sine wave to PBIN. Adjust the variable resistor connected between FADJ1 and GND to maximize the REC OUT output. This adjustment also adjusts the 1.1MHz and 2.2MHz band-pass filters. The value of the variable resistor must be at least 2kΩ. If it is less than this, adjustment may not be possible.

2. Bell filter fo adjustment

Set to REC mode and input a 170mVP-P, 4.286MHz sine wave to RECIN. Adjust the variable resistor connected between FADJ2 and GND to maximize the AMP OUT output. This adjustment also adjusts the 4.3MHz and 4.3MHz A and B band-pass filters. The value of the variable resistor must be at least 2kΩ. If it is less than this, adjustment may not be possible.

3. Test pins

The MUL, DIV, LAO and 4XO pins are test terminals. By connecting these pins to GND via a 3.6kΩ resistor, it is possible to monitor there waveforms. When unused, connect these pins to Vcc to prevent interference.

4. REC/PB input levels

The frequency characteristics of the built-in filters can change. For this reason use the following input signal levels:

RECIN: 540mVP-P +/-6dB (cyan level)
PBIN: 75mVP-P +/-6dB (cyan level)

5. Capacitor connected to VREG

Use a ceramic with a static capacitance of 0.1 μF. The filter may not operate correctly with other capacitance values.

6. PBIN input

If there is a chroma component imposed on the FM brightness signal, use a low-pass filter (with an fc of about 2.2MHz) to remove the FM brightness signal component, and ensure that only the chroma component is input to PBIN.

7. RECIN input

In the case of composite video input, connect a 100pF capacitor to ensure that only the chroma component is input to RECIN.

8. Sync-gate phase adjustment

Perform fine adjustment of the sync-gate phase by applying a voltage to the SGADJ terminal, or using a resistor divider connected between Vcc and GND. The adjustment sensitivity is shown in Fig. 6.

SGADJ pin voltage when open: VSGADJ=2.5V
Input impedance Z=125kΩ

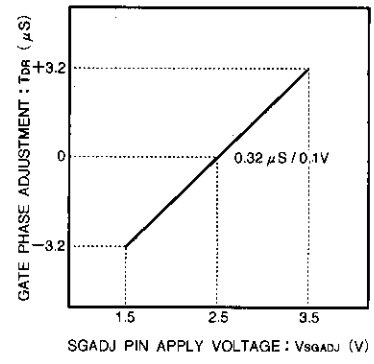


Fig.8 Sync-gate phase

●Electrical characteristic curves

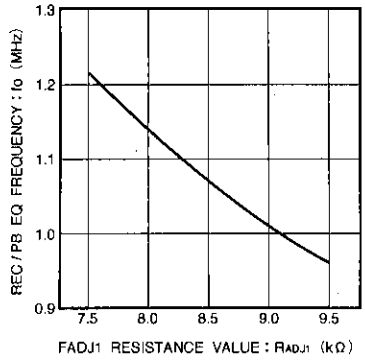


Fig.9 REC/PB EQ fo frequency adjustment range

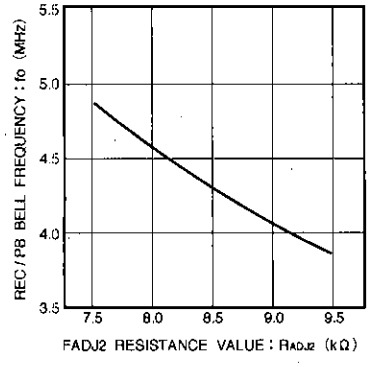


Fig.10 REC/PB BELL fo frequency adjustment range

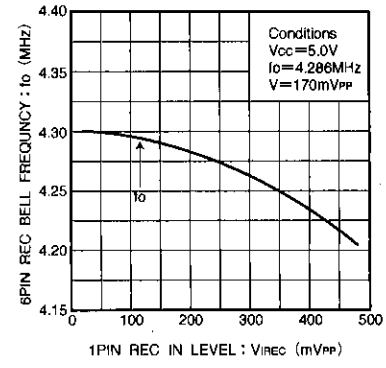


Fig.11 REC/BELL fo frequency variation

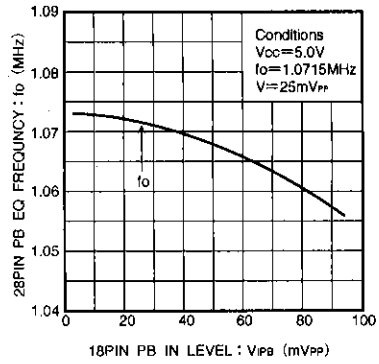


Fig.12 PB EQ fo frequency variation

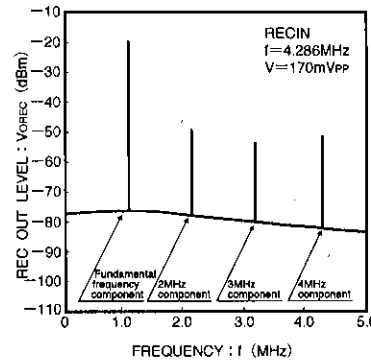


Fig.13 REC OUT spurious characteristics

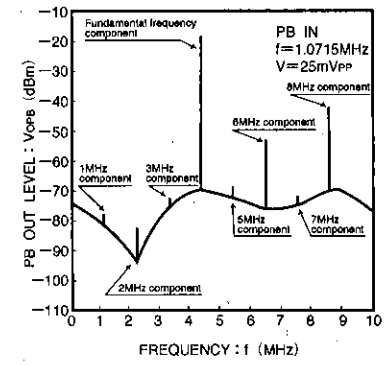
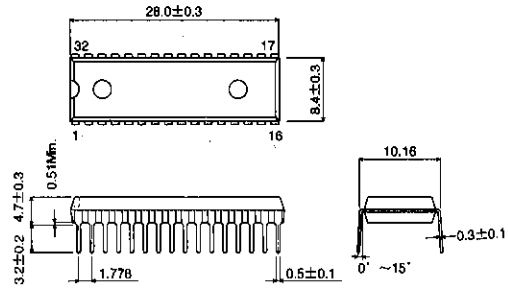


Fig.14 PB OUT spurious characteristics

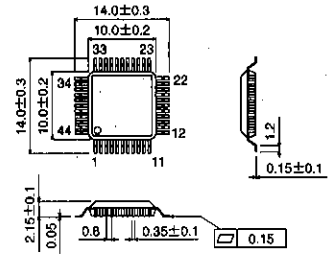
●External dimensions (Units: mm)

BA7207AS



SDIP32

BA7207AK



QFP44

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