SYNC separator IC with AFC

BA7071F

The BA7071F contains a video synchronization separation circuit, a vertical video synchronization separation circuit, a horizontal oscillation circuit, and a phase comparator. It separates and outputs the horizontal and vertical synchronization signals (HD and VD), and the composite synchronization signal (Sync-out) from input video or composite synchronization signals. The phase difference between HD and VD is guaranteed for both the rising and falling edges of VD.

●Applications

TV, VCR and camcorders

●Features

1) Built in AFC circuit.
2) HD and VD phase difference guaranteed.
3) Wide supply voltage range (3V to 7V).
4) Horizontal free-run frequency does not require adjustment.
5) Low external parts count.
6) SOP 8-pin package.

●Absolute maximum ratings (Ta=25℃)

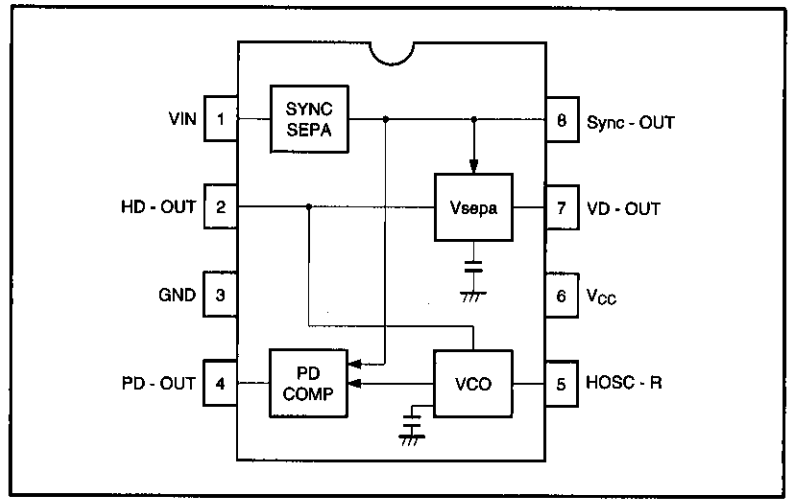
Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	8.0	V
Power dissipation	Pd	350*	mW
Operating temperature	Topr	−20~75	℃
Storage temperature	Tstg	−55~125	℃

* Reduced by 3.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	2.85	−	7.5	V

●Block diagram

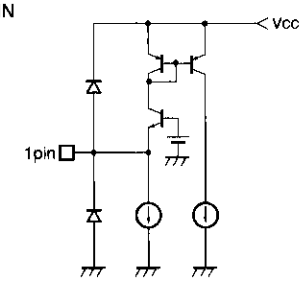


●Pin descriptions

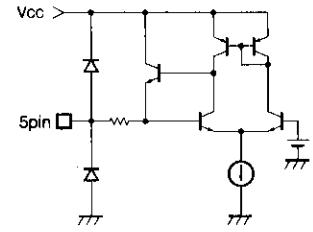
Pin No.	Pin name	Function
1	VIN	Video input
2	HD - OUT	HD output
3	GND	GND
4	PD - OUT	Phase comparator output
5	HOSC - R	Horizontal oscillator resistor
6	Vcc	Power supply (Vcc)
7	VD - OUT	VD output
8	Sync - OUT	Synchronization signal output (open collector)

●Input / output circuits

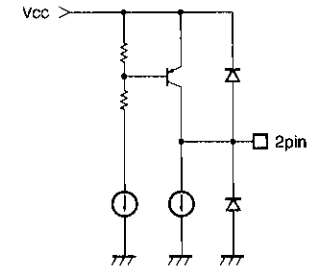
VIN



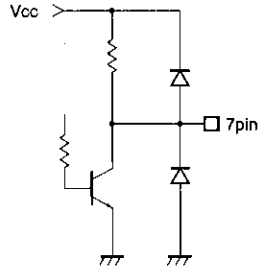
HOSC - R



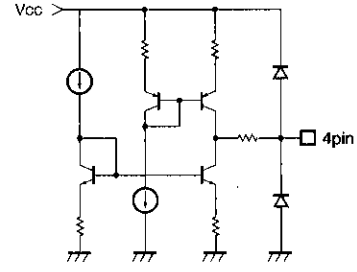
HD - OUT



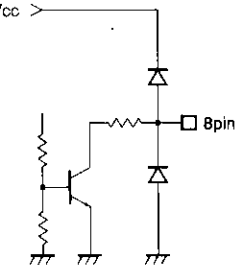
VD - OUT



PD - OUT



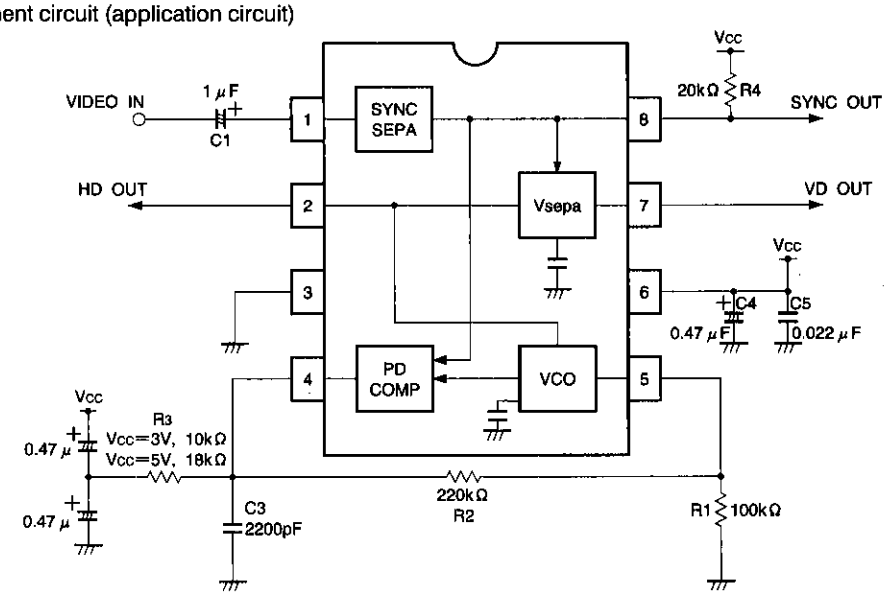
Sync - OUT



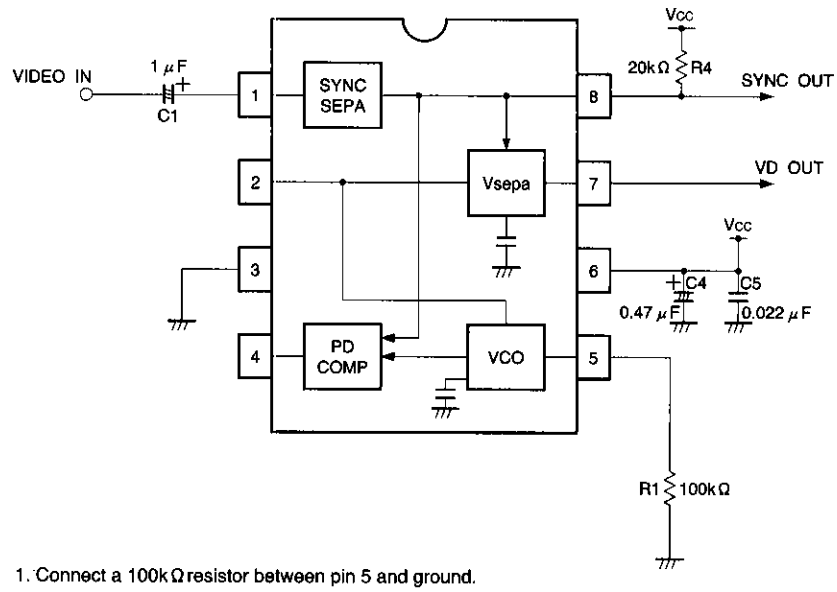
●Electrical characteristics (Unless otherwise specified Ta=25℃ and V_{CC}=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Quiescent current	I_Q	3.0	5.8	8.6	mA	Pin 8 open	Fig.1
Minimum SYNC separation level	Vsyn-min	—	0.08	0.15	V_{PP}	Pin 1 terminated with 75Ω resistor	Fig.1
Pulse voltage low	V_P-L	—	0.1	0.3	V	2, 7pin	Fig.1
Pulse voltage high	V_P-H	4.7	5.0	—	V	2, 7pin	Fig.1
(Horizontal) free-running frequency	f_{H0}	13.5	15.7	17.9	kHz	No input signal	Fig.1
Capture range	Δf_{CAP}	2.3	2.7	—	kHz		Fig.1
Lock-in phase	T_{HPH}	0.6	1.6	2.6	μs	2pin ↓ —1pin ↓	Fig.1
HD, VD phase difference 1	T_{HVD1}	19.0	24.0	29.0	μs	7pin ↓ —2pin ↑ (FLD1)	Fig.1
HD, VD phase difference 2	T_{HVD2}	19.0	24.0	29.0	μs	7pin ↑ —2pin ↑ (FLD1)	Fig.1
HD pulse width	T_{HD}	9.0	10.0	11.0	μs	2pin ↓↑	Fig.1
VD pulse width	T_{VD}	249	254	259	μs	7pin ↓↑	Fig.1
VIN, VD phase difference	T_{INVD}	41.0	48.0	55.0	μs	1pin ↓ —7pin ↓	Fig.1

●Measurement circuit (application circuit)



When SYNC SEPA output only is used. HD and VD unused.



1. Connect a 100kΩ resistor between pin 5 and ground.
   Leave pins 2, 4 and 7 open.
2. SYNC OUT (pin 8) has positive output.
3. The SYNC OUT (pin 8) output rise delay times in relation to the VIDEO IN(pin 1) input signal Sync fall are as follws:

   830 nc(reference value),when Vcc=5V
   830 nc(reference value),when Vcc=3V

4. The SYNC OUT (pin 8) output fall delay times in relation to the VIDEO IN(pin 1) input signal Sync rise are as follws:

   150 nc(reference value),when Vcc=5V
   220 nc(reference value),when Vcc=3V

Fig. 1 Electrical characteristics measurement circuit diagram and applied circuit diagram

●Circuit operation

1) Synchronization separation circuit

Detects the charging current to a externally-connected capacitor, and performs synchronization separation.

2) Horizontal oscillation circuit

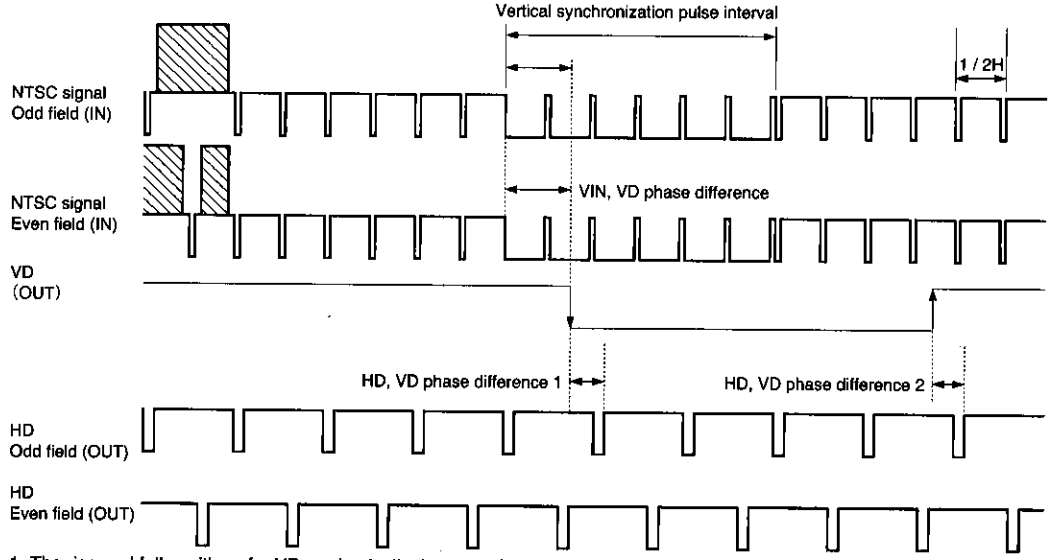
When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency is determined by external resistor R_1.

$$f_{H \cdot O} = \frac{1.57E6}{R_1} \text{ [kHz]}$$

3) Vertical synchronization separation circuit

When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

4) VIN, HD, and VD timing charts



1. The rise and fall positions for VD are basically the same for both odd and even fields.
2. HD shifts by 1/2H during the odd and even field interval.
3. Only the odd field is given for the specification.

Fig. 2 Timing chart

●External components

Resistor R_1 should have a tolerance of ±2%, and a temperature coefficient of 100ppm or lower.

●Electrical characteristic curves

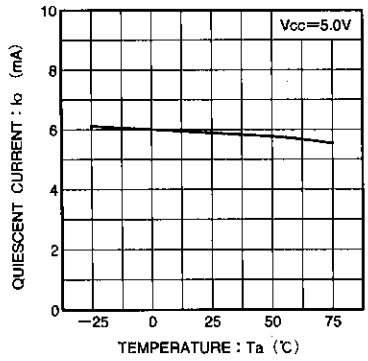


Fig. 3 Quiescent current vs. temperature

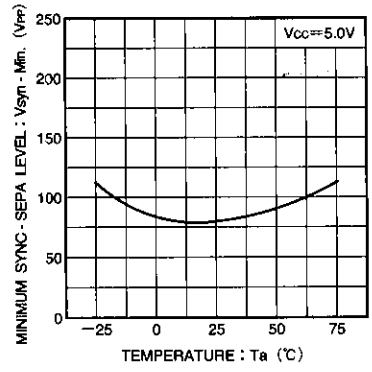


Fig. 4 Minimum synchronization separation level vs. temperature

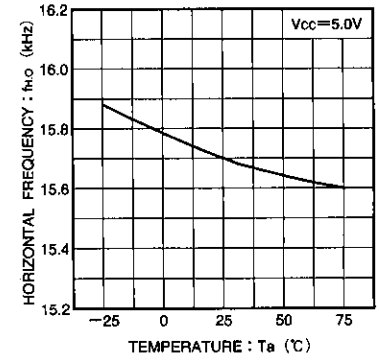


Fig. 5 Horizontal free-running frequency vs. temperature

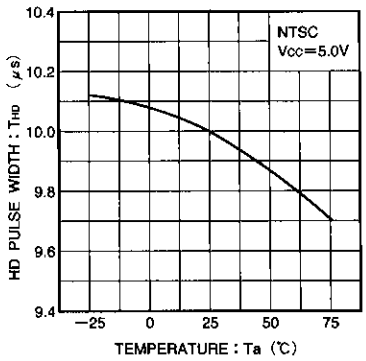


Fig. 6 HD pulse width vs. temperature

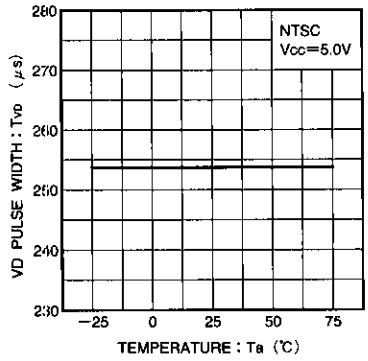


Fig. 7 VD pulse width vs. temperature

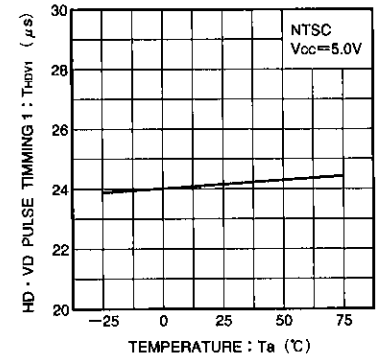


Fig. 8 HD, VD phase difference 1 vs. temperature

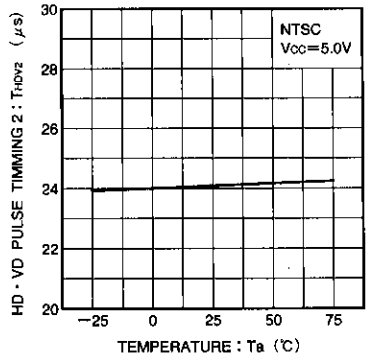
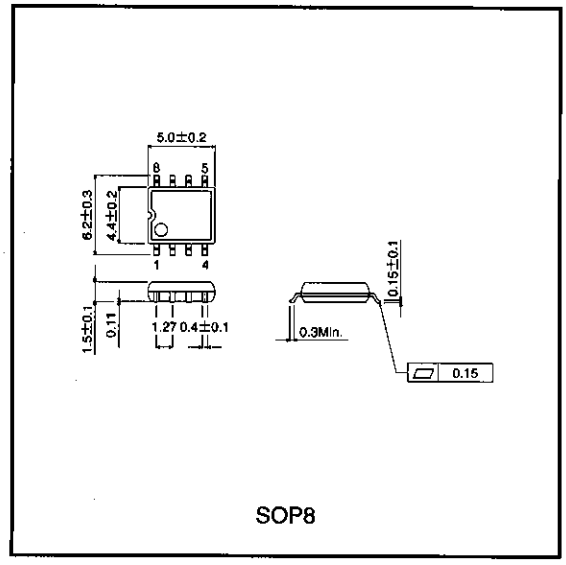


Fig. 9 HD, VD phase difference 2 vs. temperature

●External dimensions (Units: mm)



SOP8

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