SYNC separator IC with AFC

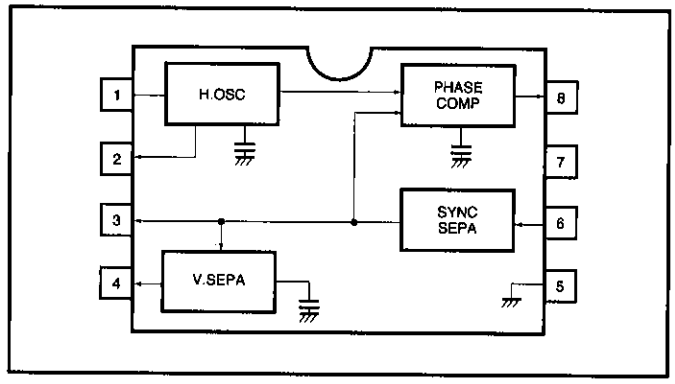
BA7062F

The BA7062F separates the synchronization signals from a video signal and outputs the horizontal and vertical synchronization signals (H_D and V_D), and the composite synchronization signal (Sync-out).
The H_D and V_D pulse widths are different.

●Applications
TV and VCR

●Features
1) Built-in AFC circuit.
2) Low power dissipation (approx. 21mW).
3) Low external parts count.
4) SOP 8-pin package.
5) Horizontal free-run frequency does not require adjustment.

●Block diagram



●Internal circuits

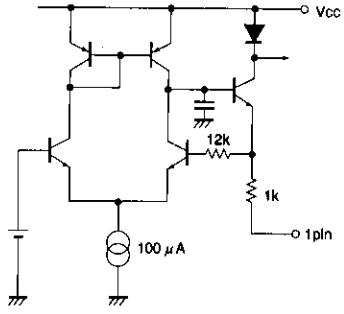


Fig. 1

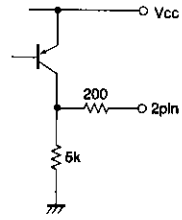


Fig. 2

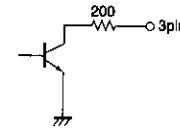


Fig. 3

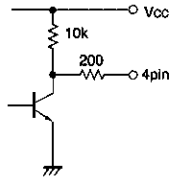


Fig. 4

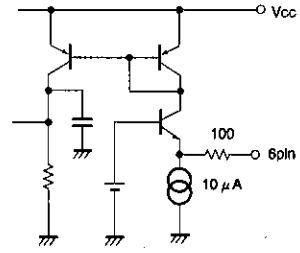


Fig. 5

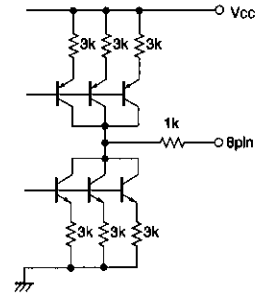


Fig. 6

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{CC\ Max.}$	8.0	V
Power dissipation	Pd	350 *	mW
Operating temperature	Topr	−20~75	℃
Storage temperature	Tstg	−55~125	℃

* When mounted on a 50mm × 50mm PCB, reduced by 3.5mW for each increase in Ta of 1℃ over 25℃.

●Pin descriptions

Pin No.	Function
1	Horizontal oscillator resistor
2	H_D output
3	SYNC output (open collector)
4	V_D output
5	GND
6	Video input
7	Power supply
8	Phase comparator output

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	4.5	—	5.5	V

●Electrical characteristics (Unless otherwise specified :Ta=25℃ and V_{CC}=5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Quiescent current	I_Q	2.0	4.1	6.2	mA	Pin 3 open	Fig.7
Minimum SYNC separation level	$V_{syn\text{-}Min.}$	—	0.08	0.15	$V_{P\text{-}P}$	Pin 6 terminated with 75Ω resistor	
Pulse voltage, Low	$V_{P\text{-}L}$	—	0.1	0.3	V	2, 4 pin	
Pulse voltage, High	$V_{P\text{-}H}$	4.7	4.9	—	V	2, 4 pin	
(Horizontal) free-running frequency	$f_{H\text{-}O}$	13.9	15.7	17.5	kHz	No input signal, I_1 = open	
Capture range	Δf_{CAP}	±2.1	±2.9	—	kHz		
Lock-in phase	T_{HPH}	−1.0	0	+1.0	μs	2pin ↓ −6pin ↓	
H_D pulse width	T_{HD}	10.5	11.5	12.5	μs	2pin ⊓	
V_D pulse width	T_{VD}	200	260	320	μs	4pin ⊓	

◎Not designed for radiation resistance.

●Measurement circuit

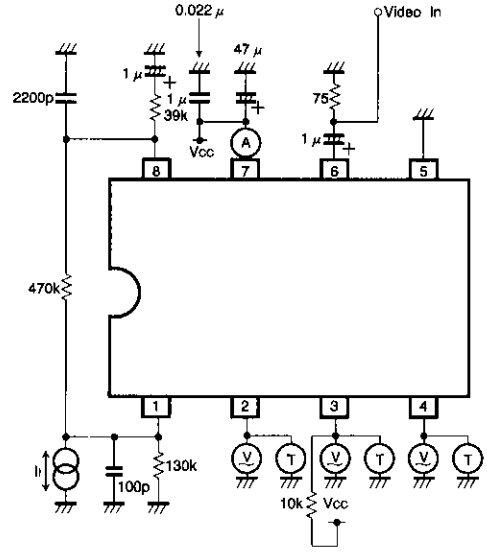


Fig. 7

●Electrical characteristic curves

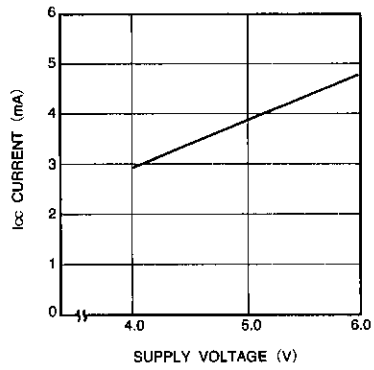


Fig. 8 Quiescent current vs. supply voltage

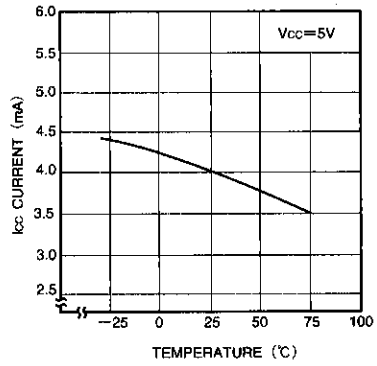


Fig. 9 Quiescent current vs. temperature

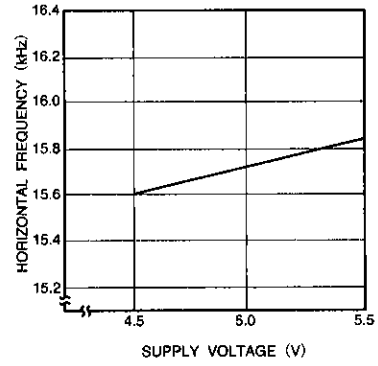


Fig. 10 Horizontal free-running frequency vs. supply voltage

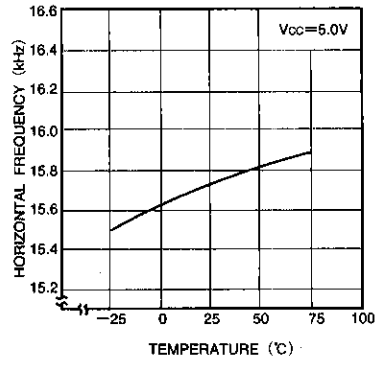


Fig. 11 Horizontal free-running frequency vs. temperature

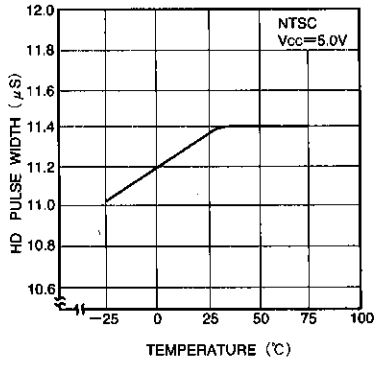


Fig. 12 H_D pulse width vs. temperature

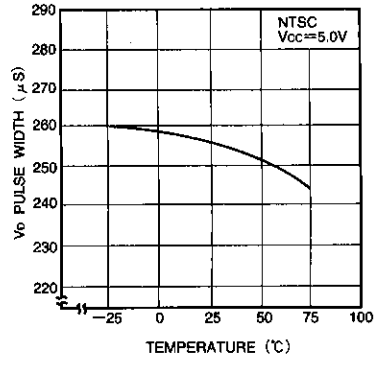


Fig. 13 V_D pulse width vs. temperature

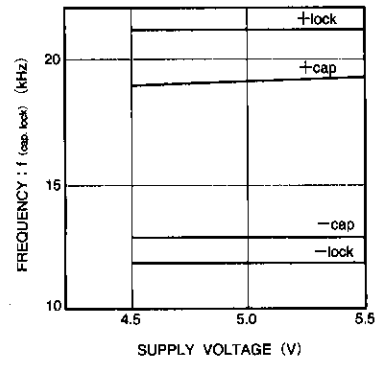


Fig. 14 Capture range/lock range vs. supply voltage

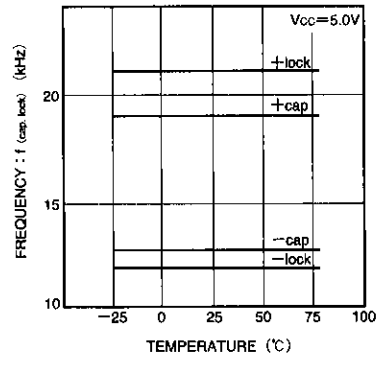


Fig. 15 Capture range/lock range vs. temperature

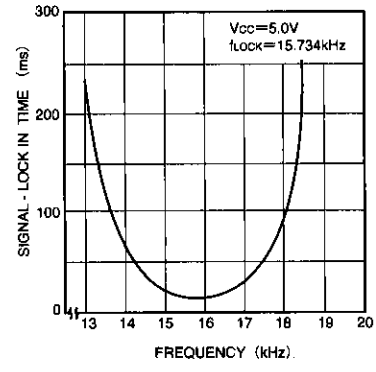


Fig. 16 Time from no signal to pull in

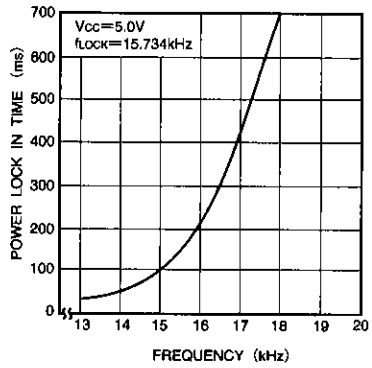


Fig. 17 Time from power on to pull in

●Circuit operation

(1) Synchronization separation circuit

Detects the charging current to a externally-connected capacitor, and performs synchronization separation.

(2) Horizontal oscillation circuit

When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency is determined by external resistor R_1.

$$f_{H\text{-}O} = \frac{2.05E6}{R_1} \quad [kHz]$$

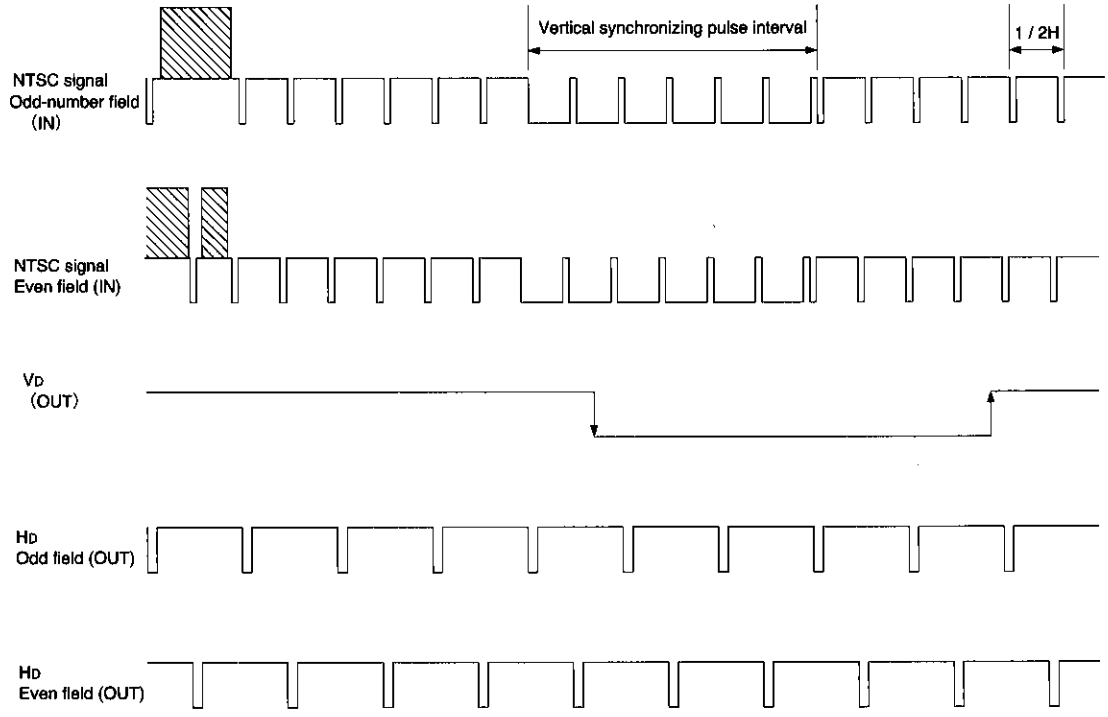
(3) Vertical synchronization separation circuit

When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

●Operation notes

- Make the ground line as thick as possible.
- Keep power supply noise to a minimum.

●V_{IN}, H_D, and V_D timing charts



1. The rise and fall positions for V_D are basically the same for both odd and even fields.
2. H_D shifts by 1/2H during the odd and even field interval.

●Application example

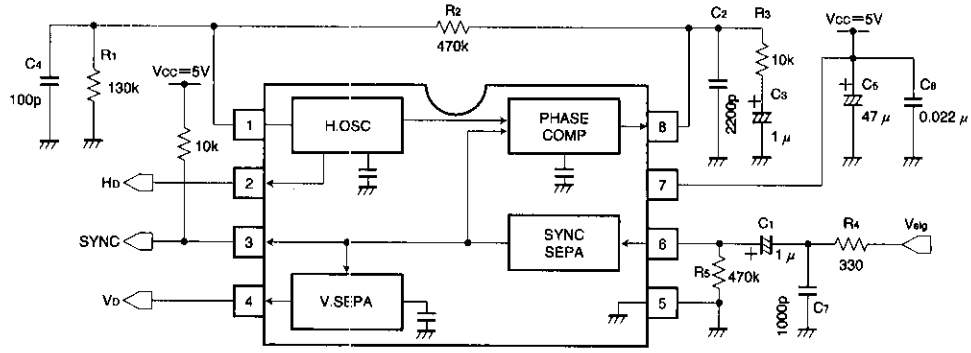


Fig. 18

· When SYNC SEPA output only is used. HD and VD unused.

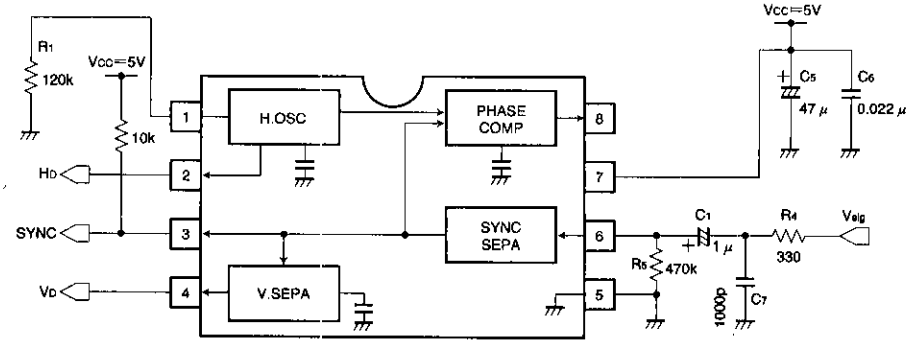


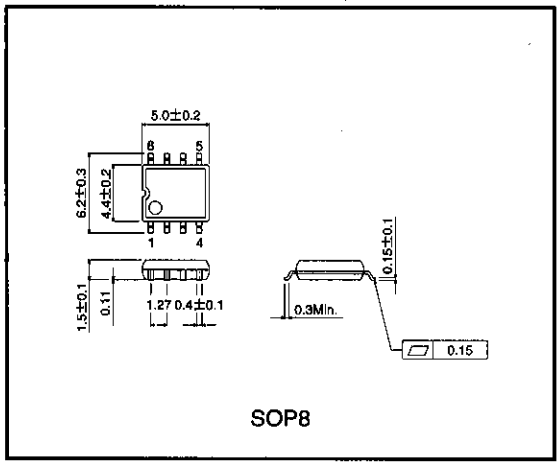
Fig. 19

1. Connect pin 1 to GND via a 120kΩ (approx.) resistor. Leave pins 2, 4 and 8 open.
2. SYNC output polarity (pin 3) is positive.
3. The delay time for rising edge of the SYNC output (pin 3) with respect to the falling edge of Sync for the Vsig input signal (pin 6) is 850ns (reference value).
4. The delay time for falling edge of the SYNC output (pin 3) with respect to the rising edge of Sync for the Vsig input signal (pin 6) is 450ns (reference value).

●External components

Resistor R_1 should have a tolerance of ±2%, and a temperature coefficient of 100ppm or lower.

●External dimensions (Units: mm)



SOP8

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