Features

- **Available in Gate Array or Embedded Array**
- **High-speed, 100 ps Gate Delay, 2-input NAND, FO = 2 (nominal)**
- **Up to 6.9 Million Used Gates and 976 Pins**
- **0.25µ Geometry in up to Five-level Metal**
- **System-level Integration Technology**
  - **Cores: ARM7TDMI™, ARM920T™, ARM946E-S™ and MIPS64™ 5Kf™ RISC Microprocessors; AVR® RISC Microcontroller; OakDSPCore™, Teak™ and PalmDSPCore™ Digital Signal Processors; 10/100 Ethernet MAC, USB, 1394, 1284, CAN and Other Assorted Processor Peripherals**
  - **Analog Functions: DACs, ADCs, OPAMPs, Comparators, PLLs and PORs**
  - **Soft Macro Memory: Gate Array**
    SRAM — ROM — DPSRAM — FIFO
  - **Hard Macro Memory: Embedded Array**
    SRAM — ROM — DPSRAM — FIFO — Stacked E^2 — Stacked Flash
  - **I/O Interfaces: CMOS, LVTTL, LVDS, PCI, USB; Output Currents up to 16 mA @2.5V; 2.5V Native I/O, 3.3V Tolerant/Compliant I/O, 5.0V Tolerant I/O**

ASIC

ATL25 Series

Description

The ATL25 Series ASIC family is fabricated on a 0.25µ CMOS process with up to five levels of metal. This family features arrays with up to 6.9 million routable gates and 976 pins. The high density and high pin count capabilities of the ATL25 family, coupled with the ability to add embedded microprocessor cores, DSP engines and memory on the same silicon, make the ATL25 series of ASICs an ideal choice for system-level integration.
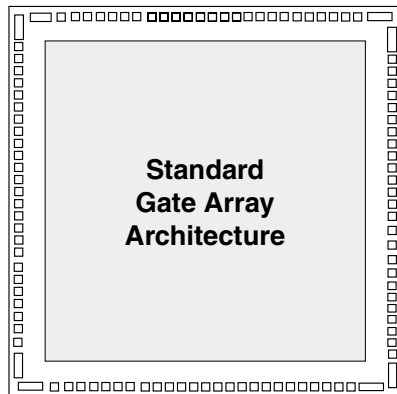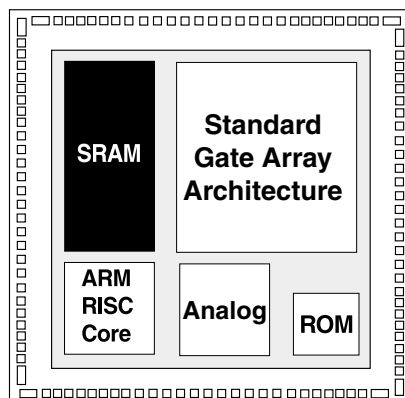
Figure 1. ATL25 Gate Array ASIC

Figure 2. ATL25 Embedded Array ASIC

Table 1. ATL25 Array Organization

Device Number	4LM Routable Gates[1]	5LM Routable Gates[1]	Available Routing Sites[2]	Max Pad Count	Max I/O Count	Gate Speed[3]
ATL25/44	9,535	10,727	15,892	44	36	100 ps
ATL25/68	30,096	33,858	50,161	68	60	100 ps
ATL25/84	50,410	56,712	84,018	84	76	100 ps
ATL25/100	75,472	84,906	125,788	100	92	100 ps
ATL25/120	106,278	120,449	188,940	120	112	100 ps
ATL25/132	131,670	149,226	234,080	132	124	100 ps
ATL25/144	159,778	181,081	284,050	144	136	100 ps
ATL25/160	200,998	227,797	357,330	160	152	100 ps
ATL25/184	270,663	306,751	481,179	184	176	100 ps
ATL25/208	329,281	376,321	627,203	208	200	100 ps
ATL25/228	401,010	458,298	763,830	228	220	100 ps
ATL25/256	512,398	585,598	975,998	256	248	100 ps
ATL25/304	733,635	838,440	1,397,400	304	296	100 ps
ATL25/352	925,815	1,068,248	1,899,108	352	344	100 ps
ATL25/388	1,133,594	1,307,994	2,325,323	388	380	100 ps
ATL25/432	1,417,125	1,635,145	2,906,925	432	424	100 ps
ATL25/484	1,651,406	1,926,640	3,669,792	484	476	100 ps
ATL25/540	2,069,052	2,413,894	4,597,895	540	532	100 ps
ATL25/600	2,567,790	2,995,755	5,706,200	600	592	100 ps
ATL25/700	3,520,954	4,107,780	7,824,344	700	692	100 ps
ATL25/800	4,231,979	5,001,430	10,259,344	800	792	100 ps
ATL25/900	5,378,257	6,356,122	13,038,200	900	892	100 ps
ATL25/976	5,765,320	6,918,384	15,374,188	976	968	100 ps

Notes: 1. One gate = NAND2
2. Routing site = 4 transistors
3. Nominal 2-input NAND gate FO = 2 at 2.5V

Design

Atmel supports several major software systems for design with complete cell libraries, as well as utilities for netlist verification, test vector verification and accurate delay simulations

**Table 2.** Design Systems Supported

System	Tools	Version
Cadence® Design Systems, Inc.	Opus™ – Schematic and Layout NC Verilog™ – Verilog Simulator Pearl™ – Static Path Verilog-XL™ – Verilog Simulator BuildGates™ – Synthesis (Ambit)	4.46 3.3-s008 4.3-s095 3.3-s006 4.0-p003
Mentor Graphics®	ModelSim® – Verilog and VHDL (VITAL) Simulator Leonardo Spectrum™ – Logic Synthesis	5.5e 2001.1d
Synopsys®	Design Compiler™ – Synthesis DFT Compiler – 1-Pass Test Synthesis BSD Compiler – Boundary Scan Synthesis TetraMax® – Automatic Test Pattern Generation PrimeTime™ – Static Path VCS™ – Verilog Simulator Floorplan Manager™	01.01-SP1 01.08-SP1 01.08-SP1 01.08 01.08-SP1 5.2 01.08-SP1
Novas Software, Inc.®	Debussy®	5.1
Silicon Perspective™	First Encounter®	v2001.2.3

Atmel's ASIC design flow is structured to allow the designer to consolidate the greatest number of system components onto the same silicon chip, using widely available third-party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage and process, and includes the effects of metal loading, interlevel capacitance, and edge rise and fall times. The design flow includes clock tree synthesis to customer-specified skew and latency goals. RC extraction is performed on the final design database and incorporated into the timing analysis.

The ASIC design flow, shown on page 4, provides a pictorial description of the typical interaction between Atmel's design staff and the customer. Atmel will deliver design kits to support the customer's synthesis, verification, floorplanning and scan insertion activities. Leading-edge tools from vendors such as Synopsys and Cadence are fully supported in our design flow. In the case of an embedded array design, Atmel will conduct a design review with the customer to define the partition of the embedded array ASIC and to define the location of the memory blocks and/or cores so an underlayer layout model can be created.

Following database acceptance, automated test pattern generation (ATPG) is performed, if required, on scan paths using Synopsys tools; the design is routed; and post-route RC data is extracted. After post-route verification and a final design review, the design is taped out for fabrication.

Table 3. Design Flow

Customer
Atmel
Joint

Rev. 2.2-03/02

ATL25 Series ASIC
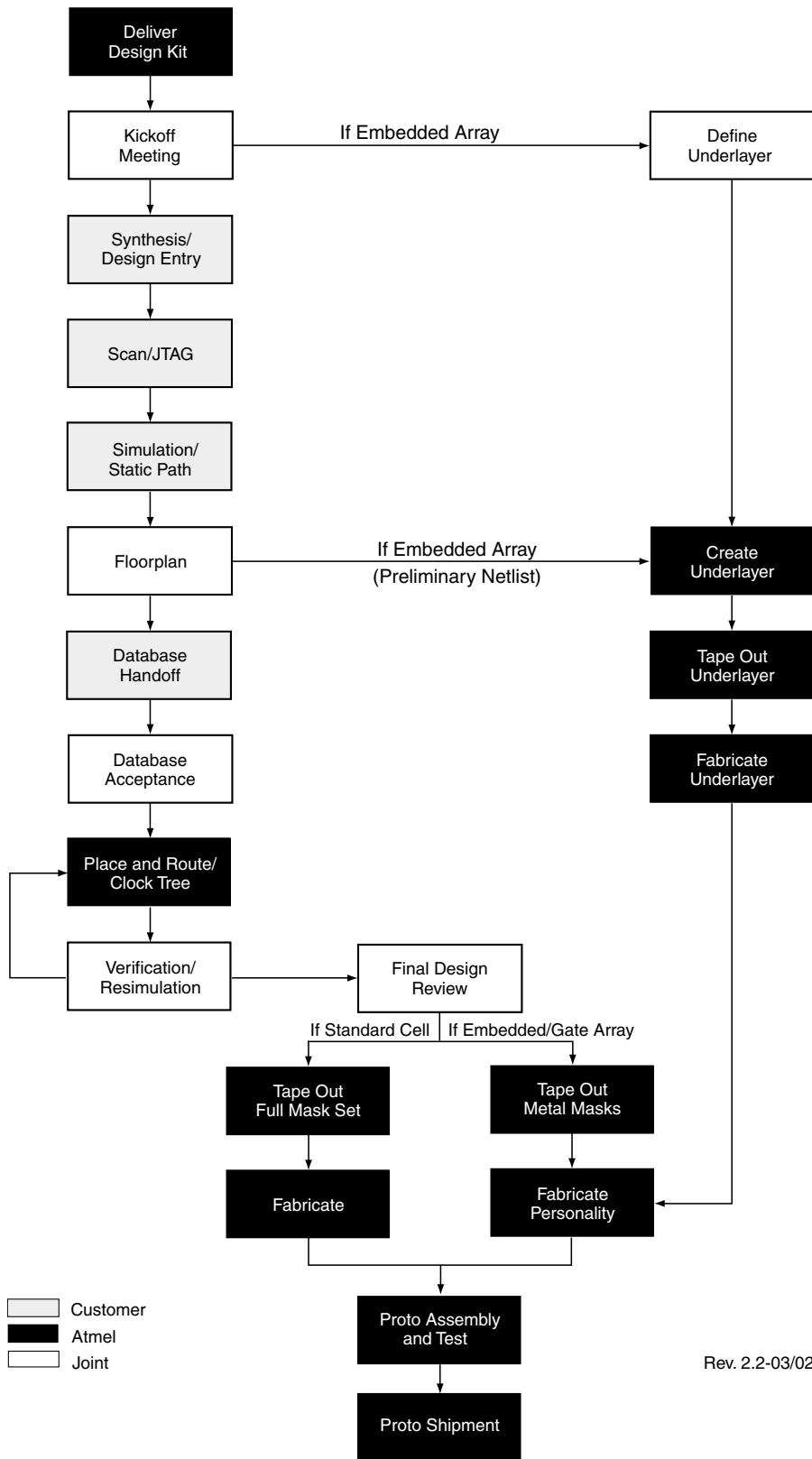
Pin Definition Requirements

The corner pads are reserved for power and ground only. All other pads are fully programmable as input, output, bidirectional, power, or ground. When implementing a design with 3.3V compliant buffers, an appropriate number of pad sites must be reserved for the V_{DD} 3 pins, which are used to distribute 3.3V power to the compliant buffers.

Design Options

Logic Synthesis

Atmel can accept RTL designs in Verilog or VHDL HDL formats. Atmel fully supports Synopsys for Verilog or VHDL simulation as well as synthesis. Of the two HDL formats, Verilog and VHDL, Atmel's preferred HDL format for ASIC design is Verilog.

ASIC Design Translation

Atmel has successfully translated existing designs from most major ASIC vendors into Atmel ASICs. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated as a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors into Atmel ASICs. There are four primary reasons to convert from an FPGA/PLD to an ASIC:

• Conversion of high-volume devices for a single or combined design is cost effective.
• Performance can often be optimized for speed or low power consumption.
• Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements.
• In situations where an FPGA/PLD was used for fast cycle time prototyping, an ASIC may provide a lower cost answer for long-term volume production.

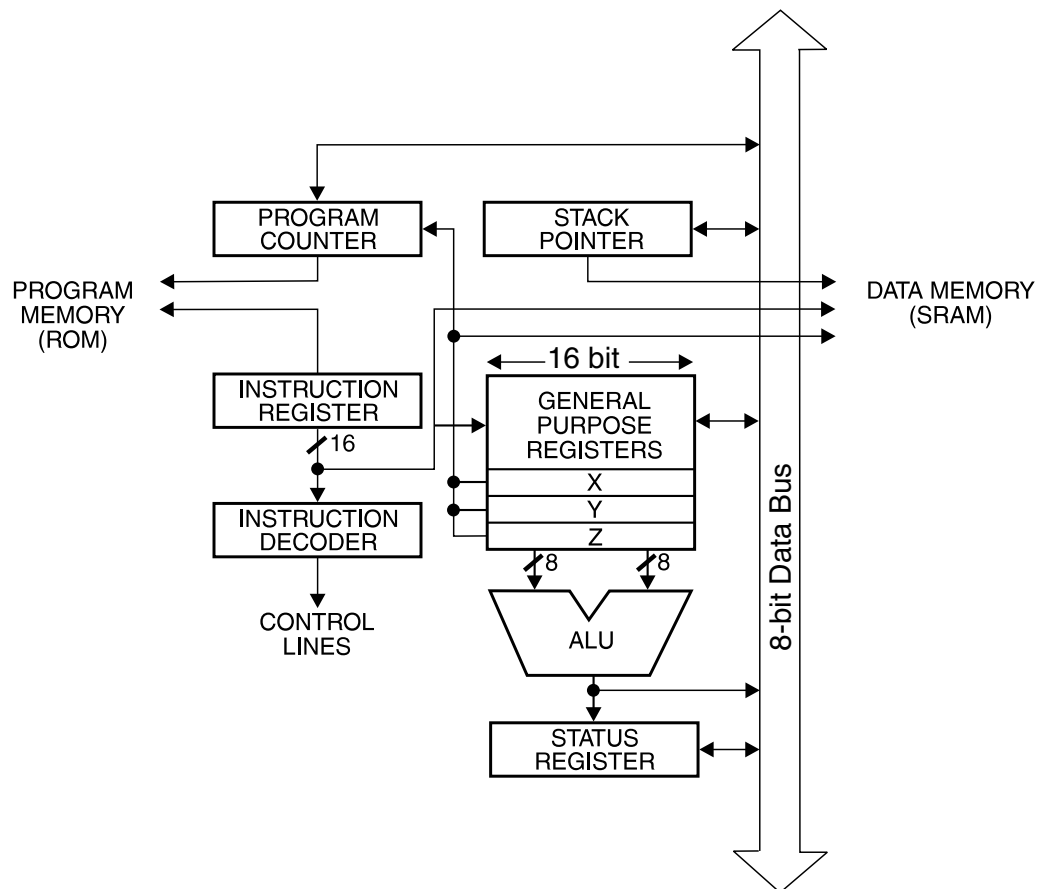# Macro Cores

AVR 8-bit RISC Microcontroller Core

The AVR RISC microcontroller is a true 8-bit RISC architecture, ideally suited for embedded control applications. The AVR is offered as a gate level, synthesizable macro core in the ATL25 family.

The AVR supports a powerful set of 120 instructions. The AVR prefetches an instruction during a prior instruction execution, enabling the execution of one instruction per clock cycle.

The Fast Access RISC register file consists of 32 general purpose working registers. These 32 registers eliminate the data transfer delay in the traditional program code intensive accumulator architectures.

The AVR can incorporate up to 64 x 16K program memory (ROM) and 64 x 8K data memory (SRAM). Among the peripheral options offered are: UART, 8-bit timer/counter, 16-bit timer/counter, programmable watchdog timer and SPI.

Figure 3. AVR 8-bit RISC Microcontroller Core

ARM7TDMI™ 32-bit RISC Microprocessor Core

The ARM7TDMI is a powerful 32-bit processor offered as a hard macro core in the ATL25 family.

The ARM7TDMI is a member of the Advanced RISC Machines (ARM) family of general purpose 32-bit microprocessors, which offer high performance with very low power consumption. Additionally, the ARM7T offers users a "thumb" mode (for higher code density using 16-bit instructions

The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micropro- grammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and an impressive real-time interrupt response from a small and cost- effective chip.

Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM memory interface has been designed to allow the performance potential to be real- ized without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals facilitate the exploitation of the fast local access modes offered by industry standard SRAMs.

The ARM7TDMI core interfaces to several optional peripheral macros. Among the peripheral options offered are real-time clock, peripheral data controller, USART, external bus interface, interrupt controller, timer counter and watchdog timer.

Figure 4. ARM7TDMI 32-bit RISC Microprocessor Core
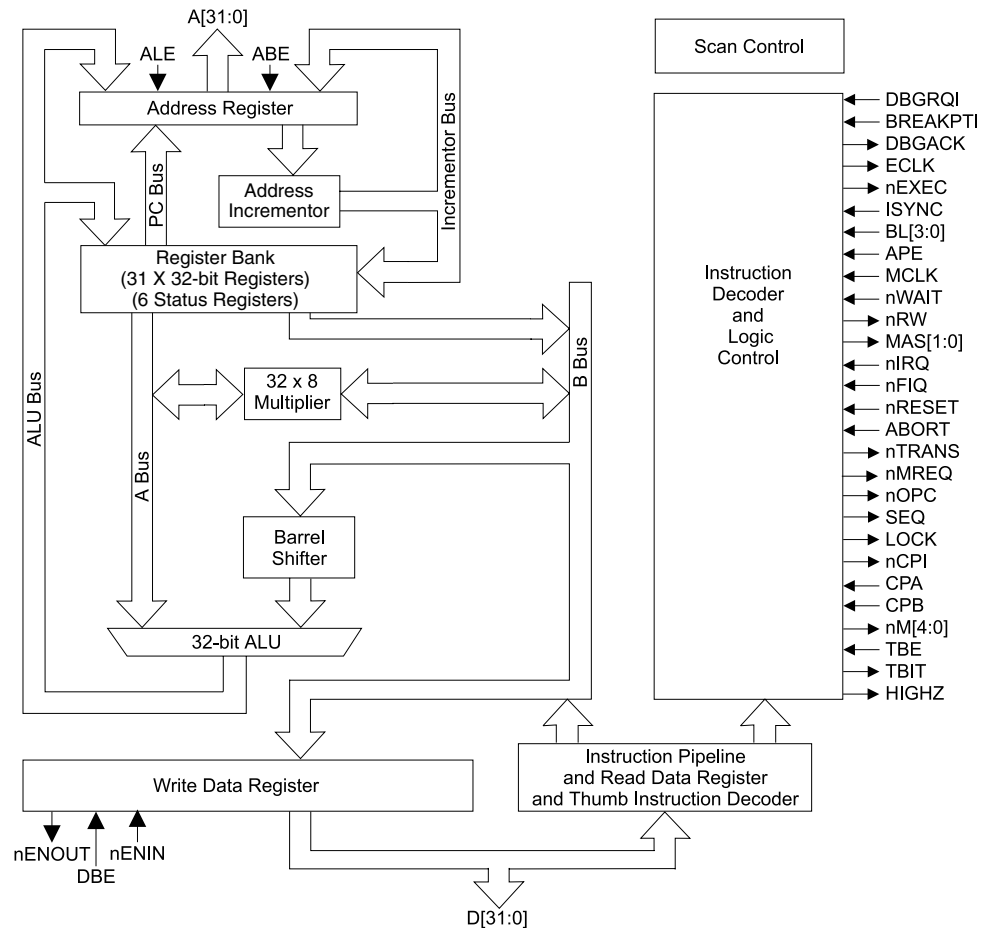
ARM920T™ 32-bit RISC Microprocessor Core

The ARM920T extends the capabilities of the popular ARM7TDMI, while maintaining code compatibility and Thumb instruction compression. Enhancements include Harvard architecture and a memory management unit with virtual addressing support (allowing the use of advanced platform operating systems such as Windows CE™, Linux®, Symbian OS™ and VxWorks™). 16 Kbyte data and instruction caches are included.

ARM946E-S™ 32-bit RISC Microprocessor Core

The ARM946E-S is a synthesizable version of the ARM9E-S core, with similar features to the ARM920T. The ARM9E-S instruction set adds saturation logic to enhance DSP implementation, as well as double-word data moves. Additional DSP features include a single cycle 16 x 32 Multiply Accumulate (MAC) Unit. A memory protection unit is provided, but without full virtual memory support. As a result, the ARM946E-S is more suited to deeply embedded tasks that do not require extended-platform OS support. Cache sizes can be tailored to the application, resulting in a (potentially) smaller die size compared to the ARM920T.

OakDSPCore® Digital Signal Processing Core

Atmel's hard macro OakDSPCore is a 16-bit, general purpose, low-power, low-voltage and high-speed Digital Signal Processor (DSP).

Oak is designed for mid-to-high-end telecommunications and consumer electronics applications, where low-power and portability are major requirements. Among the applications supported are digital cellular telephones, fast modems, advanced facsimile machines and hard disk drives. Oak is available as a DSP core in Atmel's ASIC cell library, to be utilized as an engine for a DSP-based ASIC. It is specified with several levels of modularity in SRAM, ROM and I/O blocks, allowing efficient DSP-based ASIC development.

Oak is aimed at achieving the best cost-performance factor for a given (small) silicon area. As a key element of a system-on-chip, it takes into account such requirements as program size, data memory size, glue logic and power management.

The Oak core consists of three main execution units operating in parallel: the Computation/Bit-Manipulation Unit (CBU), the Data Addressing Arithmetic Unit (DAAU) and the Program Control Unit (PCU).

The core also contains ROM and SRAM addressing units, and Program Control Logic (PCL). All other peripheral blocks that are application specific are defined as part of the user-specific logic and implemented around the DSP core on the same silicon die.

Oak has an enhanced set of DSP and general microprocessor functions to meet most application requirements. The Oak programming model and instruction set are aimed at the straightforward generation of efficient and compact code.

MIPS64™ 5Kf™ 64-bit RISC Microprocessor Core

The MIPS64 5Kf is a synthesizable MIPS64 5K family core that provides 64-bit address and data paths along with an onboard IEEE 754-compliant Floating Point Unit. A built-in memory management unit with virtual addressing support allows the use of platform operating systems such as Windows CE and others. Also provided are configurable instruction and data caches, as well as a multiply divide unit capable of single cycle 32 x 16 Multiply Accumulate (MAC) operations.

Teak and PalmDSPCore® Digital Signal Processing Cores

The Teak and Palm are synthesizable dual-MAC DSP cores from DSP Group, Inc. The Teak is a fixed-point 16-bit DSP, whereas the Palm can be configured for 16-bit, 20-bit or 24-bit fixed-point math. Both cores are optimized for high MIPs per mW, with performance targeted to handling filtering, voice compression/decompression and modem functions for portable and wireless applications such as 3G digital cellular. Hardware support is also provided for implementing Viterbi forward error correction.

The Teak and Palm cores both have a comprehensive suite of development tools that are easy to learn and are intended to support rapid code development. A C compiler that supports in-line assembly language and provides language extensions to enhance C code optimization is provided. An assembler and linker are also provided. Both emulation (using test silicon) and source-level simulation of C and assembly language enhance software verification.

ATL25 Series Cell Library

Atmel's ATL25 Series ASICs make use of an extensive library of cell structures, including logic cells, buffers and inverters, multiplexers, decoders and I/O options. Soft macros are also available.

These cells are characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test silicon. Characterization is performed over the rated temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Absolute Maximum Ratings*

Parameter	Rating
Operating Ambient Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Maximum Input Voltage: Inputs 3.3V Compliant 3.3V/5V Tolerant	 V_{DD} + 0.5V V_{DD3} + 0.5V 5.5V
Maximum Operating Voltage (V_{DD})	2.7V
Maximum Operating Voltage (V_{DD3})	3.6V

Note: * Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. 2.5-volt DC Characteristics
Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		−55		125	°C
V_{DD}	Supply Voltage	All		2.3	2.5	2.7	V
I_{IH}	High-level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD}$ (max)			10	µA
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD}$ (max) Pull-up = 620 KΩ	−10			µA
I_{OZ}	High-impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No pull-up or pull-down	−10		10	µA
I_{OS}	Output Short-circuit Current	PO11	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)		6		mA
		PO11	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)		−4		
V_{IH}	High-level Input Voltage	CMOS		$0.7V_{DD}$			V
		CMOS Schmitt		$0.7V_{DD}$	1.3		
V_{IL}	Low-level Input Voltage	CMOS				$0.3V_{DD}$	V
		CMOS Schmitt			1.1	$0.3V_{DD}$	
V_{HYS}	Hysteresis	CMOS Schmitt			0.4		V
V_{OH}	High-level Output Voltage (Standard and Tolerant)	PO11	$I_{OH} = 2$ mA, $V_{DD} = V_{DD}$ (max)	$0.7V_{DD}$			V
		3.3V Tolerant	$I_{OH} = 2$ mA	$0.7V_{DD}$			
V_{OL}	Low-level Output Voltage (Standard and Tolerant)	PO11	$I_{OL} = 2$ mA, $V_{DD} = V_{DD}$ (max)			$0.3V_{DD}$	V

Note: All I/Os 2.5V Compliant

Table 5. 3.3-volt DC Characteristics
Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		−55		125	°C
V_{DD}	Supply Voltage	All Except 3.3V Compliant I/O		2.3	2.5	2.7	V
V_{DD3}	Supply Voltage	3.3V Compliant I/O		3.0	3.3	3.6	V
I_{IH}	High-level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD}$ (max)			10	µA
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD}$ (max) Pull-up = 620 KΩ	−10			µA
I_{OZ}	High-impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = V_{DD}$ (max) No pull-up	−10		10	µA
I_{OS}	Output Short-circuit Current	2 mA Buffer	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)		10		mA
		2 mA Buffer	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)		−9		
V_{IH}	High-level Input Voltage	CMOS, LVTTL		2.0			V
		PCI		$0.475V_{DD3}$			
		CMOS/TTL-level Schmitt		2.0	1.7		
V_{IL}	Low-level Input Voltage	CMOS				0.8	V
		PCI				$0.325V_{DD3}$	
		CMOS/TTL-level Schmitt			1.1	0.8	
V_{HYS}	Hysteresis	TTL-level Schmitt			0.6		V
V_{OH}	High-level Output Voltage	PO11	$I_{OH} = 2$ mA, $V_{DD3} = V_{DD}$ (min)	$0.8V_{DD3}$			V
		PCI	$I_{OH} = 500$ µA	$0.9V_{DD3}$			
V_{OL}	Low-level Output Voltage	PO11	$I_{OL} = 2$ mA, $V_{DD3} = V_{DD}$ (min)			$0.2V_{DD}$	V
		PCI	$I_{OL} = 1.5$ mA			$0.1V_{DD}$	

Note: All I/Os 3.3V Tolerant/Compliant

Table 6. I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Typical	Units
C_{IN}	Capacitance, Input Buffer (die)	3.3V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3.3V	5.6	pF
$C_{I/O}$	Capacitance, Bidirectional	3.3V	6.6	pF

Testability Techniques

For complex designs involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs requires the use of more efficient testability techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in self-test logic (in addition to functional test patterns) must be employed to provide both the user and Atmel with the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microprocessor or DSP engine or both, SRAM to support the microprocessor or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high-performance digital tester. Combinations of parametric, functional and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and/or parametric testing can be performed. Since a digital tester must control all the clocks during the testing of an ASIC, provisions must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test without impinging upon the normal functionality.

In a similar vein, access to microprocessor, DSP and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. The ARM and MIPS microprocessors, AVR microcontroller and OakDSPCore/TeakDSPCore/PalmDSPCore digital signal processors all support SCAN testing. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins is a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that in almost all of these cases, the purpose of the testability technique is to assure all embedded circuit blocks are functional. All of the techniques described above should be considered supplemental to a set of patterns that exercise the functionality of the design in its anticipated operating modes.

Advanced Packaging

The ATL25 Series ASICs are offered in a wide variety of standard packages, including plastic and ceramic quad flatpacks, thin quad flatpacks, ceramic pin grid arrays and ball grid arrays. High-volume onshore and offshore contractors provide assembly and test for commercial product, with prototype capability in Colorado Springs. Custom package designs are also available as required to meet a customer's specific needs, and are supported through Atmel's package design center. If a standard package cannot meet a customer's needs, a package can be designed to precisely fit the customer-specific application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Table 7. Packaging Options–Partial List

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
Power Quad	144, 160, 208, 240, 304
L/TQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
PBGA	121, 169, 208, 217, 225, 240, 256, 272, 300, 304, 313, 316, 329, 352, 388, 420, 456
Super BGA	168, 204, 240, 256, 304, 352, 432, 560, 600
Low-profile Mini BGA	40, 48, 49, 56, 60, 64, 80, 81, 84, 96, 100, 108, 128, 132, 144, 160, 176, 192, 208, 224, 228
Chip-scale BGA	32, 36, 40, 48, 49, 56, 64, 81, 84, 100, 108, 121, 128, 144, 160, 169, 176, 192, 208, 224, 256, 288, 324
Flex-tape BGA	48, 49, 64, 80, 81, 84, 96, 100, 112, 132, 144, 156, 160, 180, 192, 196, 204, 208, 220, 225, 228, 256, 280
FCBGA[1]	416, 480, 564, 672, 788, 896, 960, 1032, 1152, 1157, 1292, 1357, 1413, 1500, 1517, 1557, 1677, 1728, 1932

Note: 1.   Require customer design substrate.

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