AUGUST 1999
Revision 1.1

10BASE-T PHY

Design and Layout Guide

General Description

This application note provides information essential for the successful design and layout of systems using Level One 10BASE-T PHY transceiver products. The following topics are covered in this document:

- Product Line Overview.
- Design and Layout Guidelines.
- Grounding Considerations.
- Network Interfaces.

Product Line Overview—This section summarizes features, functions, and characteristics of the LXT90X PHY transceiver product line.

Design and Layout Guidelines—This section provides design and layout guidelines to achieve the highest performance possible from Level One's 10BASE-T PHY transceivers. Meeting EMI and ESD requirements and achieving optimum line performance are accomplished by following good design practices throughout the *entire* design. This section also details placement of power and ground planes and provides some tips on avoiding the loop-antenna effect.

Grounding Considerations—The successful design and layout of any network product depends on a good grounding plan. Design considerations for earth, chassis, and circuit ground are discussed in this section.

Network Interfaces—The Network Interface section provides information about the Twisted-Pair Interface and Attachment Unit Interface (AUI).

The Twisted-Pair Interface section details the receive and transmit circuitry. This section includes magnetics information, impedance matching, and recommended termination circuitry.

The Attachment Unit Interface (AUI), is briefly discussed, and a standard AUI circuit diagram is provided.

Product Line Overview

The LXT90X family of Ethernet PHY transceivers supports 10BASE-T (10T) applications and includes the following products:

- LXT901/LXT907: Universal 10BASE-T and AUI PHY Transceivers.
- LXT901A/907A: Universal 10BASE-T and AUI PHY Transceivers.
- LXT902: Integrated 10BASE-T MAU.
- LXT905: 3.3V Universal 10BASE-T Transceiver.
- LXT908: 3.3V Universal 10BASE-T and AUI Transceiver.
- LXT944: Universal Quad 10BASE-T Transceiver.

Level One's Ethernet PHY transceivers implement all the required functions of the Physical Layer Signaling (PLS) and Media Attchment Unit (MAU) as defined in IEEE 802.3 and are designed for 10BASE-T hub, switch, and LAN adapter board products.

The LXT901, LXT901A, LXT907, LXT907A, and LXT908 are extremely robust universal transceivers with a twisted-pair and AUI port. They function as a PLS-only device (for use with 10BASE-2 or 10BASE-5 coaxial cable networks) or as an Integrated PLS/MAU (for use with twisted-pair networks). Selectable polarity schemes and control signal timing allow compatibility with most industry-standard 10BASE-T MAC controllers.

The LXT944 integrates four transceivers on a single chip that drives four independent 10BASE-T twisted-pair cables.

The LXT901 and LXT907 are operated with a single 5V power supply. The LXT901A, LXT907A, and LXT908 provide 3.3V low-power operation, ideal for mobile computing, modems, and NICs. The LXT905 operates at 5V or 3.3V. Functions offered in the PHY family include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link testing, and reversed polarity detection/correction. Integrated filters simplify the design work required for FCC-compliant EMI performance.

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DESIGN AND LAYOUT GUIDELINES

General Guidelines

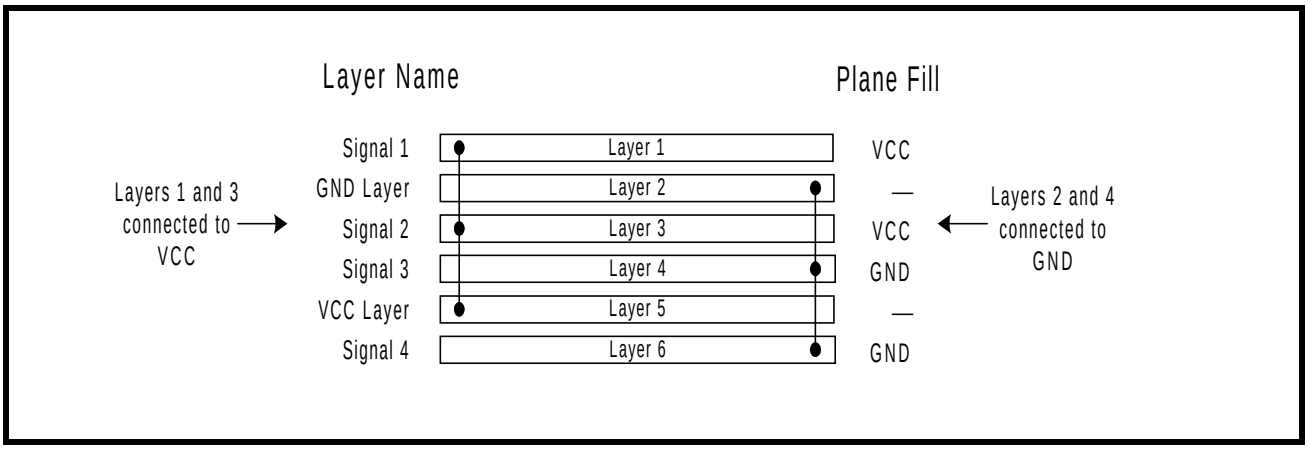
Good design practices are essential to meet EMI and ESD requirements, and to achieve maximum line performance. These practices minimize high-speed digital switching noise, common-mode noise, and provide shielding between internal circuits and the environment. Good design practices apply *throughout* the entire design and include the following:

- Verify that all components meet application requirements. Use component listings for reference only.
- Ensure that the power supply is rated for the load and that output ripple is minimal (<50 mV).
- Provide ample power planes.
- Keep power and ground noise levels below 50 mV.
- Void the power plane between the magnetics and RJ-45 connector and at the edge of the card. Use this region for chassis ground.
- Avoid breaks in the ground plane, especially in areas where it is shielding high-frequency signals.
- Use bulk capacitors (4.7-10 µF) between the power and ground planes to minimize switching noise, particularly near high-speed busses.
- Use an ample supply of .01 µF decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- Filter and shield DC-DC converters and oscillators.
- Keep high-speed signals out of the area between the device and the magnetics.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer. See signal layer filling diagram in Figure 1.

Power Requirements

LXT901 and LXT907 devices require a single +5V DC power supply and a single ground reference. Low-power devices, such as the LXT901A, LXT907A and LXT908, are supplied by a 3.3V power supply. The LXT905 may be supplied by either a 3.3V or 5V power supply.

Figure 1: Signal Layer Filling



Differential Signal Layout Guidelines

- Route differential pairs close together and away from other signals.
- Keep both traces of each differential pair as identical to each other as possible.
- Avoid vias and layer changes.
- Keep transmit and receive pairs away from each other. Run orthogonally, or separate with a ground plane layer.
- Place all components for the transmit circuit on one side of the board, and all components for the receive circuit on the other side of the board.

Clock Circuit

The clock circuit should provide a 20 MHz, 100 ppm digital reference clock to the LXT90X. A crystal oscillator and clock driver are recommended. Characteristics of the clock include:

Duty cycle distortion no greater than 40 to 60%.

CMOS voltage levels (V_{OH} > 2.4V).

Jitter less than 0.5 ns.

Crystals, oscillators, and DC-to-DC converters can create significant low- and high-frequency noise and generate unwanted magnetic fields if not handled correctly. These types of components should be surrounded with ample decoupling and bypass capacitors, which can greatly reduce the impact of unwanted noise and magnetic energy that can substantially degrade performance.

Noise and Filtering

Power supply ripple and digital switching noise can be created by:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (>32-bits) running at a high clock rate
- DC-to-DC converters.

Noise created by these sources can be coupled through the power and ground planes into the transmitter and receiver and out onto the network. Coupling can occur via the termination circuits or through the analog power and ground pins of the LXT90X.

Use the criteria in Table 1 for evaluating noise levels in the power and ground planes.

Table 1: Criteria for Noise Levels

Noise Level	Acceptability
Under 50 mV	Acceptable
50 mV to 80 mV	Marginally Acceptable
Above 80 mV	Unacceptable

Bypass and Decoupling Capacitors

Bypass capacitors shunt high-frequency noise from the power plane to the ground plane and create a virtual short between power and ground planes at high frequencies. The noise is shunted to the ground plane and dispersed.

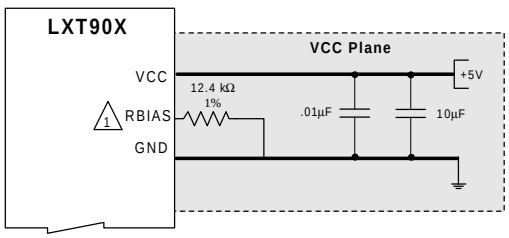
Place a high-frequency bypass cap (.01 µF) between each VCC pin and its associated ground pin as shown in Figure 2.

All bypass capacitors have parasitic inductance associated with them. This parasitic inductance causes the capacitors to have a resonance frequency, above which the capacitors actually become inductive. The suggested .01 µf cap provides protection up to 140 MHz. Use ample bypass and decoupling capacitors in a design to help minimize high-frequency noise on the power and ground planes.

Bulk Capacitors

Use bulk capacitors (4.7 µF - 10 µF typical) liberally in a design to minimize switching noise. Place a bulk capacitor near the VCC pin of the LXT90X and scatter them throughout the entire design to improve system performance.

Figure 2: Power and Ground Decoupling



1. Resistor value for RBIAS = 7.5k Ω for the LXT905 and LXT944.

Power and Ground Planes

Layout and placement of the power and ground planes are shown in Figure 3.

Power Plane

The power plane is one continuous plane that extends from the magnetics through the rest of the board. All components and high-speed signals should be placed in this area.

Ground Plane

For high-speed communications design, the ground plane may be conceptually divided into two distinct regions:

- Chassis Ground Plane
- Signal Ground Plane

Chassis Ground Plane

The chassis ground region extends from the front edge of the board (RJ-45 connectors) to the magnetics and around the entire perimeter of the board. No signals should pass through this region except for external interfaces and LED signals. This region can be used for a separate chassis ground plane (connected to the chassis), and connected to cable shields, unused signals, and safety earth ground.

Signal Ground Plane

The signal ground plane is one continuous, unbroken plane that extends from the magnetics through the rest of the board. The signal ground plane may be combined with chassis ground or isolated from it.

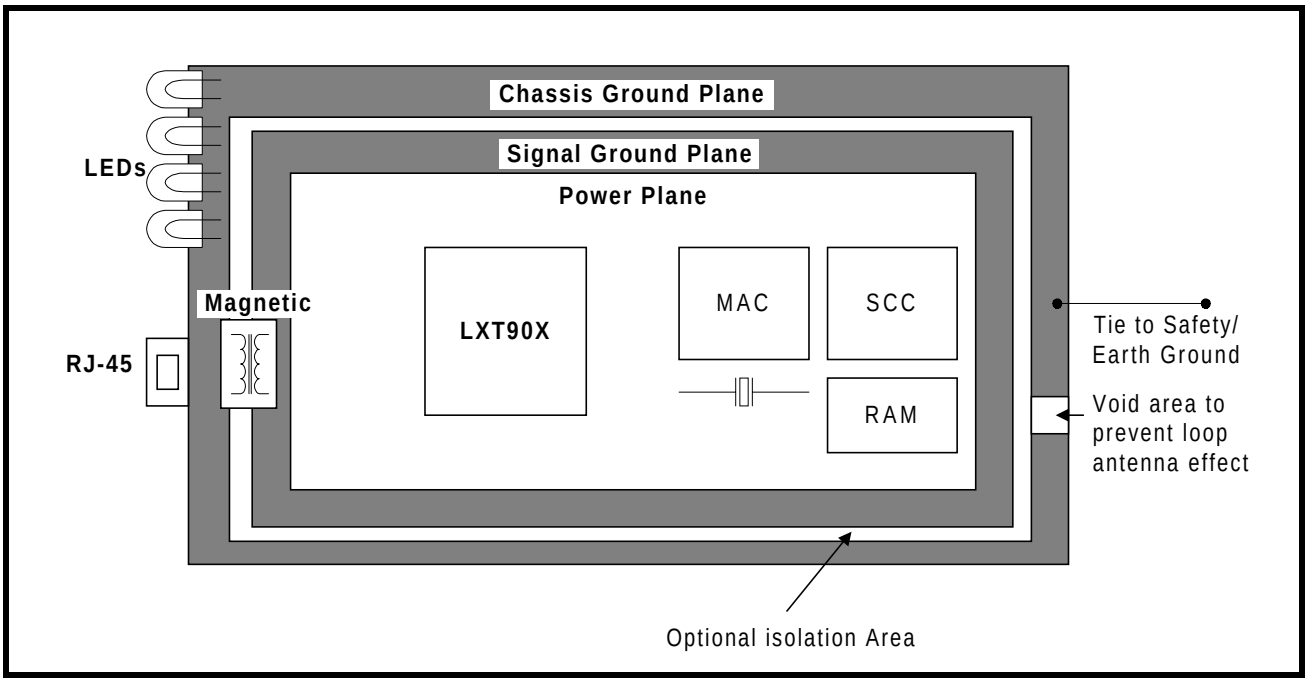
For isolation, place a “moat” around the signal ground plane to separate signal ground from chassis ground. If the ground planes are combined, an isolation area is not required.

Avoiding Loop Antenna Effect

When laying out ground planes, take extra care to avoid creating a loop antenna effect.

- Run all ground planes as solid square or rectangular regions.
- Avoid creating loops with ground planes around other planes. The only exception to this rule is chassis ground, as shown in Figure 3.
- Ensure the chassis ground area (running the perimeter of the board) is voided at some point.
- Ensure the gap of the voided area in chassis ground is large enough to prevent a loop antenna effect.

Figure 3: Power and Ground Placement



GROUNDING CONSIDERATIONS

The success of any networking product depends on beginning with a good electrical grounding plan. The ground "anchors" the product electrically and provides an escape path for unwanted electrical and magnetic energy. This note considers three kinds of ground: earth, chassis, and circuit.

Earth Ground

Earth ground is the absolute reference point for any electrical system.

Design Considerations

A designer's capability to control the earth ground connection varies greatly—from complete to little or no control. Three possible scenarios are presented here.

Earth ground is directly available to the designer. The power supply is often an integrated part of the design. In many countries, power outlets provide a specific connection point to earth ground that is separate from the power connections ("hot" and "return" leads for power, and a third "safety" lead for earth ground). In this case, earth ground is brought to the unit through the power cord and the designer has complete control.

Earth ground connection is indirectly available to the designer. The product may be a sub-component of a product with an integrated power supply. This is the case for a Network Interface Card (NIC) or PCMCIA card in a PC or laptop, or for a plug-in card in a communications product. Here, connections to earth ground are limited by the overall product design. Often, electronic connection is made through a backplane that does not provide a separate earth ground connection. Connection to earth ground, in this case, is made mechanically through mounting brackets or spring fingers.

Earth ground is not available to the designer. The product may be powered from a DC wall jack. In this case, design options are very limited.

Chassis Ground

Whenever possible, the designer should provide a connection between chassis ground and earth ground. The primary benefit of a connection between the chassis and earth ground is safety—to protect users from electrocution. A secondary benefit of this connection is to protect the electronics from Electro-Static Discharge (ESD), which is generated primarily by people. A second source of ESD is long cable connections (>1km), particularly between buildings. Over these distances, large differences in earth ground potential can build up—as much as 1 or 2 kV, especially during electrical storms.

Electronic devices are generally built to withstand some amount of ESD. Level One designs its integrated circuits with a goal of achieving 2kV isolation on all pins. At a systems level, typical ESD testing requirements go at least up to 15kV, and the system designer must provide the difference. At a system level, the solution is to route ESD currents to chassis ground, then to earth ground, avoiding the electronics as much as possible. Cable shields and sometimes the unused wires in the cable can be tied to chassis ground, which is then tied to earth ground.

Metal Chassis

A metal chassis provides a Farraday shield, which prevents unwanted electrical and magnetic fields from emanating from the product. It also protects the product from outside electrical and magnetic fields. The chassis is then securely connected to earth ground.

Non-Metallic Chassis

Many high-volume designs completely dispense with a metal chassis, preferring instead a molded-plastic case. Even though the circuit does not have a metal chassis, a chassis ground connected to earth ground is still recommended. The chassis ground can be incorporated into the design of the PCB board as a separate ground plane and provides ESD protection and some measure of Farraday shielding.

Circuit Ground

Circuit ground is the working reference point for the electronic design, and is generated by the power supply. Note that circuit ground *is not* the same as chassis/earth ground, and there are good reasons for carefully designing how the two should be connected:

- Unwanted high-frequency noise should be kept from leaking out as much as possible.
- Unwanted ESD energy should be shunted away from sensitive electronics.

There are two common (and opposite) techniques for handling unwanted noise and ESD: single- and multi-point grounding.

Single-Point Grounding

The single-point grounding technique connects chassis ground and circuit ground at a single point, usually at the power supply.

Multi-Point Grounding

The multi-point grounding technique connects the chassis and circuit ground at as many points as possible. Benefits of multi-point grounding include:

- Stress at any one point is limited because there are many points of connection.
- Although there are many connection points, where the connections are made is controlled and limited.

Using Single- or Multi-Point Grounding Design Schemes

- In a stand-alone design with integrated power supply, the designer is free to choose either a multi-point or single-point grounding scheme.
- In a sub-component design, the grounding scheme is defined by the system designer and is not at the discretion of the subcomponent designer. In this case, there are typically separate connections for chassis ground and circuit ground (brackets and spacers vs. backplane connector).
- In a wall-jack powered design, a single-point grounding scheme is usually the easiest approach.

NETWORK INTERFACES

Twisted-Pair Interface

The twisted-pair interface consists of termination networks for the receiver and transmitter, magnetics, and RJ-45 connector. A circuit known as a “Bob Smith” termination (see Figure 8 on page 9) is used to terminate unused signal pairs.

Receive Interface Circuit

The receive interface circuit requires magnetics with a 1:1 turns ratio for the receive transformer and includes a main winding and termination resistance to match the line impedance.

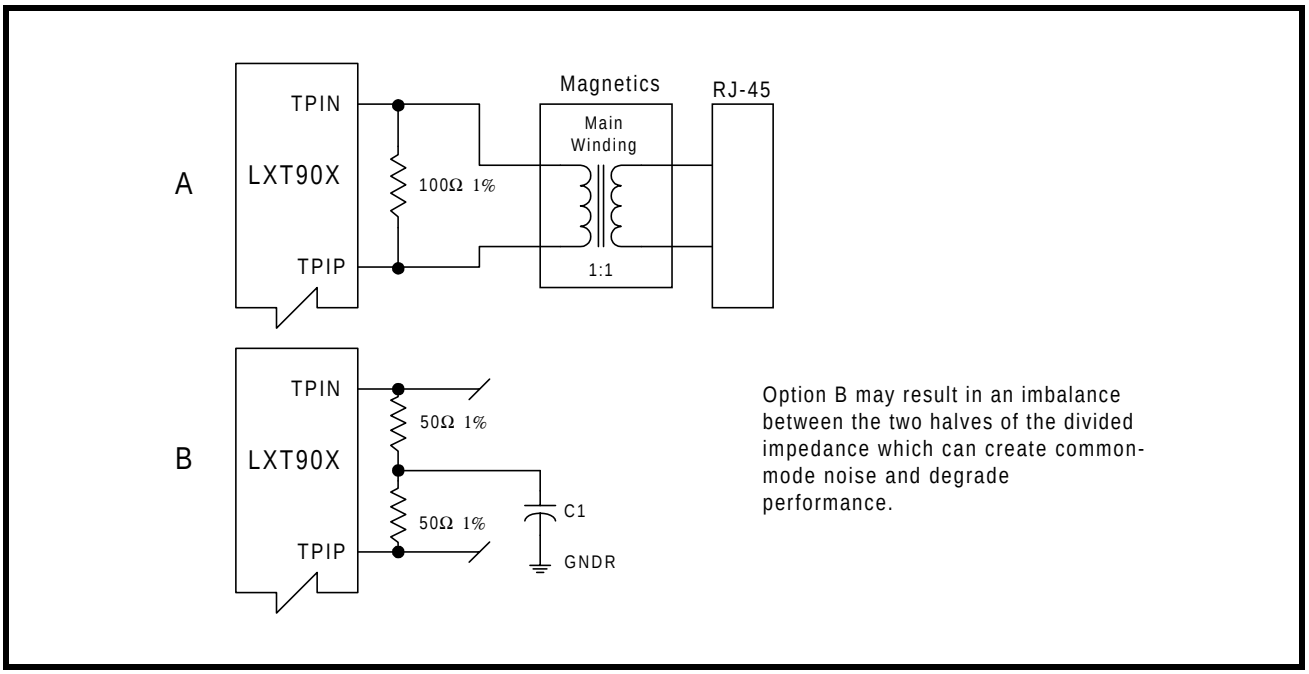
Level One 10BASE-T PHY transceivers provide on-chip advanced pulse shaping and filters omitting the need for magnetics that have optional Common-Mode (CM) chokes. When general guidelines are closely followed throughout a design to minimize common-mode noise, magnetics without CM chokes should be adequate for designing a reliable network connection.

Termination Circuitry

Figure 4 shows two options for receive termination. In both options a 100Ω load is placed across the TPIP/TPIN input pair. The first option, Figure 4A, consists of a single 100Ω resistor across the input. The second option, Figure 4B, is to divide the resistor in two with a common-mode bypass cap (.01 µF) to ground.

Testing done to date has shown neither option is consistently better. Results are strongly dependent on the specific application. The advantage of the two-resistor approach is that the bypass cap can provide additional common-mode shielding if the ground is quiet. The disadvantage of the two-resistor approach is that any imbalance or mismatch between the two resistors can create common-mode noise.

Figure 4: Receive Interface Circuitry



Transmit Interface Circuit

The turns ratio for the transmit magnetics varies across the PHY transceiver product line (see Table 2 for details). Level One 10BASE-T PHY transceivers provide on-chip advanced pulse shaping and filters omitting the need for magnetics that have optional Common-Mode (CM) chokes. When general guidelines are closely followed throughout a design to minimize common-mode noise, magnetics without CM chokes should be adequate for designing a reliable network connection.

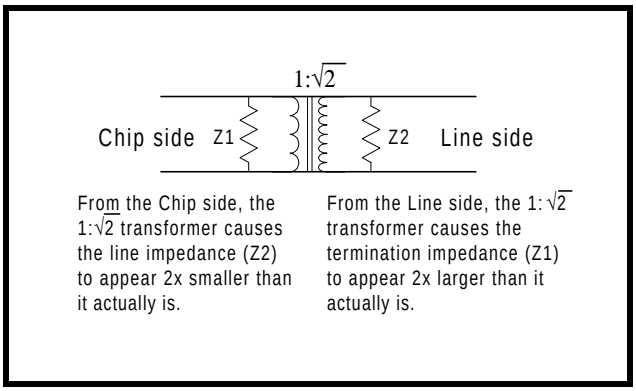
A reference list of magnetics manufacturers and part numbers are provided for each PHY transceiver device in Application Note 73: *Magnetic Manufacturers for Networking Product Applications*. Termination circuitry must be matched according to the turns ratio of the magnetic and line impedance.

Table 2: Magnetics Tx Ratio

Tx Ratio	Product(s)
1:1	LXT902
1:2	LXT905, LXT908
1:$\sqrt{2}$	LXT901, LXT901A, LXT907, LXT907A, LXT944

The output stages for the receiver and the transmitter shown in Figure 6 are designed to match a 100Ω characteristic impedance of twisted-pair wire. On the transmit side, a 1:$\sqrt{2}$ turns ratio causes the 50Ω termination to appear as a 100Ω termination to the line (see Figure 5).

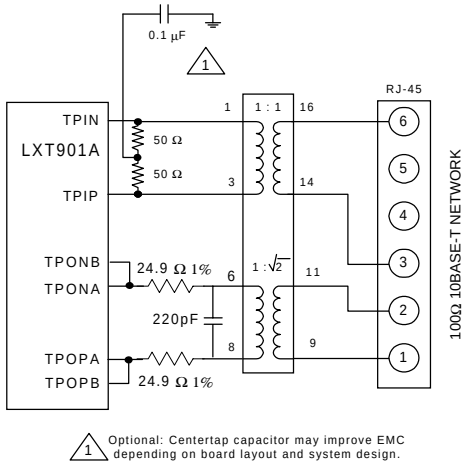
Figure 5: Effects of a 1:$\sqrt{2}$ Turns Ratio



Dual-Pair Termination

The LXT901, LXT901A, LXT907, LXT907A, and LXT908 are designed with dual-driver output pairs (TPOPA/TPOPB and TPONA/TPONB). The positive and negative sides of both output pairs are shorted together and tied to the transformer through a 24.9 Ω 1% series resistor (as shown in Figure 6).

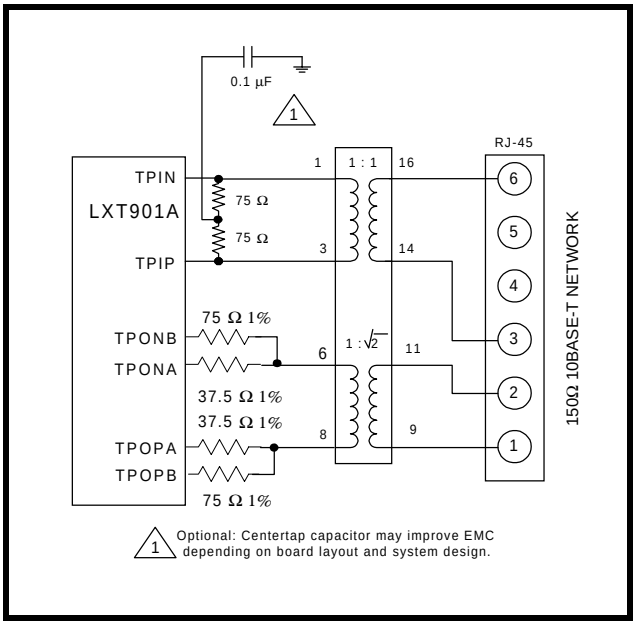
Figure 6: Dual-Pair Termination Circuit



Combination UTP/STP Termination

Most PHY products are configured with 100Ω termination for Unshielded Twisted-Pair (UTP). The LXT901 and LXT901A are designed with a Shielded Twisted-Pair ($\overline{STP}$) select pin that allows the device to match either 100Ω or 150Ω twisted-pair media. Resistors must be installed on each input and output pair to match impedance of the network media being used. A dual-resistor combination can be configured to accommodate both line terminations as shown in Figure 7. When 100Ω termination is selected, both A and B pairs are driven in parallel. When 150Ω termination is selected, the B pair is tri-stated and only the A pair is driven.

Figure 7: Combination Termination Circuit



Unused Connections

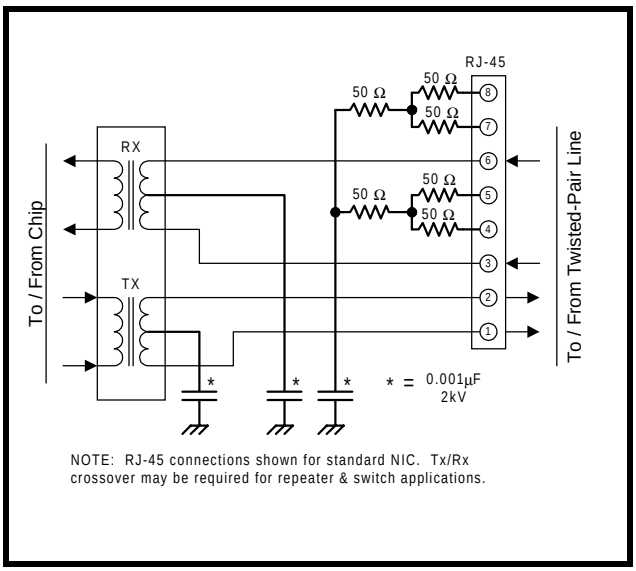
Unused Twisted-Pair Port

In applications not requiring the twisted-pair port, it is recommended that the input pair for the twisted-pair data signals (TPIP/TPIN) be differentially terminated by connecting the positive signal to the negative signal. The output pair (TPOP/TPON) can be left floating.

Unused RJ-45 Pins

A “Bob Smith” termination is often provided for the unused signal pairs of a twisted-pair interface (RJ-45 pins 4, 5, 7, and 8). Although there are many variations on this technique, the most common implementation is shown in Figure 8. Note that the signals are referenced to chassis ground rather than circuit ground.

Figure 8: Bob Smith Termination Circuit



Attachment Unit Interface (AUI)

The LXT901, LXT901A, LXT907, LXT907A, and LXT908 support both a twisted-pair and AUI interface. An automatic port switching feature (AUTOSEL) selects either the D-connector (AUI) or the RJ-45 connector (10BASE-T).

The AUI interface consists of three circuits. The Data Output (DO), Data Input (DI), and Collision (CI). In PLS mode, the LXT90X receives incoming signals from the AUI DI circuit with ±18 ns of jitter and drives the AUI D0 circuit.

AUI Port Termination

Figure 9 shows termination circuitry for the LXT90X AUI port in a typical application. Impedance matching resistors are installed in each I/O pair but no external filters are required.

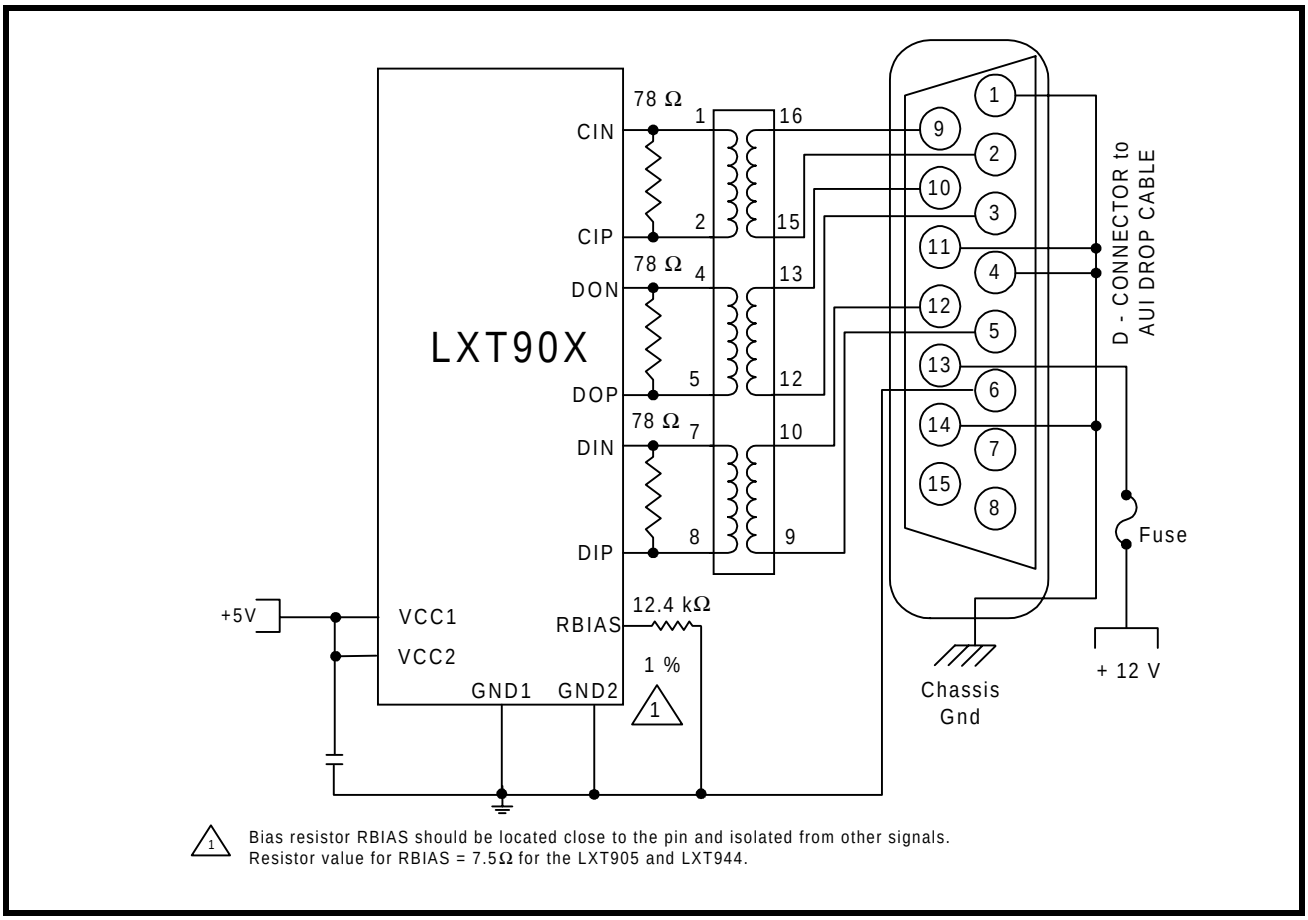
Unused AUI Port

In applications not requiring the AUI port, it is recommended that the AUI data input pair (DIP/DIN), output pair (DOP/DON), and the collision signals (CIP/CIN) be differentially terminated. This is accomplished by connecting the positive signal to the negative signal for each pair.

NOTE

Do not float or ground these pins, which may cause the AUI port to be falsely perceived as "active".

Figure 9: Typical Internal MAU Application



REVISION HISTORY

Table 3: Changes from Revision 1.0 to Revision 1.1 (8/11/99)

Section	Page	Change	Text
Product Line Overview	1	Modify	Delete references to LXT904 and LXT906. Add LXT901 and LXT907. Clarify 3.3V-only product.
Power Requirements	2	Modify	Clarify 3.3V-only product.
Figure 1 Signal Layer Filling	2	Modify	Add notes for clarification.
Table 2 Magnetics Tx Ratio	8	Modify	Delete LXT904 and LXT906. Add LXT901 and LXT907.
Dual-Pair Termination	8	Modify	Add LXT901 and LXT907.
Combination UTP/STP Termination	9	Modify	Add LXT901.
Figure 8 Unused RJ-45 Pins	9	Update	Update termination diagram.
Attachment Unit Interface (AUI)	10	Modify	Add LXT901 and 907.

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Revision	Date	Status
1.1	08/99	Update termination diagram (Figure 8), add note to figures 6 and 7, remove references to LXT904 and LXT906, add LXT901 and LXT907, clarify statements on 5V vs 3.3V power supplies.
1.0	08/98	Initial Release.

AN-061-T9XX-R1.1-0899