

## ADR01/ADR02/ADR03

### FEATURES

- Ultracompact SC70-5/TSOT-5**
- Low temperature coefficient 3 ppm/°C**
- No external capacitor required**
- Long term stability 50 ppm/1000 hr**
- Line regulation 30 ppm/V**
- Load regulation 70 ppm/mA**
- Low noise 25  $\mu$ V p-p (0.1 Hz to 10 Hz)**
- Low hysteresis 70 ppm typical**
- Wide operating range**
- ADR01 12 V to 40 V**
- ADR02 7 V to 40 V**
- ADR03 4.5 V to 40 V**
- Quiescent current 1 mA maximum**
- High output current 10 mA**
- Wide temperature range -40°C to +125°C**
- Industry standard REF01/REF02/REF03 compatible<sup>1</sup>**

### APPLICATIONS

- Precision data acquisition systems**
- High resolution converters**
- Industrial process control systems**
- Precision instruments**
- PCMCIA cards**

### PIN CONFIGURATIONS

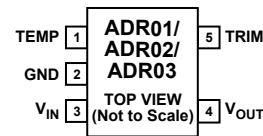
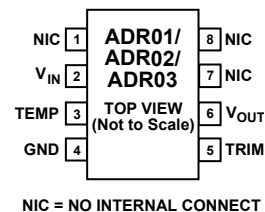


Figure 1. 5-Lead SC70/TSOT Surface Mount Packages



NIC = NO INTERNAL CONNECT

Figure 2. 8-Lead SOIC Surface Mount Package

### GENERAL DESCRIPTION

The ADR01, ADR02, and ADR03 are precision 10 V, 5 V, and 2.5 V band gap voltage references featuring high accuracy, high stability, and low power. The parts are housed in tiny SC70-5 and TSOT-5 packages, as well as the SOIC-8 versions, which are available for industry standard REF01, REF02, and REF03 drop-in replacement.<sup>1</sup> The small footprint and wide operating range make them ideal for general-purpose and space constraint applications.

With an external buffer and a simple resistor network, the TEMP terminal can be used for temperature sensing and approximation. A TRIM terminal is provided on the ADR01, ADR02, and ADR03 for fine adjustment of the output voltage.

The ADR01, ADR02, and ADR03 are compact, low drift voltage references that provide an extremely stable output voltage from a wide supply voltage range. They are available in SC70-5, TSOT-5, and SOIC-8 packages with A and B grade selections. All parts are specified over the extended industrial (-40°C to +125°C) temperature range.

<sup>1</sup> ADR01, ADR02, and ADR03 are component-level compatible with REF01, REF02, and REF03, respectively. No guarantees for system-level compatibility are implied. SOIC-8 versions of ADR01/ADR02/ADR03 are pin-to-pin compatible with SOIC-8 versions of REF01/REF02/REF03, respectively, with the additional temperature monitoring function.

### Rev. C

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# ADR01/ADR02/ADR03

## TABLE OF CONTENTS

Specifications.....	3	Introduction.....	14
Absolute Maximum Ratings.....	7	Applying the ADR01/ADR02/ADR03.....	14
Parameter Definitions.....	8	Applications.....	15
Typical Performance Characteristics.....	9	Outline Dimensions.....	18
Theory of Operation.....	14	Ordering Guide.....	20

## REVISION HISTORY

### Revision C

6/03—Data Sheet Changed from REV. B to REV. C.

Changes to FEATURES.....	1
Changes to GENERAL DESCRIPTION.....	1
Changes to Figure 2.....	1
Changes to SPECIFICATIONS.....	2
Addition of Dice Electrical Characteristics and Layout.....	6
Changes to ABSOLUTE MAXIMUM RATINGS.....	7
Updated SOIC (R-8) Outline Dimensions.....	19
Changes to ORDERING GUIDE.....	20

### Revision B

2/03—Data Sheet Changed from REV. A to REV. B.

Added ADR03.....	Universal
Added TSOT-5 (UJ) Package.....	Universal
Updated OUTLINE DIMENSIONS.....	18

### Revision A

12/02—Data Sheet Changed from REV. 0 to REV. A.

Changes to Features.....	1
Changes to GENERAL DESCRIPTION.....	1
Table I deleted.....	1
Changes to ADR01 SPECIFICATIONS.....	2
Changes to ADR02 SPECIFICATIONS.....	3
Changes to ABSOLUTE MAXIMUM RATINGS.....	4
Changes to ORDERING GUIDE.....	4
Updated OUTLINE DIMENSIONS.....	12

## SPECIFICATIONS

**Table 1. ADR01—Electrical Characteristics ( $V_{IN} = 12\text{ V to }40\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	$V_O$	A Grade	9.990	10.000	10.010	V
Initial Accuracy	$V_{OERR}$	A Grade			10	mV
					0.1	%
Output Voltage	$V_O$	B Grade	9.995	10.000	10.005	V
Initial Accuracy	$V_{OERR}$	B Grade			5	mV
					0.05	%
Temperature Coefficient	$TCV_O$	A Grade, SOIC-8, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	10	ppm/ $^\circ\text{C}$
		A Grade, TSOT-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			25	ppm/ $^\circ\text{C}$
		A Grade, SC70-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			25	ppm/ $^\circ\text{C}$
		B Grade, SOIC-8, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
		B Grade, TSOT-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			9	ppm/ $^\circ\text{C}$
		B Grade, SC70-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			9	ppm/ $^\circ\text{C}$
Supply Voltage Headroom	$V_{IN} - V_O$		2			V
Line Regulation	$\Delta V_O / \Delta V_{IN}$	$V_{IN} = 12\text{ V to }40\text{ V}$ , $-40^\circ < T_A < +125^\circ\text{C}$		7	30	ppm/V
Load Regulation	$\Delta V_O / \Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }10\text{ mA}$ , $-40^\circ < T_A < +125^\circ\text{C}$ , $V_{IN} = 15\text{ V}$		40	70	ppm/mA
Quiescent Current	$I_{IN}$	No Load, $-40^\circ < T_A < +125^\circ\text{C}$		0.65	1	mA
Voltage Noise	$e_{N\text{ p-p}}$	0.1 Hz to 10 Hz		20		$\mu\text{V p-p}$
Voltage Noise Density	$e_N$	1 kHz		510		nV/ $\sqrt{\text{Hz}}$
Turn-On Settling Time	$t_R$			4		$\mu\text{s}$
Long Term Stability <sup>1</sup>	$\Delta V_O$	1,000 Hours		50		ppm
Output Voltage Hysteresis	$\Delta V_{O\_HYS}$			70		ppm
Ripple Rejection Ratio	RRR	$f_{IN} = 10\text{ kHz}$		-75		dB
Short Circuit to GND	$I_{SC}$			30		mA
Voltage Output at TEMP Pin	$V_{TEMP}$			550		mV
Temperature Sensitivity	$TCV_{TEMP}$			1.96		mV/ $^\circ\text{C}$

<sup>1</sup>The long term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

# ADR01/ADR02/ADR03

**Table 2. ADR02—Electrical Characteristics ( $V_{IN} = 7\text{ V to }40\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	$V_O$	A Grade	4.995	5.000	5.005	V
Initial Accuracy	$V_{OERR}$	A Grade			5	mV
					0.1	%
Output Voltage	$V_O$	B Grade	4.997	5.000	5.003	V
Initial Accuracy	$V_{OERR}$	B Grade			3	mV
					0.06	%
Temperature Coefficient	$TCV_O$	A Grade, SOIC-8, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	10	ppm/ $^\circ\text{C}$
		A Grade, TSOT-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			25	ppm/ $^\circ\text{C}$
		A Grade, SC70-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			25	ppm/ $^\circ\text{C}$
		B Grade, SOIC-8, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
		B Grade, TSOT-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			9	ppm/ $^\circ\text{C}$
		B Grade, SC70-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			9	ppm/ $^\circ\text{C}$
Supply Voltage Headroom	$V_{IN} - V_O$		2			V
Line Regulation	$\Delta V_O / \Delta V_{IN}$	$V_{IN} = 7\text{ V to }40\text{ V}$ , $-40^\circ < T_A < +125^\circ\text{C}$		7	30	ppm/V
Load Regulation	$\Delta V_O / \Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }10\text{ mA}$ , $-40^\circ < T_A < +125^\circ\text{C}$ , $V_{IN} = 10\text{ V}$		40	70	ppm/mA
Quiescent Current	$I_{IN}$	No Load, $-40^\circ < T_A < +125^\circ\text{C}$		0.65	1	mA
Voltage Noise	$e_{N\text{ p-p}}$	0.1 Hz to 10 Hz		10		$\mu\text{V p-p}$
Voltage Noise Density	$e_N$	1 kHz		230		$\text{nV}/\sqrt{\text{Hz}}$
Turn-On Settling Time	$t_R$			4		$\mu\text{s}$
Long Term Stability <sup>1</sup>	$\Delta V_O$	1,000 Hours		50		ppm
Output Voltage Hysteresis	$\Delta V_{O\_HYS}$			70		ppm
Ripple Rejection Ratio	RRR	$f_{IN} = 10\text{ kHz}$		-75		dB
Short Circuit to GND	$I_{SC}$			30		mA
Voltage Output at TEMP Pin	$V_{TEMP}$			550		mV
Temperature Sensitivity	$TCV_{TEMP}$			1.96		$\text{mV}/^\circ\text{C}$

<sup>1</sup>The long term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

**Table 3. ADR03—Electrical Characteristics ( $V_{IN} = 4.5\text{ V to }40\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	$V_O$	A Grade	2.495	2.500	2.505	V
Initial Accuracy	$V_{OERR}$	A Grade			5	mV
					0.2	%
Output Voltage	$V_O$	B Grade	2.4975	2.5000	2.5025	V
Initial Accuracy	$V_{OERR}$	B Grade			2.5	mV
					0.1	%
Temperature Coefficient	$TCV_O$	A Grade, SOIC-8, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		3	10	ppm/ $^\circ\text{C}$
		A Grade, TSOT-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			25	ppm/ $^\circ\text{C}$
		A Grade, SC70-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			25	ppm/ $^\circ\text{C}$
		B Grade, SOIC-8, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	3	ppm/ $^\circ\text{C}$
		B Grade, TSOT-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			9	ppm/ $^\circ\text{C}$
		B Grade, SC70-5, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			9	ppm/ $^\circ\text{C}$
Supply Voltage Headroom	$V_{IN} - V_O$		2			V
Line Regulation	$\Delta V_O / \Delta V_{IN}$	$V_{IN} = 7.5\text{ V to }40\text{ V}$ , $-40^\circ < T_A < +125^\circ\text{C}$		7	30	ppm/V
Load Regulation	$\Delta V_O / \Delta I_{LOAD}$	$I_{LOAD} = 0\text{ mA to }10\text{ mA}$ , $-40^\circ < T_A < +125^\circ\text{C}$ , $V_{IN} = 7.0\text{ V}$		25	70	ppm/mA
Quiescent Current	$I_{IN}$	No Load, $-40^\circ < T_A < +125^\circ\text{C}$		0.65	1	mA
Voltage Noise	$e_{N\text{ p-p}}$	0.1 Hz to 10 Hz		10		$\mu\text{V p-p}$
Voltage Noise Density	$e_N$	1 kHz		105		nV/ $\sqrt{\text{Hz}}$
Turn-On Settling Time	$t_R$			4		$\mu\text{s}$
Long Term Stability <sup>1</sup>	$\Delta V_O$	1,000 Hours		50		ppm
Output Voltage Hysteresis	$\Delta V_{O\_HYS}$			70		ppm
Ripple Rejection Ratio	RRR	$f_{IN} = 10\text{ kHz}$		-75		dB
Short Circuit to GND	$I_{SC}$			30		mA
Temperature Sensitivity	$TCV_{TEMP}$			1.96		mV/ $^\circ\text{C}$

<sup>1</sup>The long term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

# ADR01/ADR02/ADR03

**Table 4. Dice Electrical Characteristics ( $V_{IN} = \text{up to } 40 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage						
ADR01NBC	$V_O$	$25^\circ\text{C}$	9.995	10.004	10.005	V
ADR02NBC	$V_O$	$25^\circ\text{C}$	4.997	5.002	5.003	V
Temperature Coefficient	$TCV_O$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10		ppm/ $^\circ\text{C}$
Line Regulation						
ADR01NBC	$\Delta V_O / \Delta V_{IN}$	$V_{IN} = 15 \text{ V to } 40 \text{ V}$		7		ppm/V
ADR02NBC	$\Delta V_O / \Delta V_{IN}$	$V_{IN} = 7 \text{ V to } 40 \text{ V}$		7		ppm/V
Load Regulation	$\Delta V_O / \Delta I_{LOAD}$	$I_{LOAD} = 0 \text{ mA to } 10 \text{ mA}$		40		ppm/mA
Quiescent Current	$I_{IN}$	No Load		0.65		mA
Voltage Noise	$e_{N \text{ p-p}}$	0.1 Hz to 10 Hz		25		$\mu\text{V p-p}$

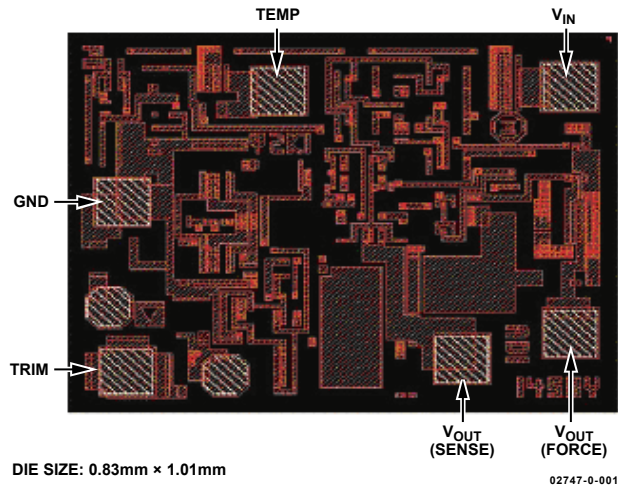


Figure 3. Die Layout

## ABSOLUTE MAXIMUM RATINGS

**Table 5. Absolute Maximum Ratings (at 25°C, unless otherwise noted)**

Parameter	Rating
Supply Voltage	40 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range: KS, UJ, R Packages	-65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

**Table 6. Thermal Resistance**

Package Type	$\theta_{JA}^1$	$\theta_{JC}$	Unit
SC70-5 (KS-5)	376	189	°C/W
TSOT-5 (UJ-5)	230	146	°C/W
SOIC-8 (R-8)	130	43	°C/W

<sup>1</sup>  $\theta_{JA}$  is specified for the worst-case conditions, i.e.,  $\theta_{JA}$  is specified for device soldered in circuit board for surface mount packages.

## PARAMETER DEFINITIONS

### TEMPERATURE COEFFICIENT

The change of output voltage with respect to operating temperature changes normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and can be determined by the following equation:

$$TCV_O[\text{ppm}/^\circ\text{C}] = \frac{V_O(T_2) - V_O(T_1)}{V_O(25^\circ\text{C}) \times (T_2 - T_1)} \times 10^6$$

where,

$$V_O(25^\circ\text{C}) = V_O \text{ at } 25^\circ\text{C}$$

$$V_O(T_1) = V_O \text{ at temperature 1}$$

$$V_O(T_2) = V_O \text{ at temperature 2}$$

### LINE REGULATION

The change in output voltage due to a specified change in input voltage. This parameter accounts for the effects of self-heating. Line regulation is expressed in either percent per volt, parts-per-million per volt, or microvolts per volt change in input voltage.

### LOAD REGULATION

The change in output voltage due to a specified change in load current. This parameter accounts for the effects of self-heating. Load regulation is expressed in either microvolts per milliampere, parts-per-million per milliampere, or ohms of dc output resistance.

### LONG TERM STABILITY

Typical shift of output voltage at 25°C on a sample of parts subjected to a test of 1,000 hours at 25°C:

$$\Delta V_O = V_O(t_0) - V_O(t_1)$$

$$\Delta V_O[\text{ppm}] = \frac{V_O(t_0) - V_O(t_1)}{V_O(t_0)} \times 10^6$$

where,

$$V_O(t_0) = V_O \text{ at } 25^\circ\text{C} \text{ at time 0}$$

$$V_O(t_1) = V_O \text{ at } 25^\circ\text{C} \text{ after 1,000 hours operation at } 25^\circ\text{C}$$

### THERMAL HYSTERISIS

Defined as the change of output voltage after the device is cycled through temperature from +25°C to -40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle.

$$V_{O\_HYS} = V_O(25^\circ\text{C}) - V_{O\_TC}$$

$$V_{O\_HYS}[\text{ppm}] = \frac{V_O(25^\circ\text{C}) - V_{O\_TC}}{V_O(25^\circ\text{C})} \times 10^6$$

where,

$$V_O(25^\circ\text{C}) = V_O \text{ at } 25^\circ\text{C}$$

$$V_{O\_TC} = V_O \text{ at } 25^\circ\text{C} \text{ after temperature cycle at } +25^\circ\text{C} \\ \text{to } -40^\circ\text{C} \text{ to } +125^\circ\text{C} \text{ and back to } +25^\circ\text{C}$$

### NOTES

#### ***Input Capacitor***

Input capacitors are not required on the ADR01/ADR02/ADR03. There is no limit for the value of the capacitor used on the input, but a 1 μF to 10 μF capacitor on the input will improve transient response in applications where the supply suddenly changes. An additional 0.1 μF in parallel will also help reducing noise from the supply.

#### ***Output Capacitor***

The ADR01/ADR02/ADR03 do not require output capacitors for stability under any load condition. An output capacitor, typically 0.1 μF, will filter out any low level noise voltage and will not affect the operation of the part. On the other hand, the load transient response can be improved with an additional 1 μF to 10 μF output capacitor in parallel. A capacitor here will act as a source of stored energy for sudden increase in load current. The only parameter that will degrade by adding an output capacitor is the turn-on time, and it depends on the size of the capacitor chosen.



## TYPICAL PERFORMANCE CHARACTERISTICS

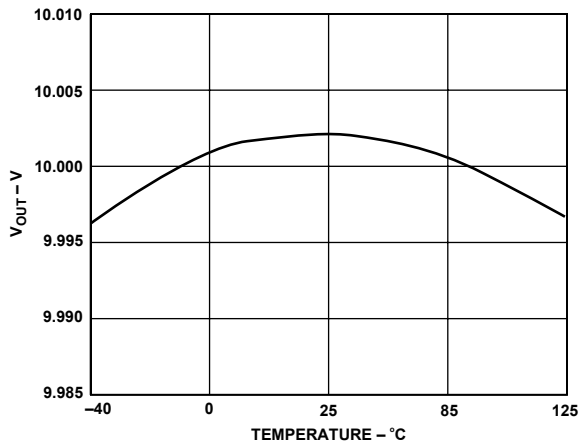


Figure 4. ADR01 Typical Output Voltage vs. Temperature

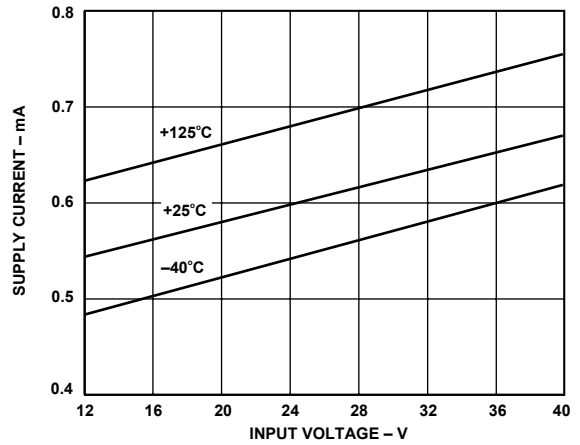


Figure 7. ADR01 Supply Current vs. Input Voltage

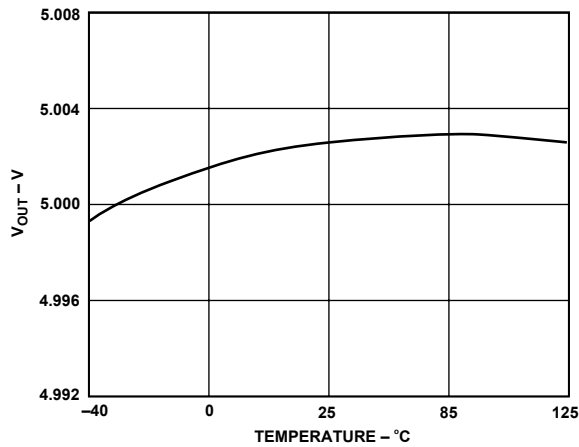


Figure 5. ADR02 Typical Output Voltage vs. Temperature

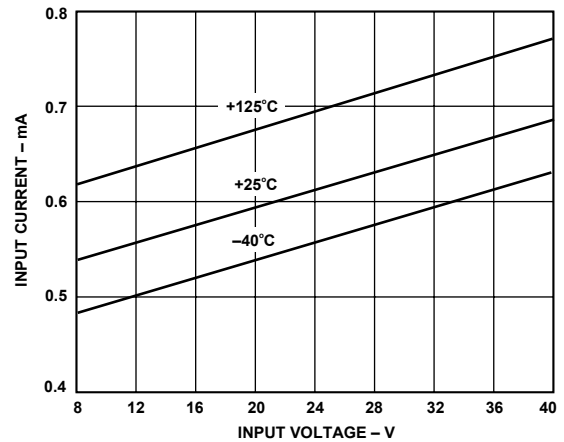


Figure 8. ADR02 Supply Current vs. Input Voltage

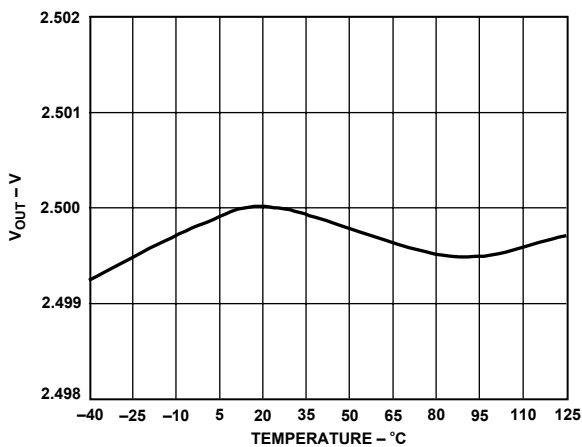


Figure 6. ADR03 Typical Output Voltage vs. Temperature

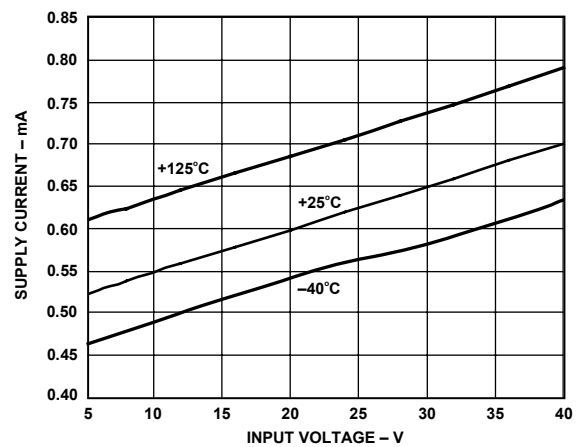


Figure 9. ADR03 Supply Current vs. Input Voltage

# ADR01/ADR02/ADR03

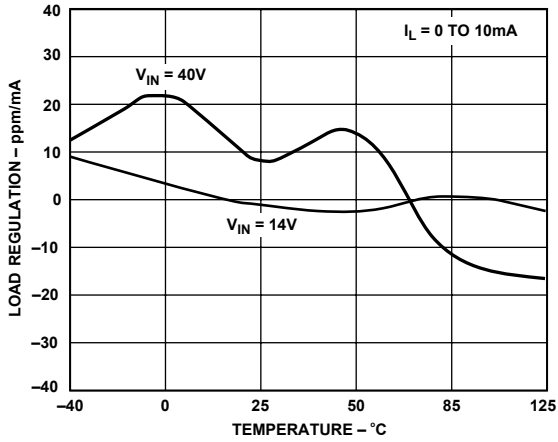


Figure 10. ADR01 Load Regulation vs. Temperature

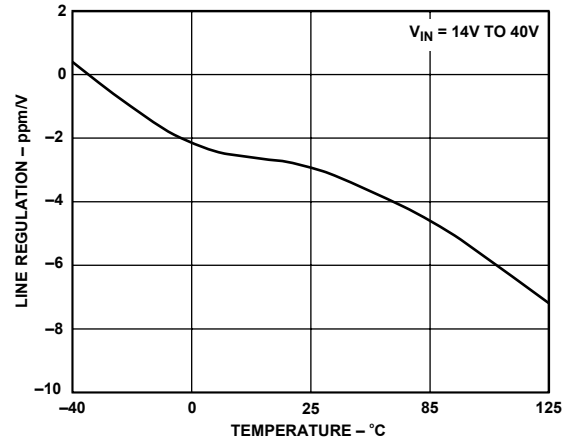


Figure 13. ADR01 Line Regulation vs. Temperature

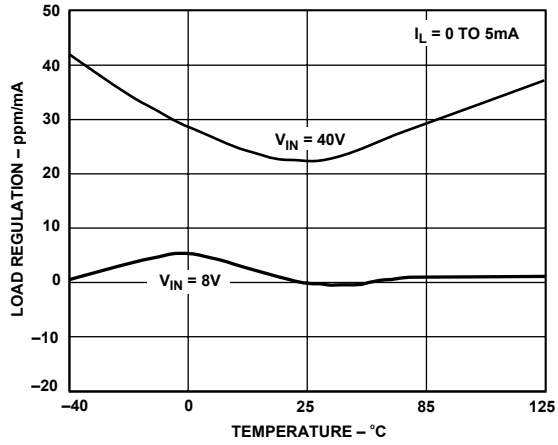


Figure 11. ADR02 Load Regulation vs. Temperature

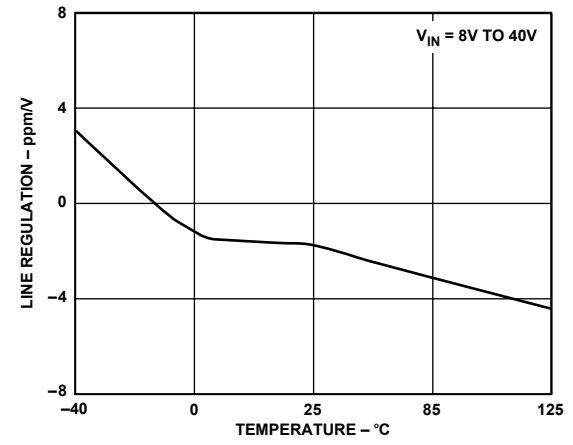


Figure 14. ADR02 Line Regulation vs. Temperature

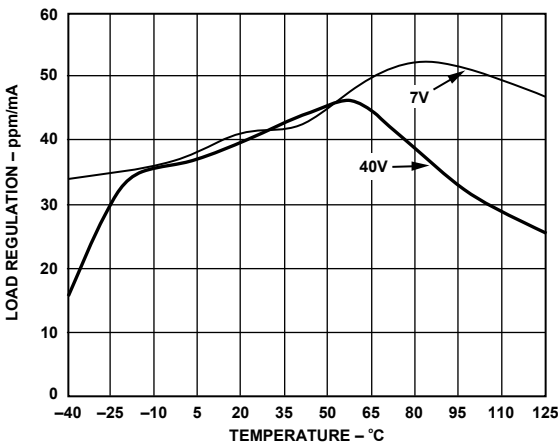


Figure 12. ADR03 Load Regulation vs. Temperature

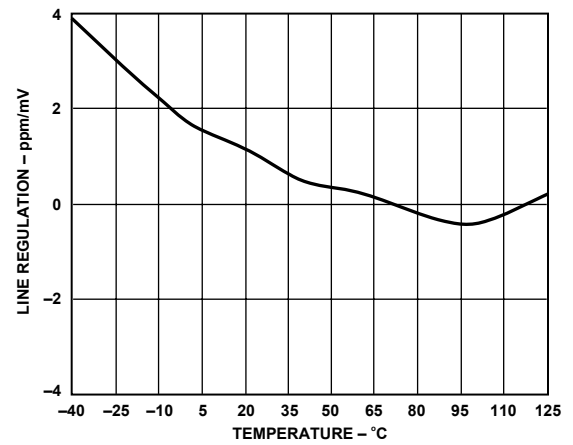


Figure 15. ADR03 Line Regulation vs. Temperature

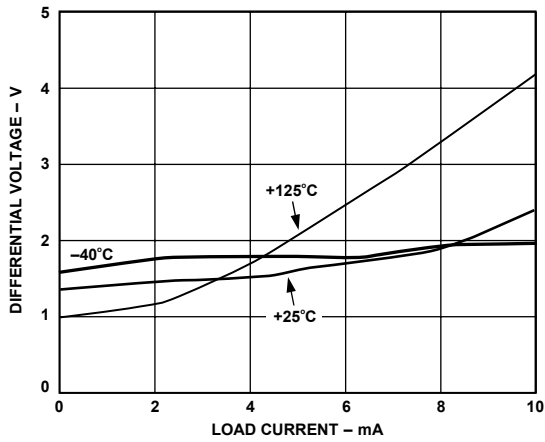


Figure 16. ADR01 Minimum Input-Output Voltage Differential vs. Load Current

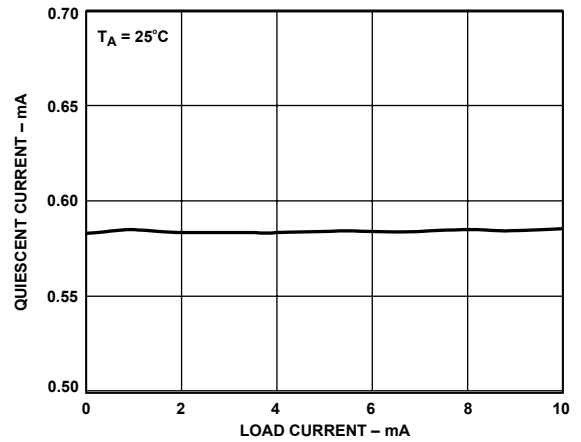


Figure 19. ADR01 Quiescent Current vs. Load Current

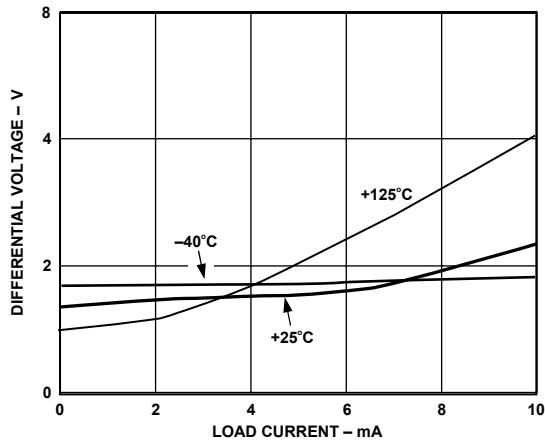


Figure 17. ADR02 Minimum Input-Output Voltage Differential vs. Load Current

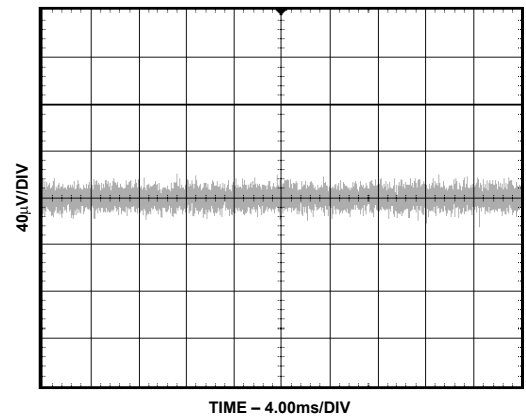


Figure 20. ADR02 Typical Noise Voltage 0.1 Hz to 10 Hz

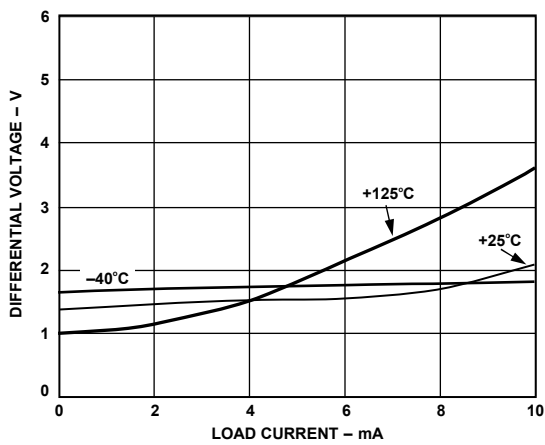


Figure 18. ADR03 Minimum Input-Output Voltage Differential vs. Load Current

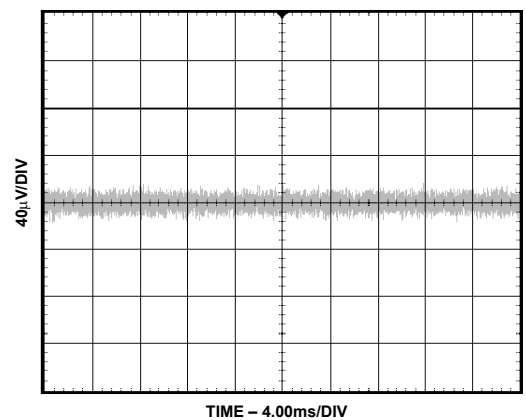


Figure 21. ADR02 Typical Noise Voltage 10 Hz to 10 KHz

# ADR01/ADR02/ADR03

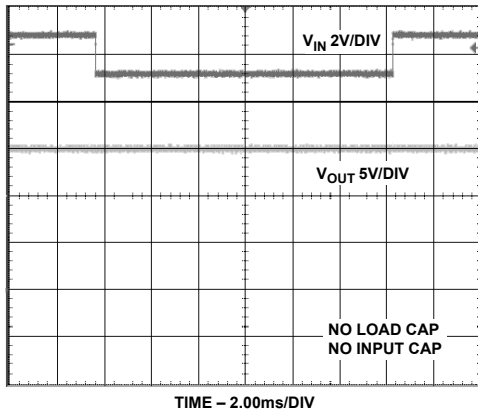


Figure 22. ADR02 Line Transient Response

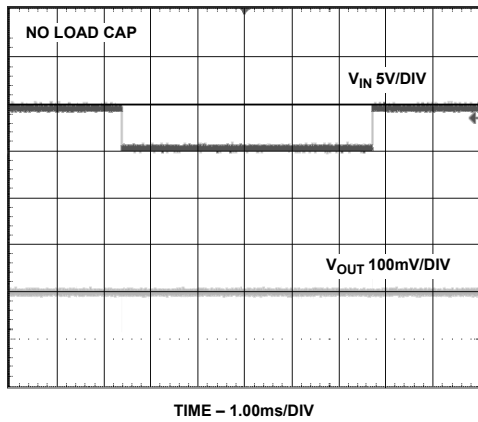


Figure 23. ADR02 Load Transient Response

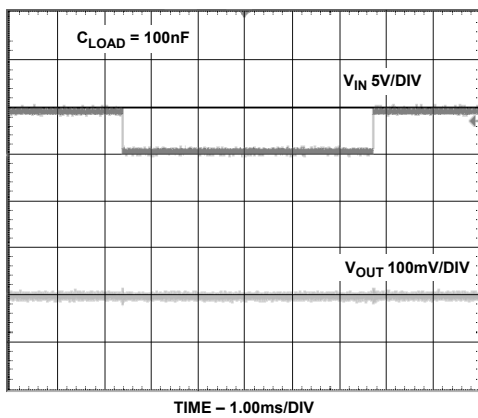


Figure 24. ADR02 Load Transient Response

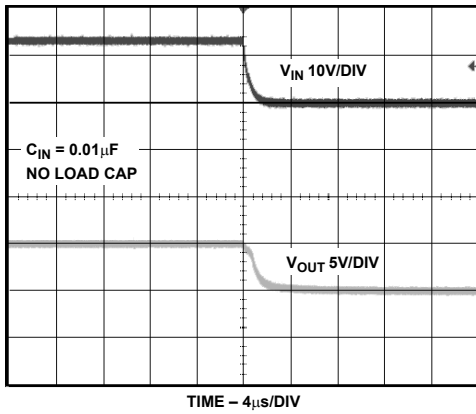


Figure 25. ADR02 Turn-Off Response

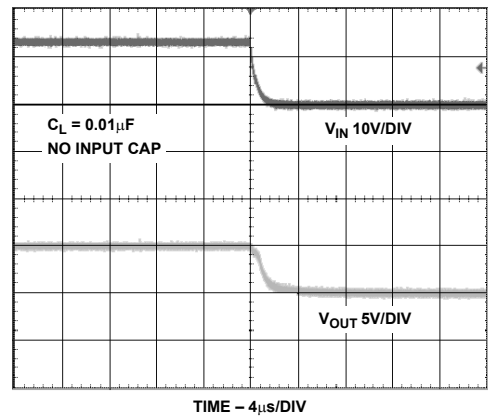


Figure 27. ADR02 Turn-Off Response

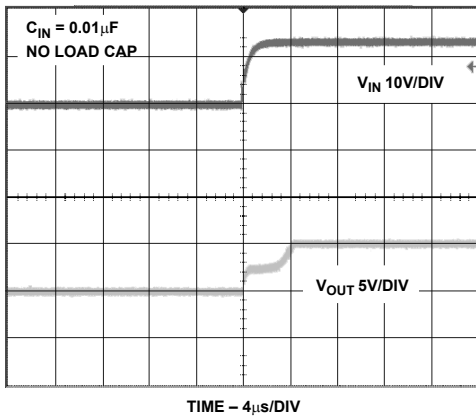


Figure 26. ADR02 Turn-On Response

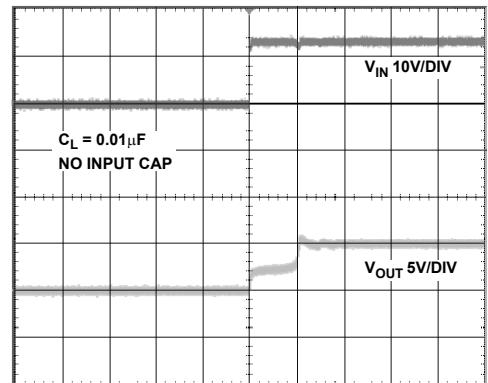


Figure 28. ADR02 Turn-On Response

# ADR01/ADR02/ADR03

## THEORY OF OPERATION

### Introduction

The ADR01/ADR02/ADR03 represent improved versions of the industry standard REF01/REF02/REF03 10 V, 5 V, and 2.5 V voltage references with higher precision, lower drift, and smaller footprint. The SOIC-8 version of the ADR01/ADR02/ADR03 is a drop-in replacement of the REF01/REF02/REF03 sockets with improved cost and performance.

The ADR01/ADR02/ADR03 are standard band gap references. The band gap cell contains two NPN transistors (Q18 and Q19) that differ in emitter area by  $2\times$ . The difference in their  $V_{BE}$  produces a Proportional to Absolute Temperature (PTAT) current in R14, when combined with the  $V_{BE}$  of Q19, produces a band gap voltage  $V_{BG}$  that is almost constant in temperature. With an internal op amp and the feedback network of R5 and R6,  $V_O$  is set precisely at 10 V, 5 V, and 2.5 V for the ADR01, ADR02, and ADR03, respectively. Precision laser trimming of the resistors and other proprietary circuit techniques are used to further enhance the initial accuracy, temperature curvature, and drift performance of the ADR01/ADR02/ADR03.

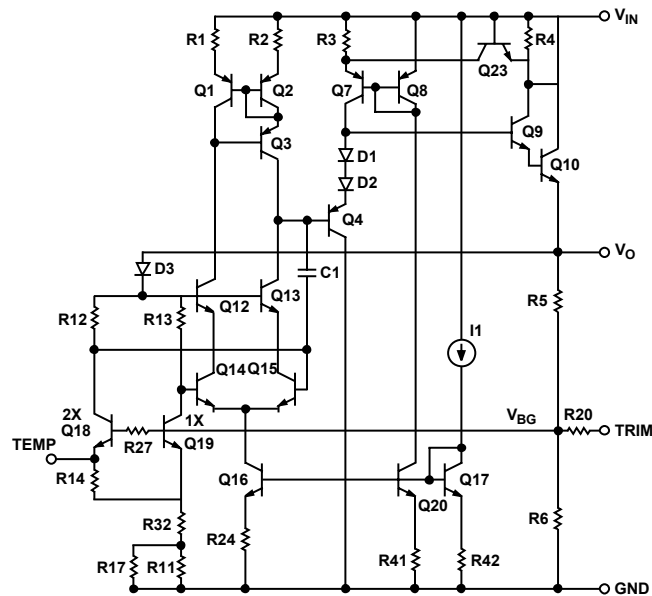


Figure 29. Simplified Schematic Diagram

The PTAT voltage is made available at the TEMP pin of the ADR01/ADR02/ADR03. It has a stable  $1.96 \text{ mV}/^\circ\text{C}$  temperature coefficient, such that users can estimate the temperature change of the device by knowing the voltage change at the TEMP pin.

### Applying the ADR01/ADR02/ADR03

The ADR01/ADR02/ADR03 can be used without any external components to achieve the specified performance. Because of the internal op amp amplifying the band gap cell to 10 V/5 V/2.5 V, power supply decoupling will help the transient response of the ADR01/ADR02/ADR03. As a result, a  $0.1 \mu\text{F}$  ceramic type decoupling capacitor should be applied as close as possible to the input and output pins of the device. An optional  $1 \mu\text{F}$  to  $10 \mu\text{F}$  bypass capacitor can also be applied at the  $V_{IN}$  node to maintain the input under transient disturbance.

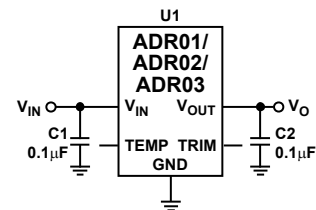


Figure 30. Basic Configuration

### OUTPUT ADJUSTMENT

The ADR01/ADR02/ADR03 trim terminal can be used to adjust the output voltage over a nominal voltage. This feature allows a system designer to trim system errors by setting the reference to a voltage other than 10 V/5 V/2.5 V. For finer adjustment, a series resistor of  $470 \text{ k}\Omega$  can be added. With the configuration shown in Figure 31, the ADR01 can be adjusted from 9.70 V to 10.05 V, the ADR02 can be adjusted from 4.95 V to 5.02 V, and the ADR03 can be adjusted from 2.3 V to 2.8 V. Adjustment of the output does not significantly affect the temperature performance of the device, provided the temperature coefficients of the resistors are relatively low.

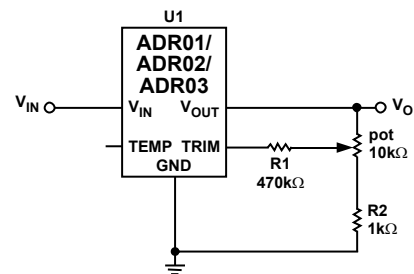


Figure 31. Optional Trim Adjustment

## TEMPERATURE MONITORING

As described previously, the ADR01/ADR02/ADR03 provide a TEMP output (Pin 3) that varies linearly with temperature. This output can be used to monitor the temperature change in the system. The voltage at  $V_{TEMP}$  is approximately 550 mV at 25°C, and the temperature coefficient is approximately 1.96 mV/°C (see Figure 32).

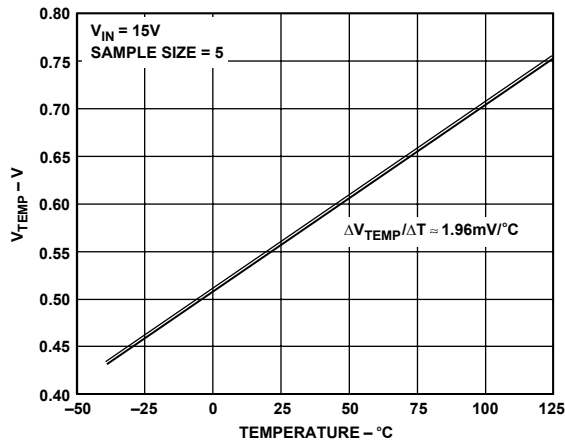


Figure 32. Voltage at TEMP Pin vs. Temperature

A voltage change of 39.2 mV at the TEMP pin corresponds to a 20°C change in temperature.

The TEMP function is provided as a convenience rather than a precise feature. Since the voltage at the TEMP node is acquired from the band gap core, current pulling from this pin will have a significant effect on  $V_{OUT}$ . Care must be taken to buffer the TEMP output with a suitable low bias current op amp, such as the AD8601, AD820, or OP1177 (all of which would result in less than a 100  $\mu$ V change in  $\Delta V_{OUT}$ ) (see Figure 33). Without buffering, even tens of microamps drawn from the TEMP pin can cause  $V_{OUT}$  to fall out of specification.

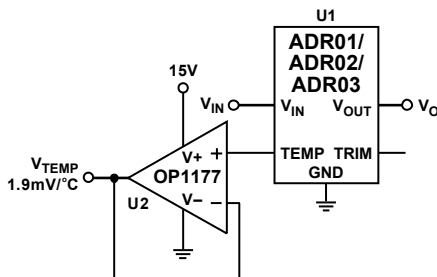


Figure 33. Temperature Monitoring

## Applications

### NEGATIVE REFERENCE

Without using any matching resistors, a negative reference can be configured as shown in Figure 34. For the ADR01, the voltage difference between  $V_{OUT}$  and GND is 10 V. Since  $V_{OUT}$  is at virtual ground, U2 will close the loop by forcing the GND pin to be the negative reference node. U2 should be a precision op amp with a low offset voltage characteristic.

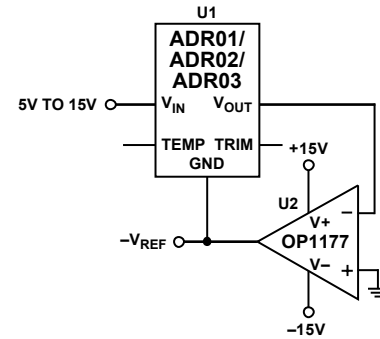


Figure 34. Negative Reference

### LOW COST CURRENT SOURCE

Unlike most references, the ADR01/ADR02/ADR03 employ an NPN Darlington in which the quiescent current remains constant with respect to the load current (see Figure 19). As a result, a current source can be configured as shown in Figure 35 where  $I_{SET} = (V_{OUT} - V_L)/R_{SET}$ .  $I_L$  is simply the sum of  $I_{SET}$  and  $I_Q$ . Although simple,  $I_Q$  varies typically from 0.55 mA to 0.65 mA, limiting this circuit to general-purpose applications.

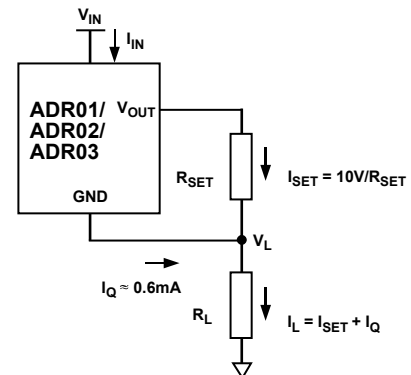


Figure 35. Low Cost Current Source





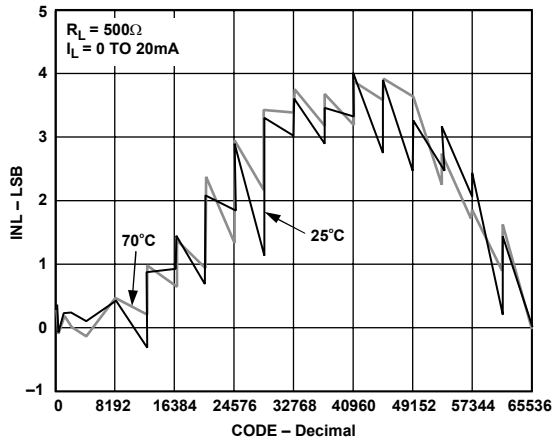


Figure 38. Result of Programmable 4–20 mA Current Transmitter

## PRECISION BOOSTED OUTPUT REGULATOR

A precision voltage output with boosted current capability can be realized with the circuit shown in Figure 39. In this circuit, U2 forces  $V_O$  to be equal to  $V_{REF}$  by regulating the turn-on of N1, thereby making the load current furnished by  $V_{IN}$ . In this configuration, a 50 mA load is achievable at  $V_{IN}$  of 15 V. Moderate heat will be generated on the MOSFET, and higher current can be achieved with a replacement of a larger device. In addition, for a heavy capacitive load with a fast edging input signal, a buffer should be added at the output to enhance the transient response.

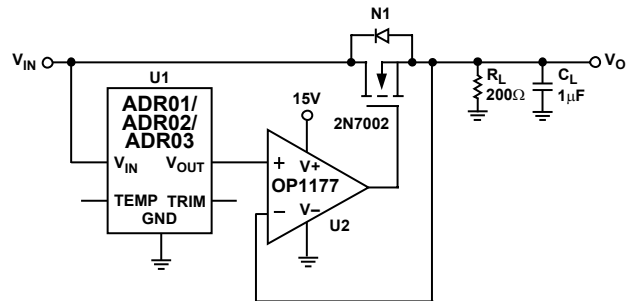


Figure 39. Precision Boosted Output Regulator

# ADR01/ADR02/ADR03

## OUTLINE DIMENSIONS

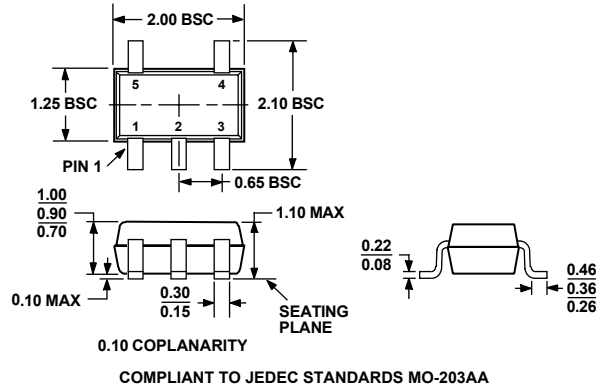


Figure 40. 5-Lead [SC70] Plastic Surface-Mount Package (KS-5)  
Dimensions Shown in Millimeters

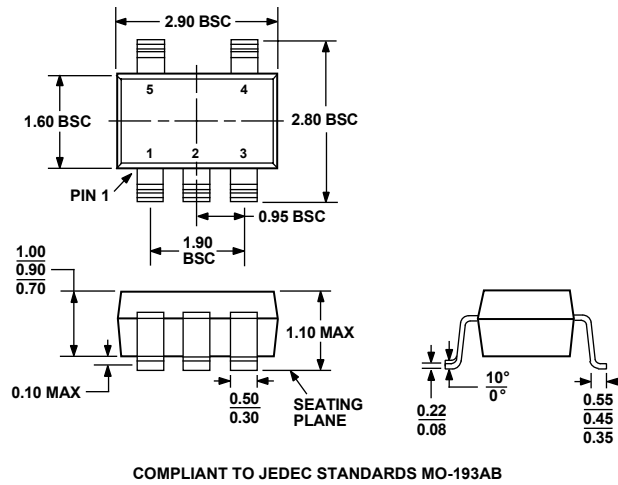
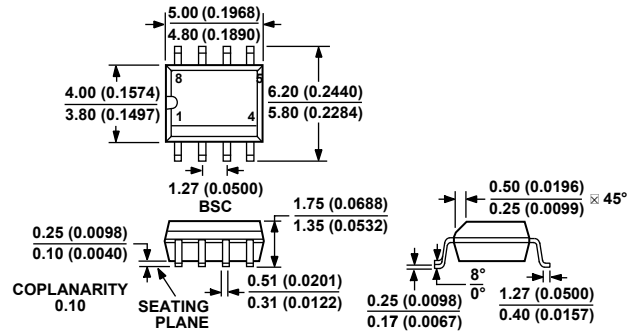


Figure 41. 5-Lead [TSOT-5] Thin Small Outline Transistor Package (UJ-5)  
Dimensions Shown in Millimeters



COMPLIANT TO JEDEC STANDARDS MS-012AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 42. 8-Lead [SOIC] Standard Small Outline Package  
(R-8)  
Dimensions Shown in Millimeters and (Inches)

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these products feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADR01/ADR02/ADR03

## ORDERING GUIDE

Table 7.

ADR01/ADR02/ADR03 Product	Output Voltage V <sub>o</sub> (V)	Initial Accuracy		Temperature Coefficient (ppm/°C)	Package Description	Package Option	Top Mark <sup>1</sup>	Number of Parts per Reel/Tray	Temperature Range (°C)
		(mV)	(%)						
ADR01AR	10	10	0.1	10	SOIC-8	R-8	ADR01		-40 to +125
ADR01AR-REEL7	10	10	0.1	10	SOIC-8	R-8	ADR01	1,000	-40 to +125
ADR01BR	10	5	0.05	3	SOIC-8	R-8	ADR01		-40 to +125
ADR01BR-REEL7	10	5	0.05	3	SOIC-8	R-8	ADR01	1,000	-40 to +125
ADR01AUJ-REEL7	10	10	0.1	25	TSOT-5	UJ-5	R8A	3,000	-40 to +125
ADR01AUJ-R2	10	10	0.1	25	TSOT-5	UJ-5	R8A	250	-40 to +125
ADR01BUJ-REEL7	10	5	0.05	9	TSOT-5	UJ-5	R8B	3,000	-40 to +125
ADR01BUJ-R2	10	5	0.05	9	TSOT-5	UJ-5	R8B	250	-40 to +125
ADR01AKS-REEL7	10	10	0.1	25	SC70	KS-5	R8A	3,000	-40 to +125
ADR01AKS-R2	10	10	0.1	25	SC70	KS-5	R8A	250	-40 to +125
ADR01BKS-REEL7	10	5	0.05	9	SC70	KS-5	R8B	3,000	-40 to +125
ADR01BKS-R2	10	5	0.05	9	SC70	KS-5	R8B	250	-40 to +125
ARR01NBC	10	5	0.05	10 (Typ)	Dice			360	-40 to +125
ADR02AR	5	5	0.1	10	SOIC-8	R-8	ADR02		-40 to +125
ADR02AR-REEL7	5	5	0.1	10	SOIC-8	R-8	ADR02	1,000	-40 to +125
ADR02BR	5	3	0.06	3	SOIC-8	R-8	ADR02		-40 to +125
ADR02BR-REEL7	5	3	0.06	3	SOIC-8	R-8	ADR02	1,000	-40 to +125
ADR02AUJ-REEL7	5	5	0.1	25	TSOT-5	UJ-5	R9A	3,000	-40 to +125
ADR02AUJ-R2	5	5	0.1	25	TSOT-5	UJ-5	R9A	250	-40 to +125
ADR02BUJ-REEL7	5	3	0.06	9	TSOT-5	UJ-5	R9B	3,000	-40 to +125
ADR02BUJ-R2	5	3	0.06	9	TSOT-5	UJ-5	R9B	250	-40 to +125
ADR02AKS-REEL7	5	5	0.1	25	SC70	KS-5	R9A	3,000	-40 to +125
ADR02AKS-R2	5	5	0.1	25	SC70	KS-5	R9A	250	-40 to +125
ADR02BKS-REEL7	5	3	0.06	9	SC70	KS-5	R9B	3,000	-40 to +125
ADR02BKS-R2	5	3	0.06	9	SC70	KS-5	R9B	250	-40 to +125
ARR02NBC	5	3	0.06	10 (Typ)	Dice			360	-40 to +125
ADR03AR	2.5	5	0.2	10	SOIC-8	R-8	ADR03		-40 to +125
ADR03AR-REEL7	2.5	5	0.2	10	SOIC-8	R-8	ADR03	1,000	-40 to +125
ADR03BR	2.5	2.5	0.1	3	SOIC-8	R-8	ADR03		-40 to +125
ADR03BR-REEL7	2.5	2.5	0.1	3	SOIC-8	R-8	ADR03	1,000	-40 to +125
ADR03AUJ-REEL7	2.5	5	0.2	25	TSOT-5	UJ-5	RFA	3,000	-40 to +125
ADR03AUJ-R2	2.5	5	0.2	25	TSOT-5	UJ-5	RFA	250	-40 to +125
ADR03BUJ-REEL7	2.5	2.5	0.1	9	TSOT-5	UJ-5	RFB	3,000	-40 to +125
ADR03BUJ-R2	2.5	2.5	0.1	9	TSOT-5	UJ-5	RFB	250	-40 to +125
ADR03AKS-REEL7	2.5	5	0.2	25	SC70	KS-5	RFA	3,000	-40 to +125
ADR03AKS-R2	2.5	5	0.2	25	SC70	KS-5	RFA	250	-40 to +125
ADR03BKS-REEL7	2.5	2.5	0.1	9	SC70	KS-5	RFB	3,000	-40 to +125
ADR03BKS-R2	2.5	2.5	0.1	9	SC70	KS-5	RFB	250	-40 to +125

<sup>1</sup> First line shows part number ADR0x. Second line shows A or B for the grade, with the YYMM date code. Third line shows the lot number.