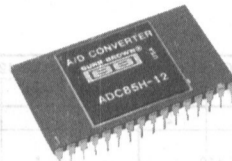


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**ADC84
ADC85H
ADC87H**

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- INDUSTRY STANDARD 12-BIT A/D CONVERTERS
- COMPLETE WITH CLOCK AND INPUT BUFFER
- HIGH SPEED CONVERSION: 10 μ s (max)
- REDUCED CHIP COUNT—HIGH RELIABILITY
- LOWER POWER DISSIPATION: 450mW (typ)
- $\pm 0.012\%$ max LINEARITY ERROR
- THREE TEMPERATURE RANGES:
0°C to +70°C — ADC84
-25°C to +85°C — ADC85H
-55°C to +125°C — ADC87H
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- PARALLEL AND SERIAL OUTPUTS
- ± 12 V OR ± 15 V POWER SUPPLY OPERATION
- HERMETIC 32-PIN CERAMIC SIDE-BRAZED DIP

DESCRIPTION

ADC84, ADC85H, and ADC87H analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 32-pin hermetic side-brazed package.

They are complete with internal reference and input buffer amplifier. Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ± 2.5 V, ± 5 V, ± 10 V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than $\pm 0.012\%$ ($\pm 1/2$ LSB).

The fast 10 μ s conversion speed for 12-bit resolution makes these ADCs excellent for a wide range of applications where system throughput sampling rates of 100kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are CMOS/TTL-compatible. Power supply voltages are ± 12 VDC or ± 15 VDC and +5VDC.

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PDS-714A

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SPECIFICATIONS

ELECTRICAL

Specified at +25°C and rated supplies, unless otherwise noted.

PARAMETER	ADC84KG-12 ⁽¹⁾			ADC85H-12			ADC87H-12			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12							Bits
ANALOG INPUTS										
Voltage Ranges: Bipolar		±2.5, ±5, ±10								V
Unipolar		0 to +5, 0 to +10								V
Impedance (Direct Input): 0 to +5V, ±2.5V	2.45	2.5	2.55	*	*	*	*	*	*	kΩ
0 to +10V, ±5V	4.9	5	5.1	*	*	*	*	*	*	kΩ
±10V	9.8	10	10.2	*	*	*	*	*	*	kΩ
Buffer Amplifier: Impedance	100			*	*	*	*	*	*	MΩ
Bias Current		50		*	*	*	*	*	*	nA
Settling Time to 0.01% for 20V Step ⁽²⁾		2		*	*	*	*	*	*	μs
DIGITAL INPUTS⁽³⁾										
Convert Command		Positive pulse 50ns (min), trailing edge initiates conversion								
Logic Loading		1								TTL Load
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error ⁽⁴⁾		±0.1	±0.25	*	*	*	*	*	*	%
Offset Error ⁽⁵⁾ : Unipolar		±0.05	±0.2	*	*	*	*	*	*	% of FSR ⁽⁶⁾
Bipolar		±0.1	±0.25	*	*	*	*	*	*	% of FSR
Linearity Error ⁽⁶⁾			±0.012	*	*	*	*	*	*	% of FSR
Inherent Quantization Error			±0.5	*	*	*	*	*	*	LSB
Differential Linearity Error			±0.5	*	*	*	*	*	*	LSB
No Missing Codes Temperature Range	0		+70	-25		+85	-55		+125	°C
POWER SUPPLY SENSITIVITY										
Gain and Offset: ±15V		±0.004		*	*	*	*	*	*	% of FSR/%V _s
+5V		±0.001		*	*	*	*	*	*	% of FSR/%V _s
DRIFT										
Gain			±30	*	±15	*	±15	*	±15	ppm/°C
Offset: Unipolar		±3		±3	±15		±10		±10	ppm of FSR/°C
Bipolar			±15		±7		±10		±10	ppm of FSR/°C
Linearity			±3		±2		±2		±2	ppm of FSR/°C
Monotonicity		Guaranteed		*						
CONVERSION TIME			10							μs
DIGITAL OUTPUT⁽³⁾										
(All Modes Complementary)										
Parallel Output Codes: Unipolar		CSB		*			*		*	TTL Loads
Bipolar		COB, CTC		*			*		*	TTL Loads
Output Drive		2		*			*		*	TTL Loads
Serial Data Codes (NRZ)		CSB, COB		*			*		*	TTL Loads
Output Drive		2		*			*		*	TTL Loads
Status		Logic "1" During Conversion		*			*		*	TTL Loads
Output Drive		2		*			*		*	TTL Loads
Internal Clock: Output Drive		2		*			*		*	TTL Loads
Frequency ⁽⁷⁾		1.35		*			*		*	MHz
INTERNAL REFERENCE VOLTAGE										
Reference Output	+6.2	+6.3	+6.4	*			*		*	V
Max. External Current with No Degradation			200	*			*		*	μA
Tempco of Drift			±20	±5	±10		±5	±10		ppm/°C
POWER SUPPLY REQUIREMENTS										
Rated Supply Voltages		+5, ±12 or ±15								V
Supply Ranges: V _{DD}	+4.75		+5.25	*			*		*	V
±V _{CC}	±11.4		±16.5	*			*		*	V
Supply Drain: +I _{CC}			20	*			*		*	mA
-I _{CC}			25	*			*		*	mA
I _{DD}			10	*			*		*	mA
Total Power Dissipation		450	725	*			*		*	mW
TEMPERATURE RANGE										
Specification	0		+70	-25		+85	-55		+125	°C
Operating (with Derated Specs)	-25		+85	-55		+125				°C
Storage	-65		+150	*			*		*	°C

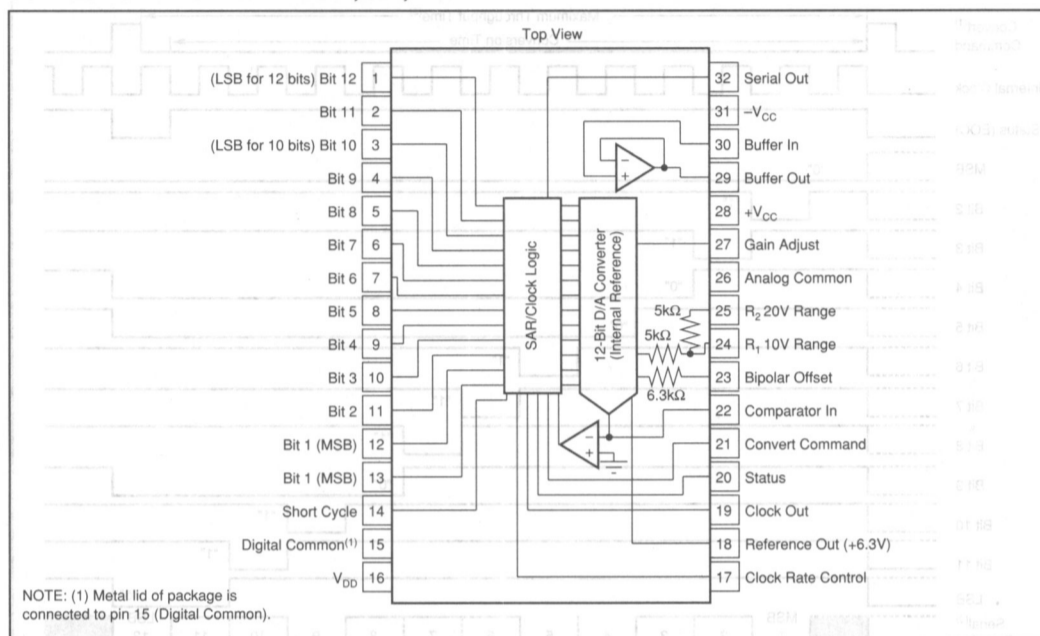
*Specification is the same as ADC84KG-12.

NOTES: (1) Model ADC84KG-10 is the same as model ADC84KG-12 except for the following: (a) Resolution: 10 bits (max), (b) Linearity Error: ±0.048% of FSR (max), (c) Conversion Time: 6μs (max), (d) Internal Clock Frequency: 1.9MHz (typ). (2) If the buffer is used, delay Convert Command until amplifier settles. (3) DTL/TTL compatible. For digital inputs Logic "0" = 0.8V (max) and Logic "1" = 2.0V (min). For digital outputs Logic "0" = 0.4V (max) and Logic "1" = 2.4V (min). (4) Adjustable to zero. (5) FSR means Full Scale Range. (6) The error shown is the same as ±1/2LSB max linearity error in % of FSR. (7) Internal clock is externally adjustable.



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CONNECTION DIAGRAM — ADC84, 85H, 87H



ORDERING INFORMATION

MODEL	RESOLUTION (Bits)	TEMPERATURE RANGE
ADC84KG-10	10	0°C to +70°C
ADC84KG-12	12	0°C to +70°C
ADC85H-12	12	-25°C to +85°C
ADC87H-12	12	-55°C to +125°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC84KG-10	Case Ceramic DIP	172-5
ADC84KG-12	Case Ceramic DIP	172-5
ADC85H-12	32-Pin Side-brazed	172-5
ADC87H-12	32-Pin Side-brazed	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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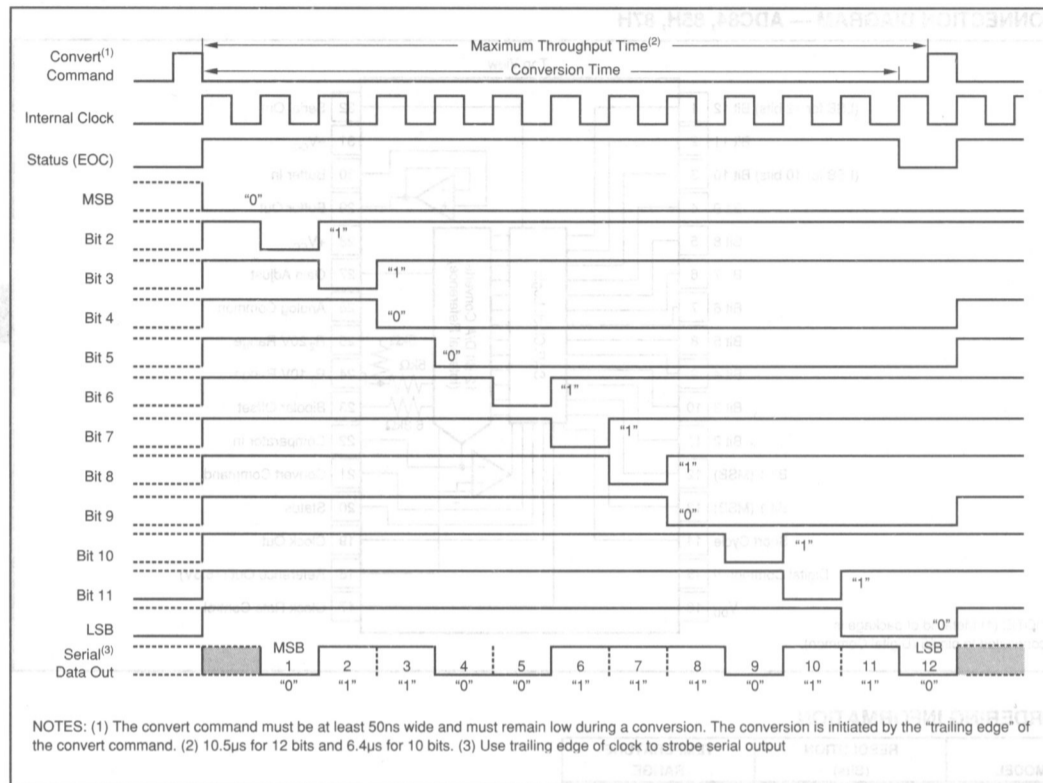


FIGURE 1. Timing Diagram.