50 MHz, 80 dB Demodulating Logarithmic Amplifier with Limiter Output

AD606

FEATURES

Logarithmic Amplifier Performance
- **–75 dBm to +5 dBm Dynamic Range**
- **≤1.5 nV/√Hz Input Noise**
- **Usable to >50 MHz**
- **37.5 mV/dB Voltage Output**
- **On-Chip Low-Pass Output Filter**

Limiter Performance
- **±1 dB Output Flatness over 80 dB Range**
- **±3° Phase Stability at 10.7 MHz over 80 dB Range**
- **Adjustable Output Amplitude**

Low Power
- **+5 V Single Supply Operation**
- **65 mW Typical Power Consumption**
- **CMOS Compatible Power-Down to 325 μW typ**
- **<5 μs Enable/Disable Time**

APPLICATIONS

Ultrasound and Sonar Processing
Phase-Stable Limiting Amplifier to 100 MHz
Received Signal Strength Indicator (RSSI)
Wide Range Signal and Power Measurement

PRODUCT DESCRIPTION

The AD606 is a complete, monolithic logarithmic amplifier using a 9-stage "successive-detection" technique. It provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation low-pass filter and provides a loadable output voltage of +0.1 V dc to +4 V dc. The logarithmic scaling is such that the output is +0.5 V for a sinusoidal input of –75 dBm and +3.5 V at an input of +5 dBm; over this range the logarithmic linearity is typically within ±0.4 dB. All scaling parameters are proportional to the supply voltage.

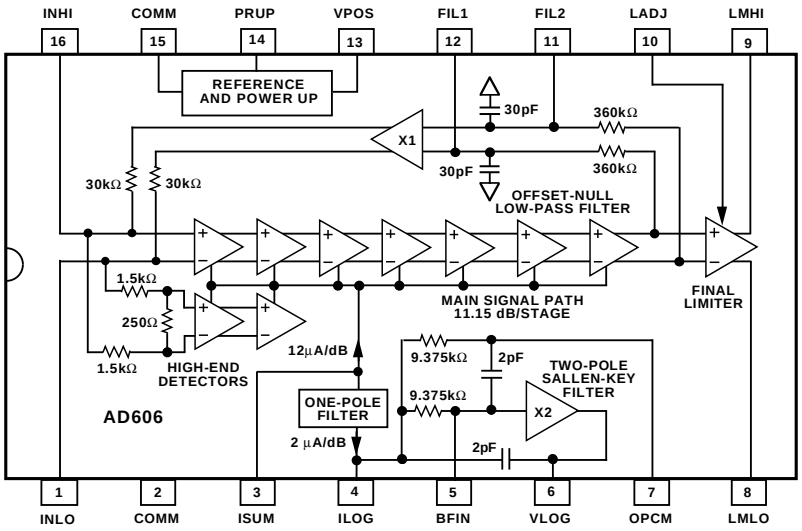
The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90 dB of conversion range. A second low-pass filter automatically nulls the input offset of the first stage down to the submicrovolt level. Adding external capacitors to both filters allows operation at input frequencies as low as a few hertz.

The AD606's limiter output provides a hard-limited signal output as a differential current of ±1.2 mA from open-collector outputs. In a typical application, both of these outputs are loaded by 200 Ω resistors to provide a voltage gain of more than 90 dB from the input. Transition times are 1.5 ns, and the phase is stable to within ±3° at 10.7 MHz for signals from –75 dBm to +5 dBm.

The logarithmic amplifier operates from a single +5 V supply and typically consumes 65 mW. It is enabled by a CMOS logic level voltage input, with a response time of <5 μs. When disabled, the standby power is reduced to <1 mW within 5 μs.

The AD606J is specified for the commercial temperature range of 0°C to +70°C and is available in 16-pin plastic DIPs or SOICs. Consult the factory for other packages and temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



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AD606—SPECIFICATIONS (@ T_A = +25°C and supply = +5 V unless otherwise noted; dBm assumes 50 Ω)

Model / Parameter	Conditions	AD606J Min	AD606J Typ	AD606J Max	Units
SIGNAL INPUT					
Log Amp f_{MAX}	AC Coupled; Sinusoidal Input		50		MHz
Limiter f_{MAX}	AC Coupled; Sinusoidal Input		100		MHz
Dynamic Range			80		dB
Input Resistance	Differential Input	500	2,500		Ω
Input Capacitance	Differential Input		2		pF
SIGNAL OUTPUT					
Limiter Flatness	–75 dBm to +5 dBm Input Signal at 10.7 MHz With Pin 9 to V_{POS} via a 200 Ω Resistor and Pin 8 to V_{POS} via a 200 Ω Resistor	–1.5		+1.5	dB
Output Current	At Pins 8 or 9, Proportional to V_{POS}, LADJ Grounded		1.2		mA
	LADJ Open Circuited		0.48		mA
Phase Variation with Input Level	–75 dBm to +5 dBm Input Signal at 10.7 MHz		±3		°
LOG (RSSI) OUTPUT					
Nominal Slope	At 10.7 MHz; (0.0075 × V_{POS})/dB		37.5		mV/dB
	At 45 MHz		35		mV/dB
Slope Accuracy	Untrimmed at 10.7 MHz	–15	±5	+15	%
Intercept	Sinusoidal Input; Independent of V_{POS}		–88.33		dBm
Logarithmic Conformance	–75 dBm to +5 dBm Input Signal at 10.7 MHz	–1.5	0.4	+1.5	dB
Nominal Output	Input Level = –75 dBm		0.5		V
	Input Level = –35 dBm		2		V
	Input Level = +5 dBm		3.5		V
Accuracy over Temperature	After Calibration at –35 dBm at 10.7 MHz T_{MIN} to T_{MAX}	–3		3	dB
Video Response Time	From Onset of Input Signal Until Output Reaches 95% of Final Value		400		ns
POWER-DOWN INTERFACE					
Power-Up Response Time	Time Delay Following HI Transition Until Device Meets Full Specifications AC Coupled with 100 pF Coupling Capacitors		3.5		µs
Input Bias Current	Logical HI Input (See Figure 12)		1		nA
	Logical LO Input		4		µA
POWER SUPPLY					
Operating Range		4.5		5.5	V
Powered-Up Current	Zero Signal Input		13		mA
	T_{MIN} to T_{MAX}		13	20	mA
Powered-Down Current	T_{MIN} to T_{MAX}		65	200	µA

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

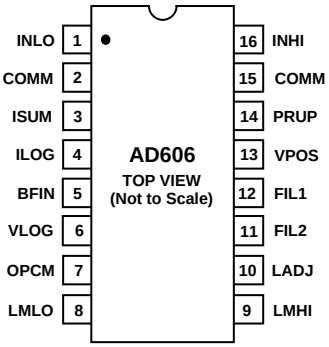
Supply Voltage V_{POS} . . . . . +9 V
Internal Power Dissipation[2] . . . . . 600 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
16-Pin Plastic DIP Package: θ_{JA} = 85°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Option
AD606JN	0°C to +70°C	16-Pin Plastic DIP (N-16)
AD606JR	0°C to +70°C	16-Pin Narrow-Body SOIC (R-16A)

PIN DESCRIPTION
Plastic DIP (N)
and
Small Outline (R)
Packages



PIN FUNCTIONS

Pin	Mnemonic	Function
1	INLO	DIFFERENTIAL RF INPUT –75 dBm to +5 dBm, Inverting, AC Coupled.
2	COMM	POWER SUPPLY COMMON Connect to Ground.
3	ISUM	LOG DETECTOR SUMMING NODE
4	ILOG	LOG CURRENT OUTPUT Normally No Connection; 2 μA/dB Output Current.
5	BFIN	BUFFER INPUT Optionally Used to Realize Low Frequency Post-Demodulation Filters.
6	VLOG	BUFFERED LOG OUTPUT 37.5 mV/dB (100 mV to 4.5 V).
7	OPCM	OUTPUT COMMON Connect to Ground.
8	LMLO	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current. Open Collector Output Must Be "Pulled" Up to VPOS with R ≤ 400 Ω.
9	LMHI	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current. Open Collector Output Must Be "Pulled" Up to VPOS with R ≤ 400 Ω.
10	LADJ	LIMITER LEVEL ADJUSTMENT Optionally Used to Adjust Limiter Output Current.
11	FIL1	OFFSET LOOP LOW-PASS FILTER Normally No Connection; a Capacitor Between FIL1 and FIL2 May Be Added to Lower the Filter Cutoff Frequency.
12	FIL2	OFFSET LOOP LOW-PASS FILTER Normally No Connection; See Above.
13	VPOS	POSITIVE SUPPLY Connect to +5 V at 13 mA.
14	PRUP	POWER UP CMOS (5 V) Logical High = Device On (≈ 65 mW). CMOS (0 V) Logical Low = Device Off (≈ 325 μW).
15	COMM	POWER SUPPLY COMMON Connect to Ground.
16	INHI	DIFFERENTIAL RF INPUT –75 dBm to +5 dBm, Noninverting, AC Coupled.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD606 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

INPUT LEVEL CONVENTIONS

RF logarithmic amplifiers usually have their input specified in "dBm," meaning "decibels with respect to 1 mW." Unfortunately, this is not precise for several reasons.

1. Log amps respond not to power but to voltage. In this respect, it would be less ambiguous to use "dBV" (decibels referred to 1 V) as the input metric. Also, power is dependent on the rms (root mean-square) value of the signal, while log amps are not inherently rms responding.
2. The response of a demodulating log amp depends on the waveform. Convention assumes that the input is sinusoidal. However, the AD606 is capable of accurately handling any input waveform, including ac voltages, pulses and square waves, Gaussian noise, and so on. See the AD640 data sheet, which covers the effect of waveform on logarithmic intercept, for more information.
3. The impedance in which the specified power is measured is not always stated. In the log amp context it is invariably assumed to be 50 Ω. Thus, 0 dBm means "1 mW rms in 50 Ω," and corresponds to an rms voltage of $\sqrt{(1\,mW \times 50\ \Omega)}$, or 224 mV.

Popular convention requires the use of dBm to simplify the comparison of log amp specifications. Unless otherwise stated, sinusoidal inputs expressed as dBm in 50 Ω are used to specify the performance of the AD606 throughout this data sheet. We will also show the corresponding rms voltages where it helps to clarify the specification. Noise levels will likewise be given in dBm; the response to Gaussian noise is 0.5 dB higher than for a sinusoidal input of the same rms value.

Note that dynamic range, being a simple ratio, is always specified simply as "dB", and the slope of the logarithmic transfer function is correctly specified as "mV/dB," NOT as "mV/dBm."

LOGARITHMIC SLOPE AND INTERCEPT

A generalized logarithmic amplifier having an input voltage V_{IN} and output voltage V_{LOG} must satisfy a transfer function of the form

$$V_{LOG} = V_Y \log_{10} (V_{IN}/V_X)$$

where, in the case of the AD606, the voltage V_{IN} is the difference between the voltages on pins INHI and INLO, and the voltage V_{LOG} is that measured at the output pin VLOG. V_Y and V_X are fixed voltages that determine the slope and intercept of the logarithmic amplifier, respectively. These parameters are inherent in the design of a particular logarithmic amplifier, although may be adjustable, as in the AD606. When $V_{IN} = V_X$, the logarithmic argument is one, hence the logarithm is zero. V_X is, therefore, called the logarithmic *intercept* voltage because the output voltage V_{LOG} crosses zero for this input. The slope voltage V_Y is can also be interpreted as the "volts per decade" when using base-10 logarithms as shown here.

Note carefully that V_{LOG} and VLOG in the above paragraph (and elsewhere in this data sheet) are different. The first is a voltage; the second is a pin designation.

This equation suggests that the input V_{IN} is a dc quantity, and, if V_X is positive, that V_{IN} must likewise be positive, since the logarithm of a negative number has no simple meaning. In fact, in the AD606, *the response is independent of the sign of* V_{IN} because of the particular way in which the circuit is built. This is part of the demodulating nature of the amplifier, which results in an alternating input voltage being transformed into a quasi-dc (rectified and filtered) output voltage.

The single supply nature of the AD606 results in common-mode level of the inputs INHI and INLO being at about +2.5 V (using the recommended +5 V supply). In normal ac operation, this bias level is developed internally and the input signal is coupled in through dc blocking capacitors. Any residual dc offset voltage in the first stage limits the logarithmic accuracy for small inputs. In ac operation, this offset is automatically and continuously nulled via a feedback path from the last stage, provided that the pins INHI and INLO are not shorted together, as would be the case if transformer coupling were used for the signal.

While any logarithmic amplifier must eventually conform to the basic equation shown above, which, with appropriate elaboration, can also fully account for the effect of the signal waveform on the effective intercept,[1] it is more convenient in RF applications to use a simpler expression. This simplification results from first, assuming that the input is always sinusoidal, and second, using a decibel representation for the input level. The standard representation of RF levels is (incorrectly, in a log amp context) in terms of power, specifically, decibels above 1 milliwatt (dBm) with a presumed impedance level of 50 Ω. That being the case, we can rewrite the transfer function as

$$V_{LOG} = V_Y (P_{IN} - P_X)$$

where it must be understood that P_{IN} means the sinusoidal input power level in a 50 Ω system, expressed in dBm, and P_X is the intercept, also expressed in dBm. In this case, P_{IN} and P_X are simple, dimensionless numbers. (P_X is sometimes called the "logarithmic offset," for reasons which are obvious from the above equation.) V_Y is still defined as the logarithmic slope, usually specified as so many millivolts per decibel, or mV/dB.

In the case of the AD606, the slope voltage, V_Y, is nominally 750 mV when operating at V_{POS} = 5 V. This can also be expressed as 37.5 mV/dB or 750 mV/decade; thus, the 80 dB range equates to 3 V. Figure 1 shows the transfer function of the AD606. The slope is closely proportional to V_{POS}, and can more generally be stated as $V_Y = 0.15 \times V_{POS}$. Thus, in those applications where the scaling must be independent of supply voltage, this must be stabilized to the required accuracy. In applications where the output is applied to an A/D converter, the reference

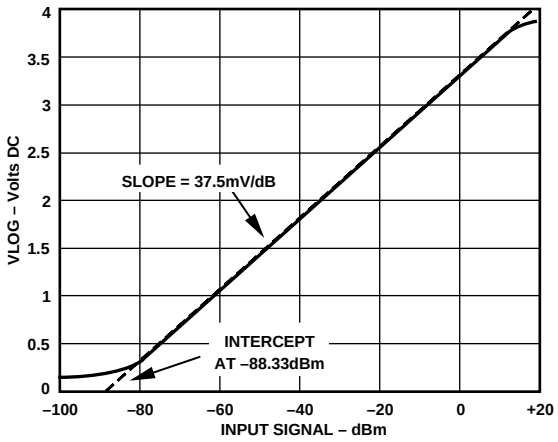


Figure 1. Nominal Transfer Function

[1]See, for example, the AD640 data sheet, which is published in Section 3 of the *Special Linear Reference Manual* or Section 9.3 of the 1992 *Amplifier Applications Guide.*

for that converter should be a fractional part of V_{POS}, if possible. The slope is essentially independent of temperature.

The intercept P_X is essentially independent of either the supply voltage or temperature. However, the AD606 is not factory calibrated, and both the slope and intercept may need to be externally adjusted. Following calibration, the conformance to an ideal logarithmic law will be found to be very close, particularly at moderate frequencies (see Figure 14), and still acceptable at the upper end of the frequency range (Figure 15).

CIRCUIT DESCRIPTION

Figure 2 is a block diagram of the AD606, which is a complete logarithmic amplifier system in monolithic form. It uses a total of nine limiting amplifiers in a "successive detection" scheme to closely approximate a logarithmic response over a total dynamic range of 90 dB (Figure 2). The signal input is differential, at nodes INHI and INLO, and will usually be sinusoidal and ac coupled. The source may be either differential or single-sided; the input impedance is about 2.5 kΩ in parallel with 2 pF. Seven of the amplifier/detector stages handle inputs from –80 dBm (32 μV rms) up to about –14 dBm (45 mV rms). The noise floor is about –83 dBm (18 μV rms). Another two stages receive the input attenuated by 22.3 dB, and respond to inputs up to +10 dBm (707 mV rms). The gain of each of these stages is 11.15 dB and is accurately stabilized over temperature by a precise biasing system.

The detectors provide full-wave rectification of the alternating signal present at each limiter output. Their outputs are in the form of currents, proportional to the supply voltage. Each cell incorporates a low-pass filter pole, as the first step in recovering the average value of the demodulated signal, which contains appreciable energy at even harmonics of the input frequency. A further real pole can be introduced by adding a capacitor between the summing node ISUM and VPOS. The summed detector output currents are applied to a 6:1 reduction current mirror. Its output at ILOG is scaled 2 μA/dB, and is converted to voltage by an internal load resistor of 9.375 kΩ between

ILOG and OPCM (output common, which is usually grounded). The nominal slope at this point is 18.75 mV/dB (375 mV/ decade).

In applications where V_{LOG} is taken to an A/D converter which allows the use of an external reference, this reference input should also be connected to the same +5 V supply. The power supply voltage may be in the range +4.5 V to +5.5 V, providing a range of slopes from nominally 33.75 mV/dB (675 mV/ decade) to 41.25 mV/dB (825 mV/decade).

A buffer amplifier, having a gain of two, provides a final output scaling at V_{LOG} of 37.5 mV/dB (750 mV/decade). This low-impedance output can run from close to ground to over +4 V (using the recommended +5 V supply) and is tolerant of resistive and capacitive loads. Further filtering is provided by a conjugate pole pair, formed by internal capacitors which are an integral part of the output buffer. The corner frequency of the overall filter is 2 MHz, and the 10%–90% rise time is 150 ns. Later, we will show how the slope and intercept can be altered using simple external adjustments. The direct buffer input BFIN is used in these cases.

The last limiter output is available as complementary currents from open collectors at pins LMHI and LMLO. These currents are each 1.2 mA typical with LADJ grounded and may be converted to voltages using external load resistors connected to VPOS; typically, a 200 Ω resistor is used on just one output. The voltage gain is then over 90 dB, resulting in a hard-limited output for all input levels down to the noise floor. The phasing is such that the voltage at LMHI goes high when the input (INHI to INLO) is positive. The overall delay time from the signal inputs to the limiter outputs is 8 ns. Of particular importance is the phase stability of these outputs versus input level. At 50 MHz, the phase typically remains within ±4° from –70 dBm to +5 dBm. The rise time of this output (essentially a square wave) is about 1.2 ns, resulting in clean operation to more than 70 MHz.

Offset-Control Loop

The offset-control loop nulls the input offset voltage, and sets up the bias voltages at the input pins INHI and INLO. A full understanding of this offset-control loop is useful, particularly when using larger input coupling capacitors and an external filter capacitor to lower the minimum acceptable operating frequency. The loop's primary purpose is to extend the lower end

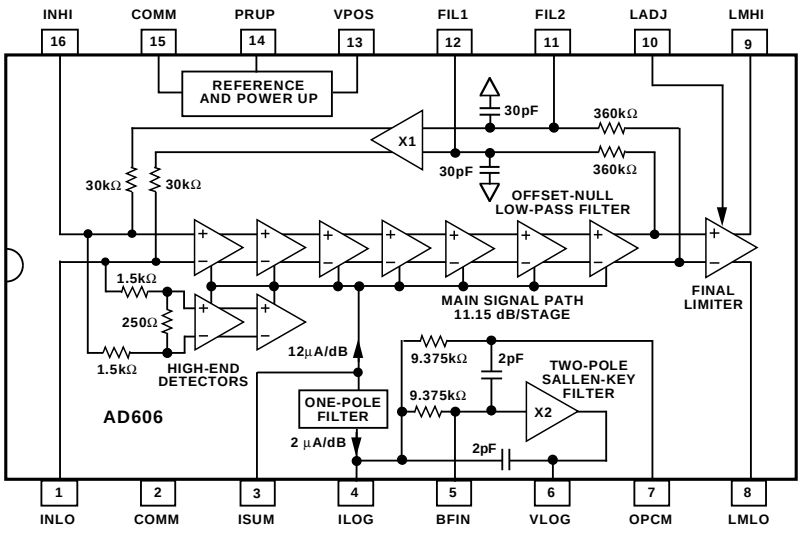


Figure 2. AD606 Simplified Block Diagram

of the dynamic range in the case where the offset voltage of the first stage should be high enough to cause later stages to prematurely enter limiting, because of the high dc gain (about 8000) of the main amplifier system. For example, an offset voltage of only 20 μV would become 160 mV at the output of the last stage in the main amplifier (before the final limiter section), driving the last stage well into limiting. In the absence of noise, this limiting would simply result in the logarithmic output ceasing to become any lower below a certain signal level at the input. The offset would also degrade the logarithmic conformance in this region. In practice, the finite noise of the first stage also plays a role in this regard, even if the dc offset were zero.

Figure 3 shows a representation of this loop, reduced to essentials. The figure closely corresponds to the internal circuitry, and correctly shows the input resistance. Thus, the forward gain of the main amplifier section is 7 × 11.15 dB, but the loop gain is lowered because of the attenuation in the network formed by

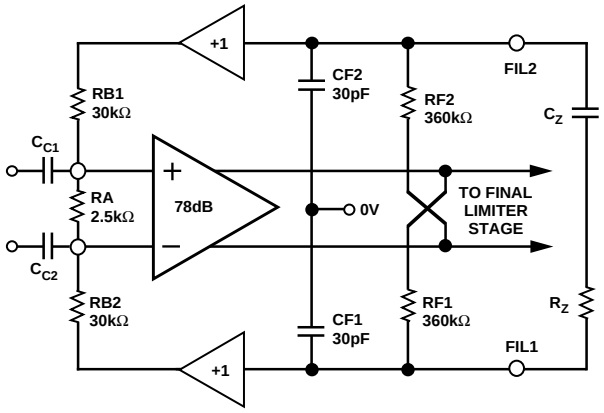


Figure 3. Offset Control Loop

RB1 and RB2 and the input resistance RA. The connection polarity is such as to result in negative feedback, which reduces the input offset voltage by the dc loop gain, here about 50 dB, that is, by a factor of about 316. We use a *differential* representation, because later we will examine the consequences to the power-up response time in the event that the ac coupling capacitors C_{C1} and C_{C2} do not exactly match. Note that these capacitors, as well as forming a high-pass filter to the signal in the forward path, also introduce a pole in the feedback path.

Internal resistors RF1 and RF2 in conjunction with grounded capacitors CF1 and CF2 form a low-pass filter at 15 kHz. This frequency can optionally be lowered by the addition of an external capacitor C_Z, and in some cases a series resistor R_Z. This, in conjunction with the low-pass section formed at the input coupling, results in a two-pole high-pass response, falling of at 40 dB/decade below the corner frequency. The damping factor of this filter depends on the ratio C_Z/C_C (when $C_Z >> C_F$) and also on the value of R_Z.

The inclusion of this control loop has no effect on the high frequency response of the AD606. Nor does it have any effect on the low frequency response when the input amplitude is substantially above the input offset voltage.

The loop's effect is felt only at the lower end of the dynamic range, that is, from about 80 dBm to –70 dBm, and when the signal frequency is near the lower edge of the passband. Thus, the small signal results which are obtained using the suggested model are not indicative of the ac response at moderate to high signal levels. Figure 4 shows the response of this model for the default case (using C_C = 100 pF and C_Z = 0) and with C_Z = 150 pF. In general, a *maximally flat ac* response occurs when C_Z is roughly twice C_C (making due allowance for the internal 30 pF capacitors). Thus, for audio applications, one can use C_C = 2.7 μF and C_Z = 4.7 μF to achieve a high-pass corner (–3 dB) at 25 Hz.

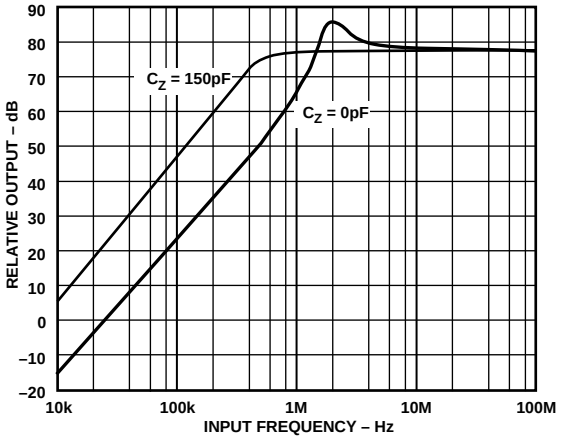


Figure 4. Frequency Response of Offset Control Loop for C_Z = 0 pF and C_Z = 150 pF (C_C = 100 pF)

However, the maximally flat ac response is not optimal in two special cases. First, where the RF input level is rapidly pulsed, the fast edges will cause the loop filter to ring. Second, ringing can also occur when using the power-up feature, and the ac coupling capacitors do not exactly match in value. We will examine the latter case in a moment. Ringing in a linear amplifier is annoying, but in a log amp, with its much enhanced sensitivity to near zero signals, it can be very disruptive.

To optimize the low level accuracy, that is, achieve a highly damped pulse response in this filter, it is recommended to include a resistor R_Z in series with an increased value of C_Z. Some experimentation may be necessary, but for operation in the range 3 MHz to 70 MHz, values of C_C = 100 pF, C_Z = 1 nF and R_Z = 2 kΩ are near optimal. For operation down to 100 kHz use C_C = 10 nF, C_Z = 0.1 μF and R_Z = 13 kΩ. Figure 5 shows typical connections for the AD606 with these filter components added.

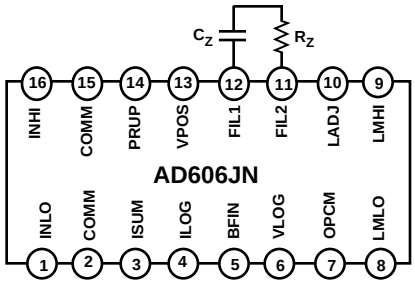


Figure 5. Use of C_Z and R_Z for Offset Control Loop Compensation

For operation above 10 MHz, it is not necessary to add the external capacitors CF1, CF2, and C_Z, although an improvement in low frequency noise can be achieved by so doing (see APPLICATIONS). Note that the offset control loop does not materially affect the low-frequency cutoff at high input levels, when the offset voltage is swamped by the signal.

Power-Up Interface

The AD606 features a power-saving mode, controlled by the logic level at Pin 14 (PRUP). When powered down, the quiescent current is typically 65 μA, or about 325 μW. A CMOS logical HIGH applied to PRUP activates both internal references, and the system becomes fully functional within about 3.5 μs. When this input is a CMOS logical LOW, the system shuts down to the quiescent level within about 5 μs.

The power-up time is somewhat dependent on the signal level and can be degraded by mismatch of the input coupling capacitors. The explanation is as follows. When the AD606 makes the transition from powered-down to fully active, the dc bias voltage at the input nodes INHI and INLO (about +2.5 V) inevitably changes slightly, as base current in the input transistors flows in the bias resistors. In fact, first-order correction for this is included in the specially designed offset buffer amplifier, but even a few millivolts of change at these inputs represents a significant equivalent "dBm" level.

Now, if the coupling capacitors do not match exactly, some fractional part of this residual voltage step becomes coupled into the amplifier. For example, if there is a 10% capacitor mismatch, and INHI and INLO jump 20 mV at power-up, there is a 2 mV pulse input to the system, which may cause the offset control loop to ring. Note that 2 mV is roughly 40 times greater than the amplitude of a sinusoidal input at –75 dBm. As long as the ringing persists, the AD606 will be "blind" to the actual input, and V_{LOG} will show major disturbances.

The solution to this problem is first, to ensure that the loop filter does not ring, and second, to use well-matched capacitors at the signal input. Use the component values suggested above to minimize ringing.

APPLICATIONS

Note that the AD606 has more than 70 MHz of input bandwidth and 90 dB of gain! Careful shielding is needed to realize its full dynamic range, since nearly all application sites will be pervaded by many kinds of interference, radio and TV stations, etc., all of which the AD606 faithfully hears. In bench evaluation, we recommend placing all of the components in a shielded box and using feedthrough decoupling networks for the supply voltage. In many applications, the AD606's low power drain allows the use of a 6 V battery inside the box.

Basic RSSI Application

Figure 6 shows the basic RSSI (Receiver Signal Strength Indicator) application circuit, including the calibration adjustments, either or both of which may be omitted in noncritical applications. This circuit may be used "as is" in such measurement applications as the log/IF strip in a spectrum or network analyzer or, with the addition of an FM or QPSK demodulator fed by the limiter outputs, as an IF strip in such communications applications as a GSM digital mobile radio or FM receiver.

The slope adjustment works in this way: the buffer amplifier (which forms part of a Sallen-Key two-pole filter, see Figure 2) has a dc gain of plus two, and the resistance from BFIN (buffer in) to OPCM (output common) is nominally 9.375 kΩ. This resistance is driven from the logarithmic detector sections with a current scaled 2 μA/dB, generating 18.75 mV/dB at BFIN, hence 37.5 mV/dB at V_{LOG} Now, a resistor (R4 in Figure 6) connected directly between BFIN and VLOG would form a controlled positive-feedback network with the internal 9.375 kΩ resistor which would raise the gain, and thus increase the slope voltage, while the same external resistor connected between BFIN and ground would form a shunt across the internal resistor and reduce the slope voltage. By connecting R4 to a potentiometer R2 across the output, the slope may be adjusted either way; the value for R4 shown in Figure 6 provides approximately ±10% range, with essentially no effect on the slope at the midposition.

The intercept may be adjusted by adding a small current into BFIN via R1 and R3. The AD606 is designed to have the nominal intercept value of –88 dBm when R1 is centered using this network, which provides a range of ±5 dB.

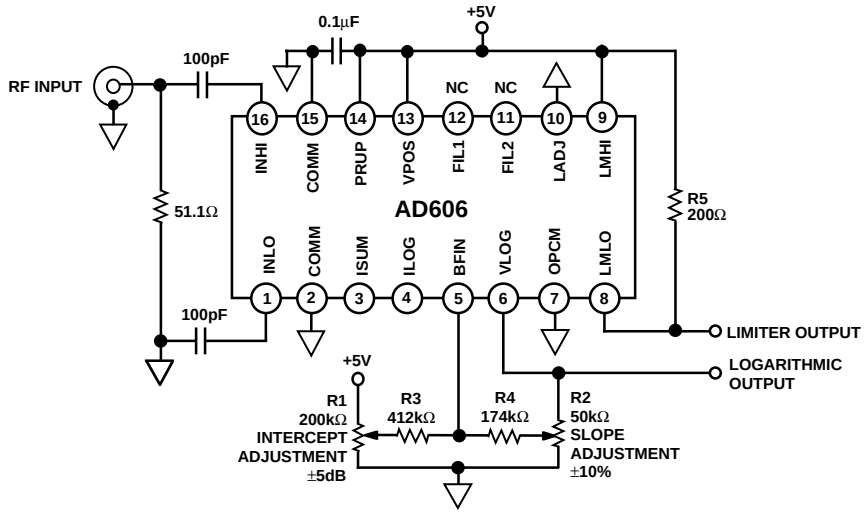


Figure 6. Basic Application Circuit Showing Optional Slope and Intercept Adjustments

Adjustment Procedure

The slope and intercept adjustments interact; this can be minimized by reducing the resistance of R1 and R2, chosen here to minimize power drain. Calibration can be achieved in several ways: The simplest is to apply an RF input at the desired operating frequency which is amplitude modulated at a relatively low frequency (say 1 kHz to 10 kHz) to a known modulation index. Thus, one might choose a ratio of 2 between the maximum and minimum levels of the RF amplitude, corresponding to a 6 dB (strictly, 6.02 dB) change in input level. The average RF level should be set to about –35 dBm (the midpoint of the AD606's range). R2 is then adjusted so that the 6 dB input change results in the desired output voltage change, for example, 226 mV at 37.5 mV/dB.

A better choice would be a 4:1 ratio (12.04 dB), to spread the residual error out over a larger segment of the whole transfer function. If a pulsed RF generator is available, the decibel increment might be enlarged to 20 dB or more. Using just a fixed-level RF generator, the procedure is more time consuming, but is carried out in just the same way: manually change the level by a known number of decibels and adjust R2 until V_{LOG} varies by the corresponding voltage.

Having adjusted the slope, the intercept may now be simply adjusted using a known input level. A value of –35 dBm (397.6 mV rms, or 400 mV to within 0.05 dB) is recommended, and if the standard scaling is used (P_X = –88.33 dBm, V_Y = 37.5 mV/dB), then V_{LOG} should be set to +2 V at this input level.

A Low Cost Audio Through RF Power Meter

Figure 7 shows a simple power meter that uses the AD606 and an ICL7136 3-1/2 digit DMM IC driving an LCD readout. The circuit operates from a single +5 V supply and provides direct readout in dBm, with a resolution of 0.1 dBm.

In contrast to the limited dynamic range of the diode and thermistor-styled sensors used in power meters, the AD606 can measure signals from below –80 dBm to over +10 dBm. An optional 50 Ω termination is included in the figure; this could form the lower arm of an external attenuator to accommodate larger signal levels. By the simple expedient of using a 13 dB attenuator, the LCD reading now becomes dBV (decibels above 1 V rms). This requires a series resistor of 174 Ω, presenting an input resistance of 224 Ω. Alternatively, the input resistance can be raised to 600 Ω using 464 Ω and 133 Ω. It is important to note that the AD606 inputs must be ac coupled. To extend the low frequency range, use larger coupling capacitors and an external loop filter, as outlined earlier.

The nominal 0.5 V to 3.5 V output of the AD606 (for a –75 dBm to +5 dBm input) must be scaled and level shifted to fit within the +1 V to +4.5 V common-mode range of the ICL7136 for the +5 V supply used. This is achieved by the passive resistor network of R1, R2, and R3 in conjunction with the bias networks of R4 through R7, which provide the ICL7136 with its reference voltage, and R9 through R11, which set the intercept. The ICL7136 measures the differential voltage between IN HI and IN LO, which ranges from –75 mV to +5 mV for a –75 dBm to +5 dBm input.

To calibrate the power meter, first adjust R6 for 100 mV between REF HI and REF LO. This sets the initial slope. Then adjust R10 to set IN LO 80 mV higher than IN HI. This sets the initial intercept. The slope and intercept may now be adjusted using a calibrated signal generator as outlined in the previous section.

To extend the low frequency limit of the system to audio frequencies, simply change C1, C2, and C3 to 4.7 μF.

The limiter output of the AD606 may be used to drive the high-impedance input of a frequency counter.

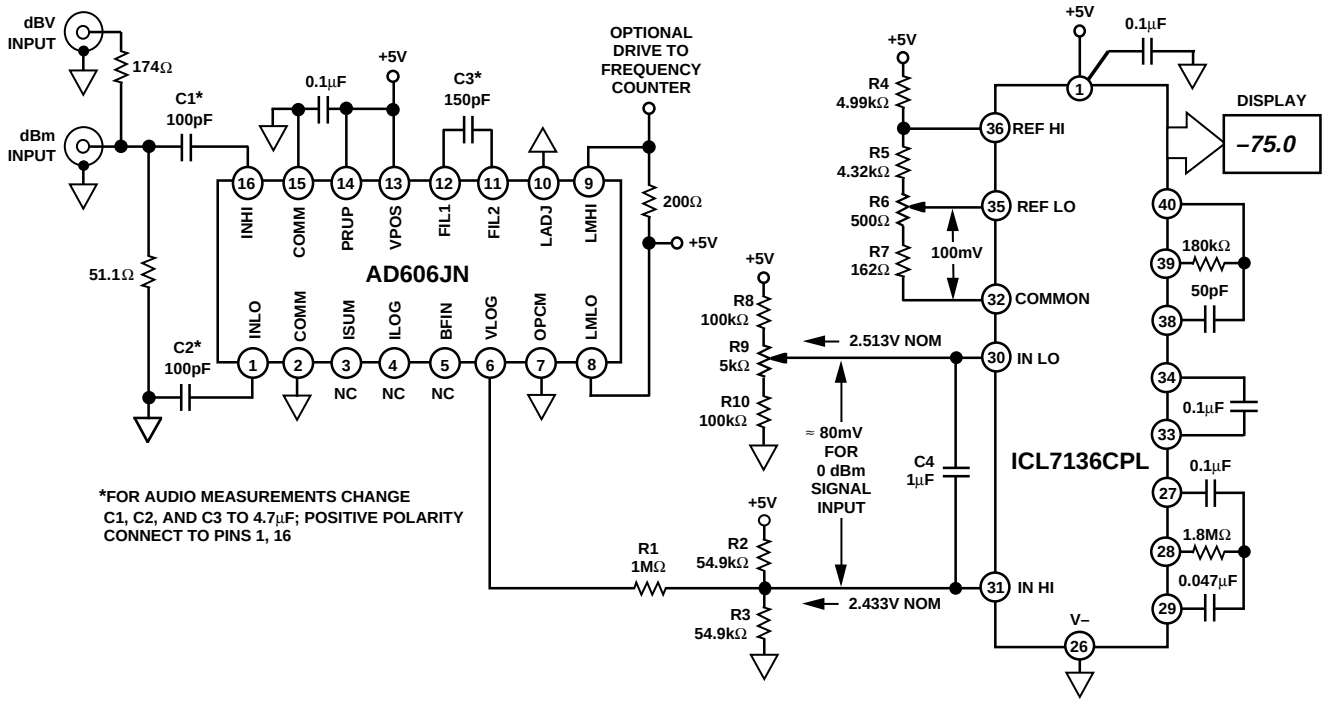


Figure 7. A Low Cost RF Power Meter

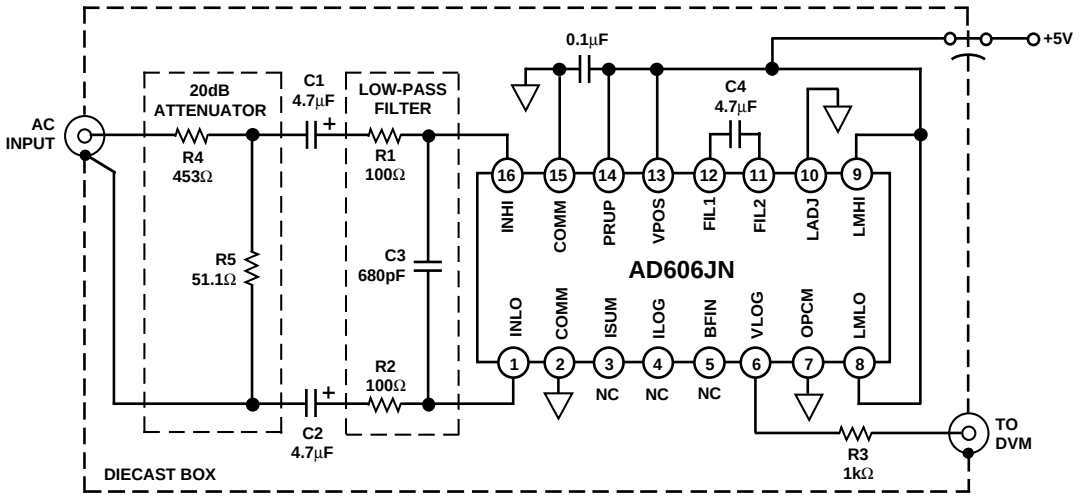


Figure 8. Circuit for Low Frequency Measurements

Low Frequency Applications

With reasonably sized input coupling capacitors and an optional input low-pass filter, the AD606 can operate to frequencies as low as 200 Hz with good log conformance. Figure 8 shows the schematic, with the low-pass filter included in the dashed box. This circuit should be built inside a die cast box and the signal brought in through a coaxial connector. The circuit must also have a low-pass filter to reject the attenuated RF signals that would otherwise be rectified along with the desired signal and be added to the log output. The shielded and filtered circuit has a 90 dB dynamic range, as shown in Figure 9.

In this circuit, R4 and R5 form a 20 dB attenuator that extends the input range to 10 V rms. R3 isolates loads from VLOG. Capacitors C1 and C2 (4.7 μF each), R1, R2, and the AD606's input resistance of 2.5 kΩ form a 100 Hz high-pass filter that is before the AD606; the corner frequency of this filter must be well below the lowest frequency of interest. In addition, the offset-correction loop introduces another pole at low signal levels that is transformed into another high-pass filter because it is in a feedback path. This indicates that there has to be a gradual transition from a 40 dB roll off at low signal levels to a 20 dB roll off at high signal levels, at which point the feedback low pass filter is effectively disabled since the incoming signal swamps the feedback signal.

This low-pass filter introduces some attenuation due to R1 and R2 in conjunction with the 2.5 kΩ input resistance of the AD606. To minimize this effect, the value of R1 and R2 should be kept as small as possible–100 Ω is a good value since it balances the need to reduce the attenuation as mentioned above with the requirement for R1 and R2 to be much larger then the impedance of C1 and C2 at the low-pass corner frequency, in our case about 1 MHz.

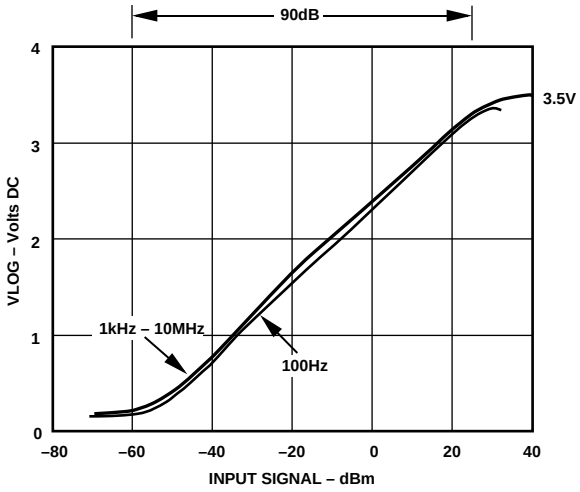


Figure 9. Performance of Low Frequency Circuit at 100 Hz and 1 kHz to 10 MHz (Note Attenuation)

AD606–Typical Characteristics

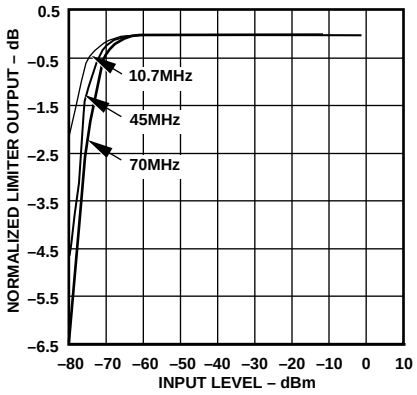


Figure 10. Normalized Limiter Amplitude Response vs. Input Level at 10.7 MHz, 45 MHz and 70 MHz

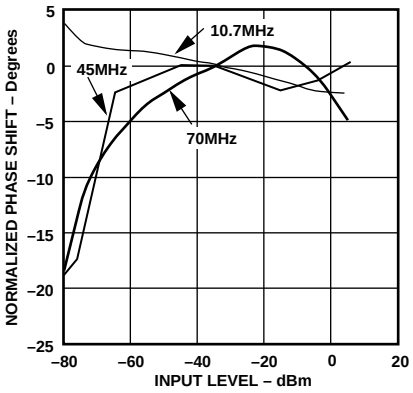


Figure 11. Normalized Limiter Phase Response vs. Input Level at 10.7 MHz, 45 MHz, and 70 MHz

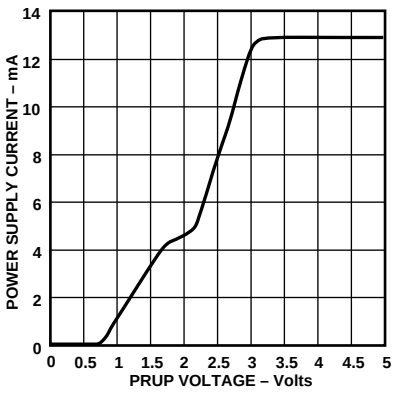


Figure 12. Supply Current vs. PRUP Voltage at +25°C

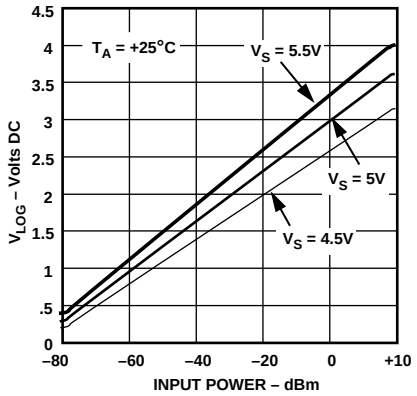


Figure 13. V_{LOG} Plotted vs. Input Level at 10.7 MHz as a Function of Power Supply Voltage

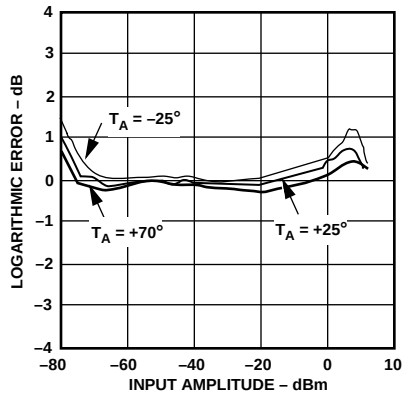


Figure 14. Logarithmic Conformance as a Function of Input Level at 10.7 MHz at –25°C, +25°C, and +70°C

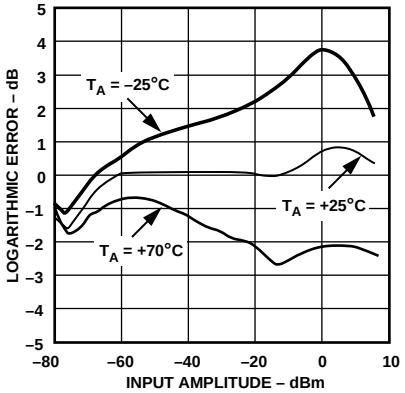


Figure 15. Logarithmic Conformance as a Function of Input Level at 45 MHz at –25°C, +25°C, and +70°C

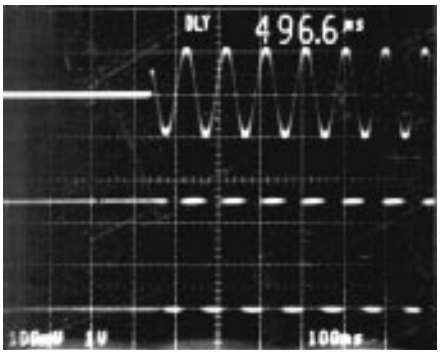


Figure 16. Limiter Response at Onset of 10.7 MHz Modulated Pulse at –75 dBm Using 200 pF Input Coupling Capacitors

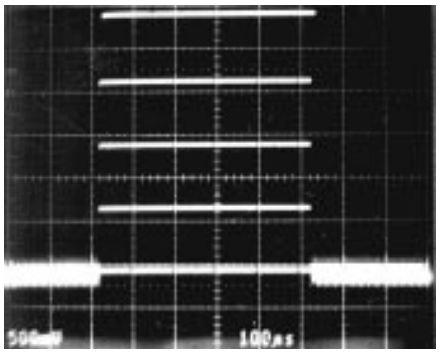


Figure 17. V_{LOG} Response to a 10.7 MHz CW Signal Modulated by a 25 μs Wide Pulse with a 25 kHz Repetition Rate Using 200 pF Input Coupling Capacitors. The Input Signal Goes from +5 dBm to –75 dBm in 20 dB Steps.

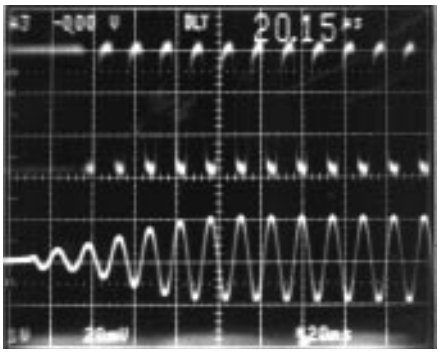


Figure 18. Limiter Response at Onset of 70 MHz Modulated Pulse at –55 dBm Using 200 pF Input Coupling Capacitors

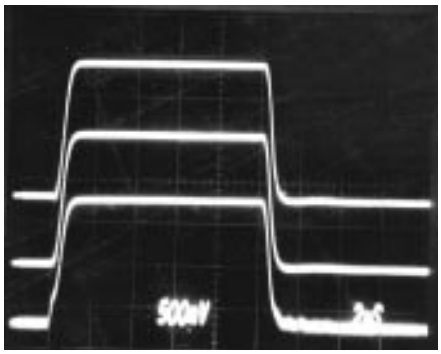


Figure 19. V_{LOG} Output for a Pulsed 10.7 MHz Input; Top Trace: –35 dBm to +5 dBm; Middle Trace: –15 dBm to –55 dBm; Bottom Trace: –35 dBm to –75 dBm

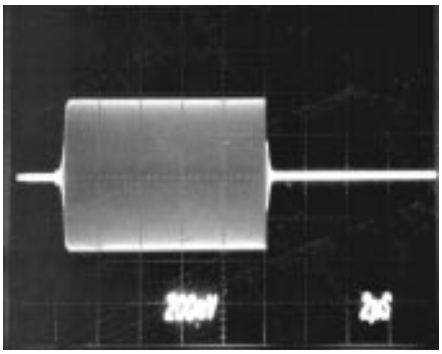


Figure 20. Example of Test Signal Used for Figure 19

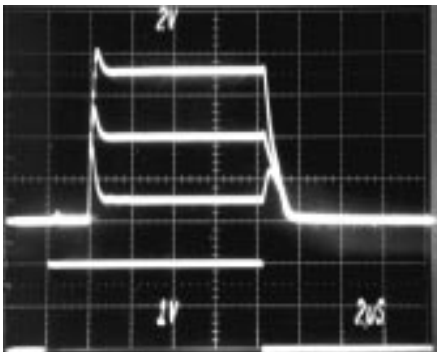


Figure 21. V_{LOG} Output for 10.7 MHz CW Input with PRUP Toggled ON and OFF; Top Trace: +5 dBm Input; Middle Trace: –35 dBm Input; Bottom Trace: –75 dBm; PRUP Input from HP8112A:0 to 4 V, 10 µs Pulse Width with 10 kHz Repetition Rate

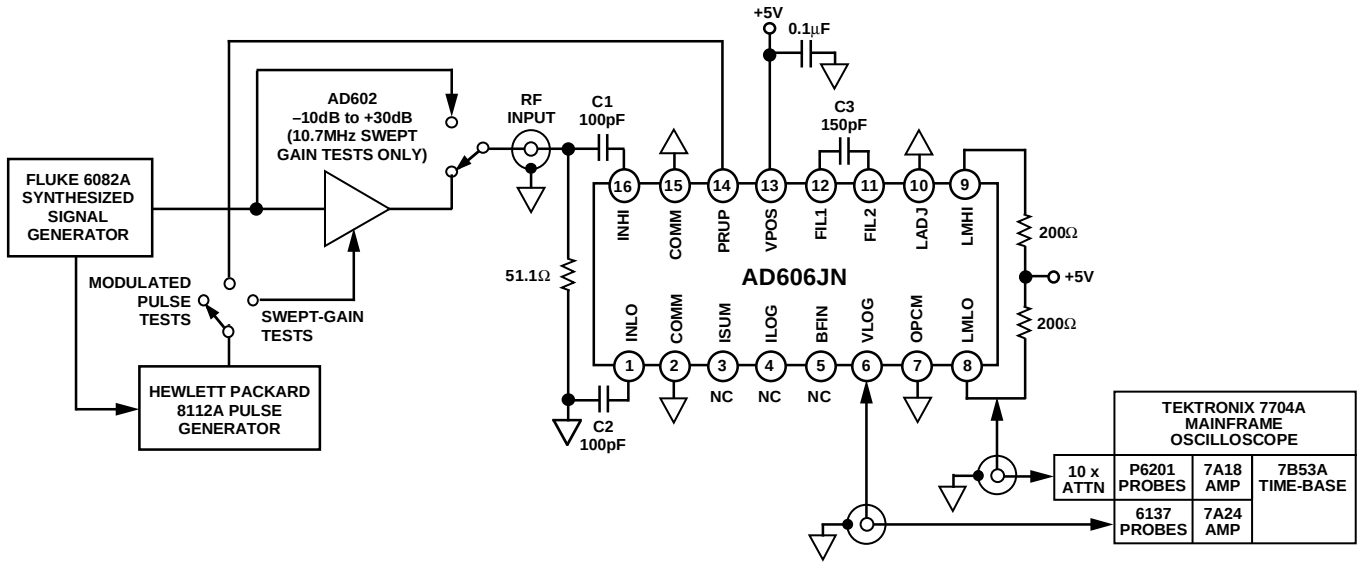
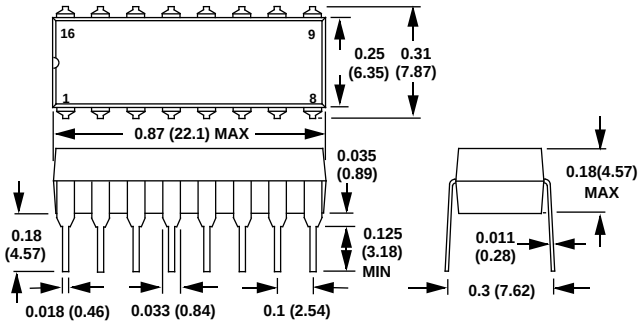


Figure 22. Test Setup for Characterization Data

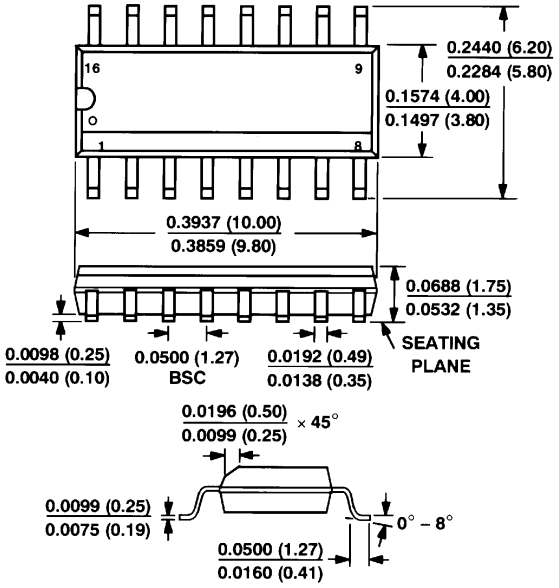
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic (N-16) Package



16-Pin Plastic Narrow-Body Small Outline IC (R-16A) Package



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