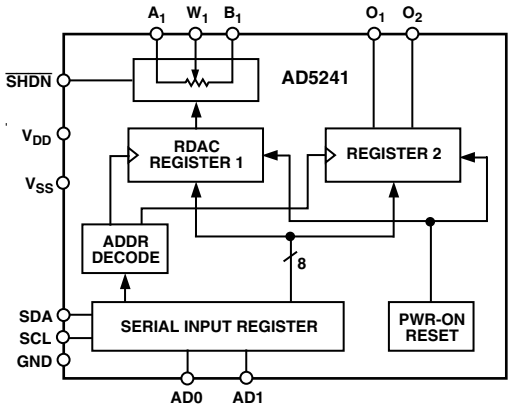
I²C®-Compatible 256-Position Digital Potentiometers

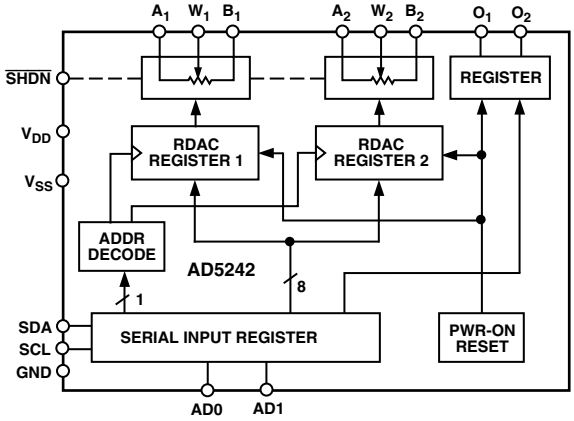
AD5241/AD5242

FEATURES
256 Position
10 kΩ, 100 kΩ, 1 MΩ
Low Tempco 30 ppm/°C
Internal Power ON Midscale Preset
Single Supply 2.7 V to 5.5 V or
Dual Supply ±2.7 V for AC or Bipolar Operation
I²C-Compatible Interface

APPLICATIONS
Multimedia, Video and Audio
Communications
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage-to-Current Conversion
Line Impedance Matching

FUNCTIONAL BLOCK DIAGRAM





GENERAL DESCRIPTION

The AD5241/AD5242 provides a single-/dual-channel, 256-position digitally-controlled variable resistor (VR) device. These devices perform the same electronic adjustment function as a potentiometer, trimmer or variable resistor. Each VR offers a completely programmable value of resistance, between the A terminal and the wiper, or the B terminal and the wiper. For AD5242, the fixed A-to-B terminal resistance of 10 kΩ, 100 kΩ or 1 MΩ has a 1% channel-to-channel matching tolerance. Nominal temperature coefficient of both parts is 30 ppm/°C.

Wiper position programming defaults to midscale at system power ON. Once powered, the VR wiper position is programmed by an I²C-compatible 2-wire serial data interface. Both parts have two extra programmable logic outputs available which facilitate users to drive digital loads, logic gates, LED drivers, and analog switches in their system.

The AD5241/AD5242 is available in surface-mount (SO-14/-16) packages and, for ultracompact solutions, TSSOP-14/-16 packages. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C. For 3-wire, SPI-compatible interface applications, please refer to AD5200, AD5201, AD5203, AD5204, AD5206, AD5231*, AD5232*, AD5235*, AD7376, AD8400, AD8402, AD8403 products.

*Nonvolatile digital potentiometer.
I²C is a registered trademark of Philips Corporation.

REV. 0

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AD5241/AD5242–SPECIFICATIONS

10 kΩ, 100 kΩ, 1 MΩ VERSION

(V_{DD} = 3 V ± 10% or 5 V ± 10%, V_A = +V_{DD}, V_B = 0 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE (Specifications apply to all VRs.)						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC	–1	±0.4	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–2	±0.5	+2	LSB
Nominal Resistor Tolerance	ΔR	T_A = 25°C, RAB = 10 kΩ	–30		+30	%
Nominal Resistor Tolerance	ΔR	T_A = 25°C, RAB = 100 kΩ/1 MΩ	–30		+50	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		30		ppm/°C
Wiper Resistance	R_W	I_W = V_{DD} /R, V_{DD} = 3 V or 5 V		60	120	Ω
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs.)						
Resolution	N		8			Bits
Differential Nonlinearity[3]	DNL		–1	±0.4	+1	LSB
Integral Nonlinearity[3]	INL		–2	±0.5	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–1	–0.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	0.5	1	LSB
RESISTOR TERMINALS						
Voltage Range[4]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[5] A, B	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 80_H		45		pF
Capacitance[5] W	C_W	f = 1 MHz, Measured to GND, Code = 80_H		60		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_W		1		nA
DIGITAL INPUTS						
Input Logic High (SDA and SCL)	V_{IH}		0.7 V_{DD}		V_{DD} + 0.5	V
Input Logic Low (SDA and SCL)	V_{IL}		–0.5		0.3 V_{DD}	V
Input Logic High (AD0 and AD1)	V_{IH}	V_{DD} = 5 V	2.4		V_{DD}	V
Input Logic Low (AD0 and AD1)	V_{IL}	V_{DD} = 5 V	0		0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1		V_{DD}	V
Input Logic Low	V_{IL}	V_{DD} = 3 V	0		0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			1	μA
Input Capacitance[5]	C_{IL}			3		pF
DIGITAL Output	V_{OL}	I_{OL} = 3 mA			0.4	V
Output Logic Low (SDA)	V_{OL}	I_{OL} = 6 mA			0.6	V
Output Logic Low (O_1 and O_2)	V_{OL}	I_{SINK} = 1.6 mA			0.4	V
Output Logic High (O_1 and O_2)	V_{OH}	I_{SOURCE} = 40 μA	4			V
Three-State Leakage Current (SDA)	I_{OZ}	V_{IN} = 0 V or 5 V			±1	μA
Output Capacitance[5]	C_{OZ}			3	8	pF
POWER SUPPLIES						
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	2.7		5.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±2.3		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		0.1	50	μA
Negative Supply Current	I_{SS}	V_{SS} = –2.5 V, V_{DD} = +2.5 V		0.1	–50	μA
Power Dissipation[6]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		0.5	250	μW
Power Supply Sensitivity	PSS		–0.01	0.002	+0.01	%/%
DYNAMIC CHARACTERISTICS[5, 7, 8]						
Bandwidth –3 dB	BW_10 kΩ	R_{AB} = 10 kΩ, Code = 80_H		650		kHz
	BW_100 kΩ	R_{AB} = 100 kΩ, Code = 80_H		69		kHz
	BW_1 MΩ	R_{AB} = 1 MΩ, Code = 80_H		6		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.005		%
V_W Settling Time	t_S	V_A = V_{DD}, V_B = 0 V, ±1 LSB Error Band, R_{AB} = 10 kΩ		2		μs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		14		nV√Hz

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS (Applies to all parts.[5, 9])						
SCL Clock Frequency	f_{SCL}		0		400	kHz
t_{BUF} Bus Free Time Between STOP and START	t_1		1.3			µs
$t_{HD; STA}$ Hold Time (Repeated START)	t_2	After this period the first clock pulse is generated.	600			ns
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU; STA}$ Setup Time for START Condition	t_5		600			ns
$t_{HD; DAT}$ Data Hold Time	t_6				900	ns
$t_{SU; DAT}$ Data Setup Time	t_7		100			ns
t_R Rise Time of Both SDA and SCL Signals	t_8				300	ns
t_F Fall Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU; STO}$ Setup Time for STOP Condition	t_{10}		600			ns

NOTES:
[1]Typicals represent average readings at 25°C, V_{DD} = 5 V.
[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 10 test circuit.
[3]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions. See Figure 9 test circuit.
[4]Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[5]Guaranteed by design and not subject to production test.
[6]P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[7]Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[8]All dynamic characteristics use V_{DD} = 5 V.
[9]See timing diagram for location of measured values.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted)

V_{DD} to GND ..... –0.3, +7 V
V_{SS} to GND ..... 0 V, –7 V
V_{DD} to V_{SS} ..... 7 V
V_A, V_B, V_W to GND ..... V_{SS}, V_{DD}
A_X–B_X, A_X–W_X, B_X–W_X at 10 kΩ in TSSOP-14 ... ±5.0 mA*
A_X–B_X, A_X–W_X, B_X–W_X at 100 kΩ in TSSOP-14 .. ±1.5 mA*
A_X–B_X, A_X–W_X, B_X–W_X at 1 MΩ in TSSOP-14 ... ±0.5 mA*
Digital Input Voltage to GND ..... 0 V, 7 V
Operating Temperature Range ..... –40°C to +85°C
Thermal Resistance θ_{JA}
  SOIC (SO-14) ..... 158°C/W
  SOIC (SO-16) ..... 73°C/W
  TSSOP-14 ..... 206°C/W
  TSSOP-16 ..... 180°C/W
Maximum Junction Temperature (T_JMAX) ..... 150°C
Package Power Dissipation $P_D = (T_J MAX - T_A)/\theta_{JA}$
Storage Temperature ..... –65°C to +150°C
Lead Temperature
  R-14, R-16, RU-14, RU-16 (Vapor Phase, 60 sec) .. 215°C
  R-14, R-16, RU-14, RU-16 (Infrared, 15 sec) ..... 220°C

*Max Current increases at lower resistance and different packages.

ORDERING GUIDE

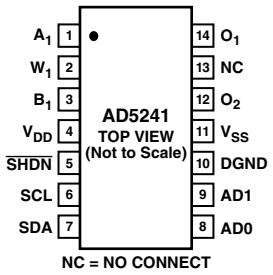
Model	Ω	Temp	Package Description	Package Option
AD5241BR10	10 k	–40/+85°C	SO-14	R-14
AD5241BRU10	10 k	–40/+85°C	TSSOP-14	RU-14
AD5241BR100	100 k	–40/+85°C	SO-14	R-14
AD5241BRU100	100 k	–40/+85°C	TSSOP-14	RU-14
AD5241BR1M	1 M	–40/+85°C	SO-14	R-14
AD5241BRU1M	1 M	–40/+85°C	TSSOP-14	RU-14
AD5242BR10	10 k	–40/+85°C	SO-16	R-16A
AD5242BRU10	10 k	–40/+85°C	TSSOP-16	RU-16
AD5242BR100	100 k	–40/+85°C	SO-16	R-16A
AD5242BRU100	100 k	–40/+85°C	TSSOP-16	RU-16
AD5242BR1M	1 M	–40/+85°C	SO-16	R-16A
AD5242BRU1M	1 M	–40/+85°C	TSSOP-16	RU-16

NOTES
1. The AD5241/AD5242 die size is 69 mil × 78 mil, 5,382 sq. mil. Contains 386 transistors for each channel. Patent Number 5495245 applies.
2. TSSOP packaged units are only available in 1,000-piece quantity Tape and Reel.

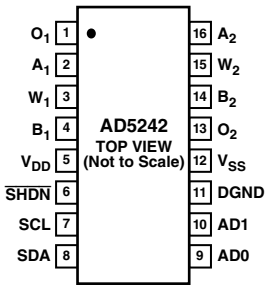
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5241/AD5242 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD5241 PIN CONFIGURATION



AD5242 PIN CONFIGURATION



AD5241 PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	A_1	Resistor Terminal A_1
2	W_1	Wiper Terminal W_1
3	B_1	Resistor Terminal B_1
4	V_{DD}	Positive power supply, specified for operation from 2.2 V to 5.5 V.
5	$\overline{SHDN}$	Active low, asynchronous connection of the Wiper W to Terminal B, and open circuit of Terminal A. RDAC register contents unchanged.
6	SCL	Serial Clock Input
7	SDA	Serial Data Input/Output
8	AD0	Programmable address bit for multiple package decoding. Bits AD0 and AD1 provide four possible addresses.
9	AD1	Programmable address bit for multiple package decoding. Bits AD0 and AD1 provide four possible addresses.
10	DGND	Common Ground
11	V_{SS}	Negative power supply, specified for operation from 0 V to –2.7 V.
12	O_2	Logic Output Terminal O_2
13	NC	No Connect
14	O_1	Logic Output Terminal O_1

AD5242 PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	O_1	Logic Output Terminal O_1
2	A_1	Resistor Terminal A_1
3	W_1	Wiper Terminal W_1
4	B_1	Resistor Terminal B_1
5	V_{DD}	Positive power supply, specified for operation from 2.2 V to 5.5 V.
6	$\overline{SHDN}$	Active low, asynchronous connection of the Wiper W to Terminal B, and open circuit of Terminal A. RDAC register contents unchanged.
7	SCL	Serial Clock Input
8	SDA	Serial Data Input/Output
9	AD0	Programmable address bit for multiple package decoding. Bits AD0 and AD1 provide four possible addresses.
10	AD1	Programmable address bit for multiple package decoding. Bits AD0 and AD1 provide four possible addresses.
11	DGND	Common Ground
12	V_{SS}	Negative power supply, specified for operation from 0 V to –2.7 V.
13	O_2	Logic Output Terminal O_2
14	B_2	Resistor Terminal B_2
15	W_2	Wiper Terminal W_2
16	A_2	Resistor Terminal A_2

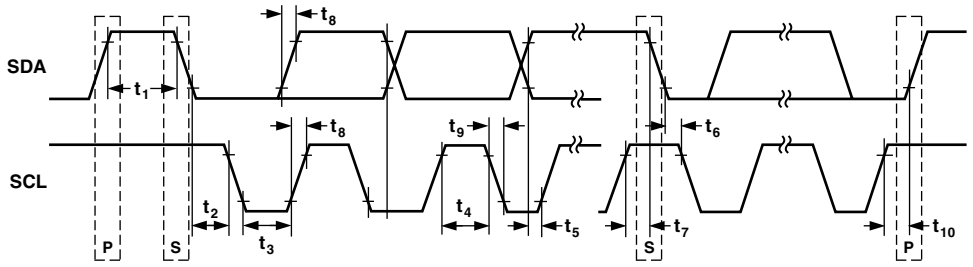


Figure 1. Detail Timing Diagram

Data of AD5241/AD5242 is accepted from the I²C bus in the following serial format:

S	0	1	0	1	1	AD1	AD0	R/$\overline{W}$	A	$\overline{A}$/B	RS	SD	O2	O1	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	SLAVE ADDRESS BYTE									INSTRUCTION BYTE									DATA BYTE									

where:
S = Start Condition.
P = Stop Condition.
A = Acknowledge.
X = Don't Care.
AD1, AD0 = Package pin programmable address bits. Must be matched with the logic states at pins AD1 and AD0.
R/$\overline{W}$ = Read Enable at High and Write Enable at Low.
$\overline{A}$/B = RDAC sub address select. '0' for RDAC1 and '1' for RDAC2.
RS = Midscale reset, active high.
SD = Shutdown in active high. Same as $\overline{SHDN}$ except inverse logic.
O_2, O_1 = Output logic pin latched values.
D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits.

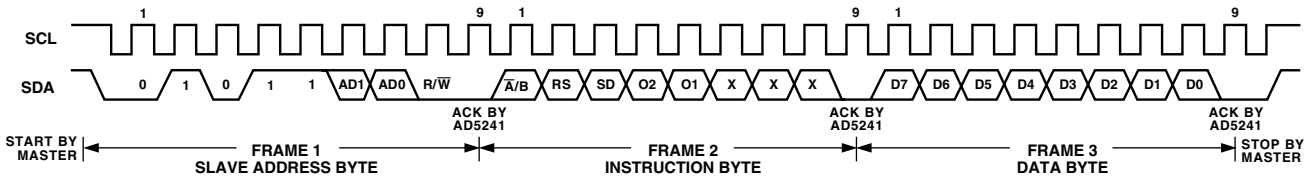


Figure 2. Writing to the RDAC Serial Register

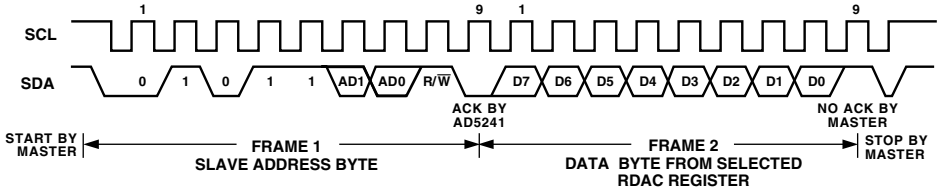
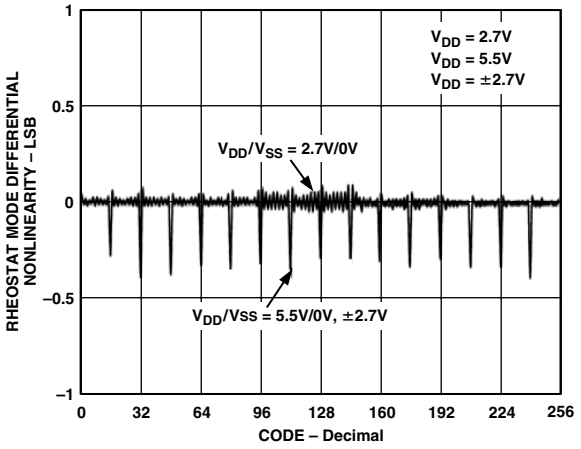
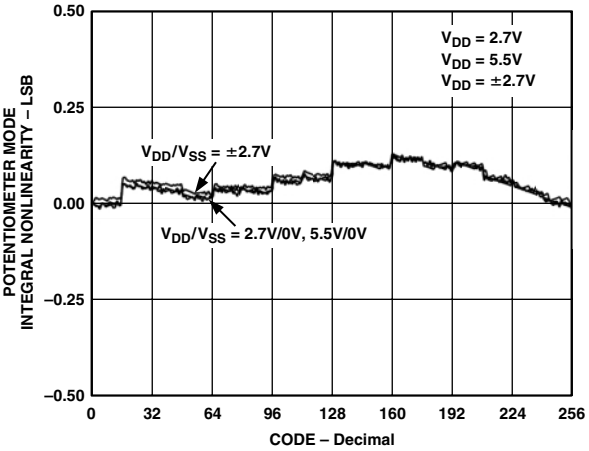


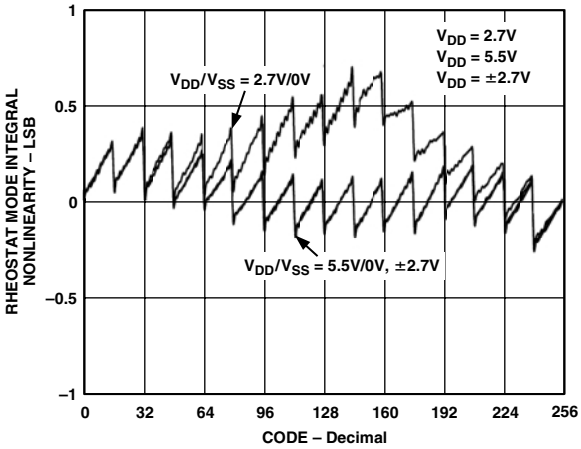
Figure 3. Reading Data from a Previously Selected RDAC Register



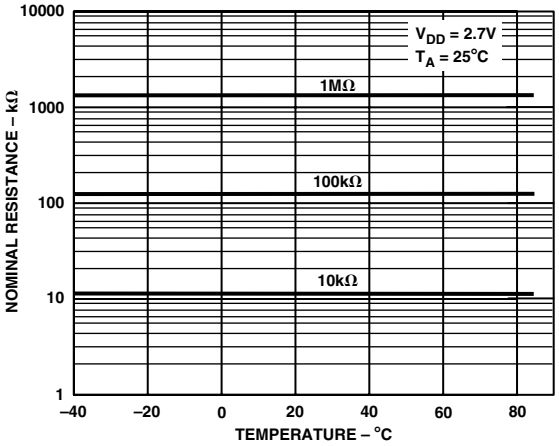
TPC 1. RDNL vs. Code



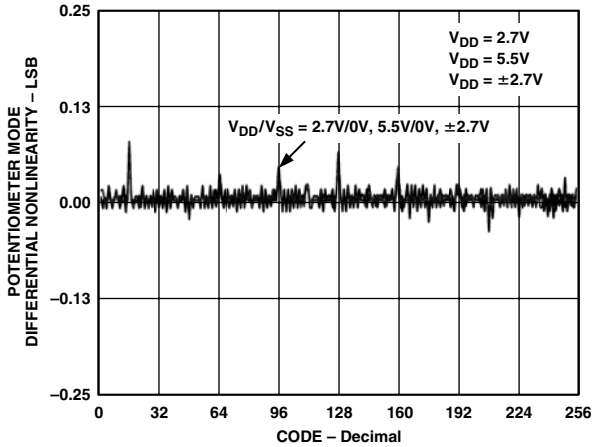
TPC 4. INL vs. Code



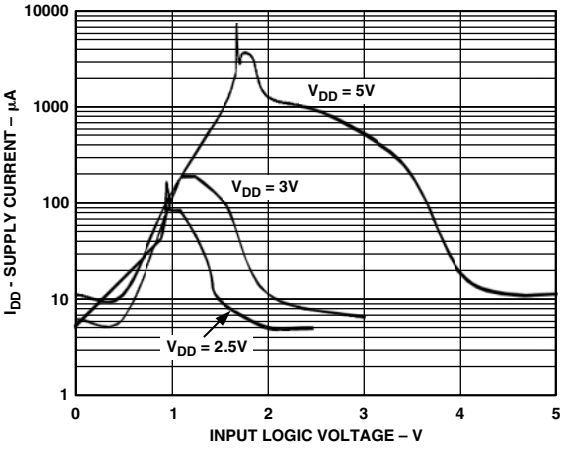
TPC 2. RINL vs. Code



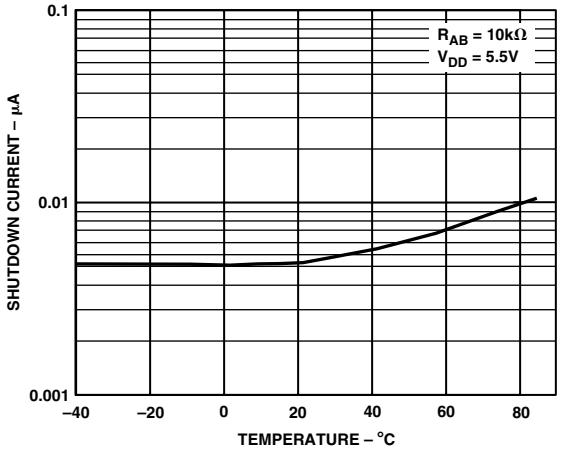
TPC 5. Nominal Resistance vs. Temperature



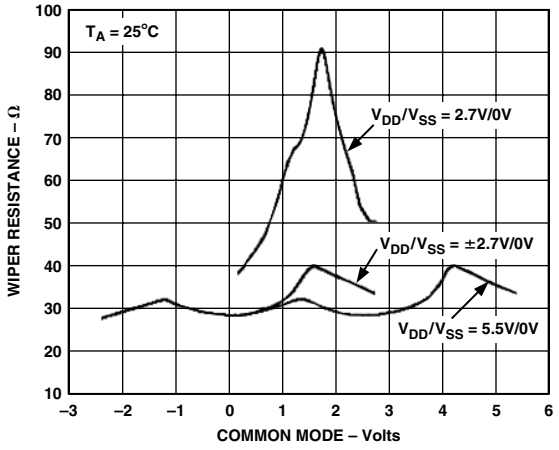
TPC 3. DNL vs. Code



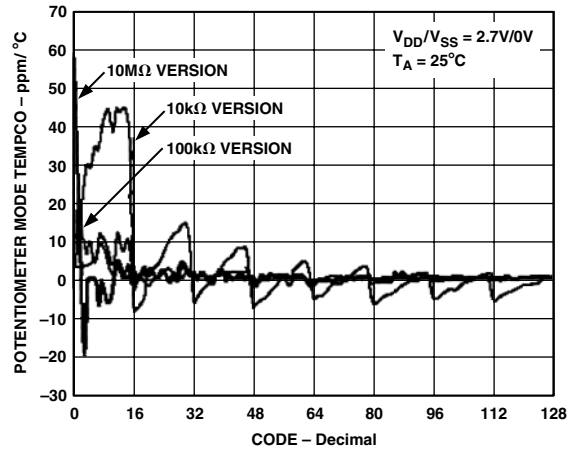
TPC 6. Supply Current vs. Logic Input Voltage



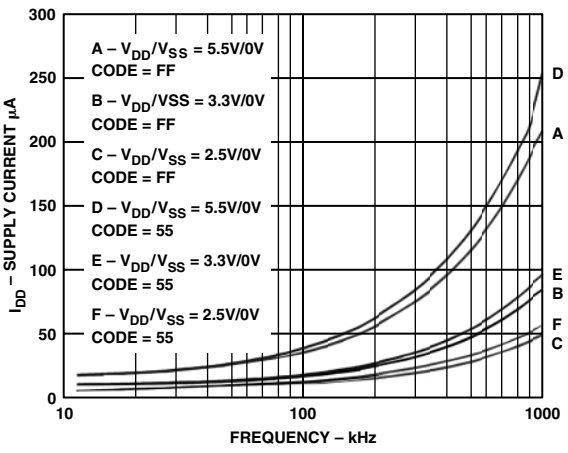
TPC 7. Shutdown Current vs. Temperature



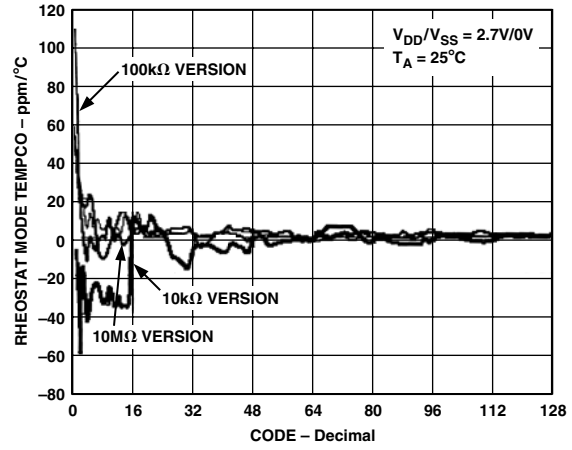
TPC 10. Incremental Wiper Contact vs. V_{DD}/V_{SS}



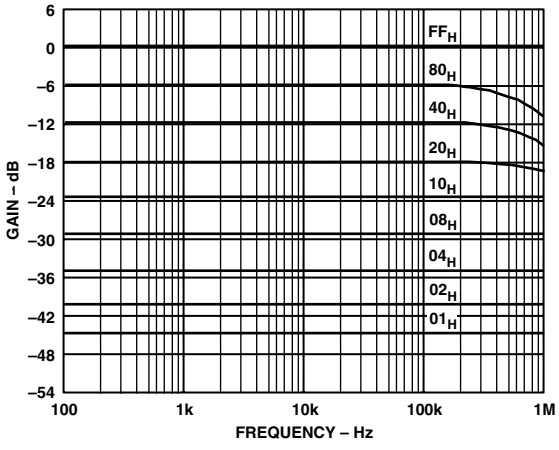
TPC 8. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco



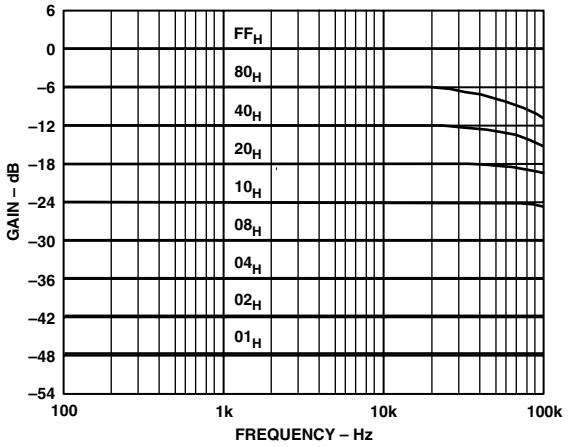
TPC 11. Supply Current vs. Frequency



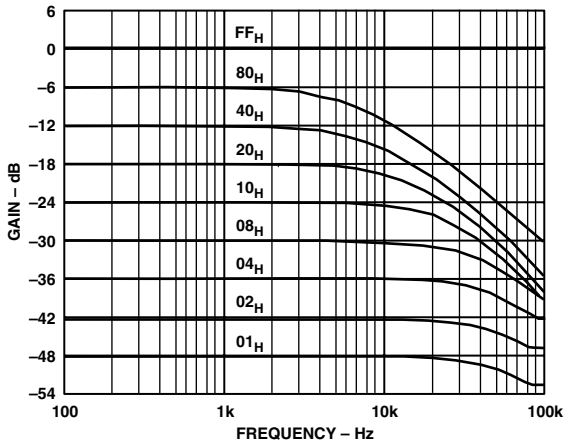
TPC 9. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco



TPC 12. AD5242 10 kΩ Gain vs. Frequency vs. Code



TPC 13. AD5242 100 kΩ Gain vs. Frequency vs. Code



TPC 14. AD5242 1 MΩ Gain vs. Frequency vs. Code

OPERATION

The AD5241/AD5242 provides a single-/dual-channel, 256-position digitally-controlled variable resistor (VR) device. The terms VR, RDAC, and programmable resistor are commonly used interchangeably to refer to digital potentiometer.

To program the VR settings, refer to the Digital Interface section. Both parts have an internal power ON preset that places the wiper in midscale during power-on, which simplifies the fault condition recovery at power-up. In addition, the shutdown $\overline{\text{SHDN}}$ pin of AD5241/AD5242 places the RDAC in an almost zero power consumption state where Terminal A is open circuited and the Wiper W is connected to Terminal B, resulting in only leakage current being consumed in the VR structure. During shutdown, the VR latch contents are maintained when the RDAC is inactive. When the part is returned from shutdown, the stored VR setting will be applied to the RDAC.

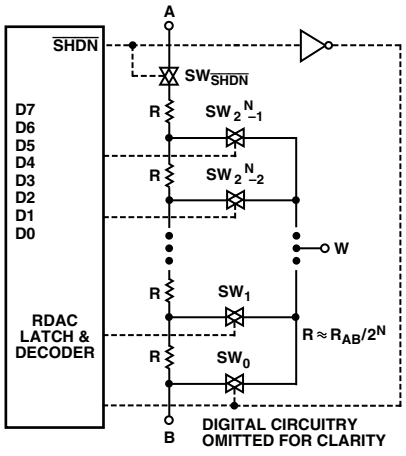


Figure 4. AD5241/AD5242 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B are available in 10 kΩ, 100 kΩ, and 1 MΩ. The final two or three digits of the part number determine the nominal resistance value, e.g. 10 kΩ = 10; 100 kΩ = 100; 1 MΩ = 1 M. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 00_H. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point corresponds to 99 Ω (R_{WB} = R_{AB}/256 + R_W = 39 + 60) for data 01_H. The third connection is the next tap point representing 138 Ω (39 × 2 + 60) for data 02_H and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10021 Ω [R_{AB} – 1 LSB + R_W]. Figure 4 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed, and therefore there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

The general equation determining the digitally programmed resistance between W and B is:

$$R_{WB}(D) = \frac{D}{256} \cdot R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code between 0 to 255 which is loaded in the 8-bit RDAC register.

R_{AB} is the nominal end-to-end resistance.

R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Again, if R_{AB} =10 kΩ and A terminal can be either open circuit or tied to W, the following output resistance at R_{WB} will be set for the following RDAC latch codes.

D (DEC)	R_{WB} (Ω)	Output State
255	10021	Full-Scale (R_{WB} – 1 LSB + R_W)
128	5060	Midscale
1	99	1 LSB
0	60	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum current of no more than ±20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a digitally controlled resistance R_{WA}. When these terminals are used, the B terminal can be opened or tied to the wiper terminal. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{256 - D}{256} \cdot R_{AB} + R_W \quad (2)$$

For R_{AB} = 10 kΩ and B terminal can be either open circuit or tied to W, the following output resistance R_{WA} will be set for the following RDAC latch codes.

D (DEC)	R_{WA} (Ω)	Output State
255	99	Full-Scale
128	5060	Midscale
1	10021	1 LSB
0	10060	Zero-Scale

The typical distribution of the nominal resistance R_{AB} from channel-to-channel matches within ±1% for AD5242. Device-to-device matching is process lot dependent and is possible to have ±30% variation. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has no more than 30 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates output voltages at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-to-B. Unlike the polarity of $V_{DD} - V_{SS}$, which must be positive, voltage across A–B, W–A, and W–B can be at either polarity provided that V_{SS} is powered by a negative supply.

If ignoring the effect of the wiper resistance for approximation, connecting A terminal to 5 V and B terminal to ground produces an output voltage at the wiper-to-B starting at zero volt up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal AB divided by the 256 position of the potentiometer divider. Since AD5241/AD5242 can be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminals A and B is:

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

which can be simplified to

$$V_W(D) = \frac{D}{256} V_{AB} + V_B \quad (4)$$

where D is decimal equivalent of the binary code between 0 to 255 which is loaded in the 8-bit RDAC register.

For more accurate calculation including the effects of wiper resistance, V_W can be found as:

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (5)$$

where $R_{WB}(D)$ and $R_{WA}(D)$ can be obtained from Equations 1 and 2.

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent on the ratio of the internal resistors R_{WA}, R_{WB}, and not the absolute values; therefore, the temperature drift reduces to 5 ppm/°C.

DIGITAL INTERFACE

2-Wire Serial Bus

The AD5241/AD5242 are controlled via an I^2C-compatible serial bus. The RDACs are connected to this bus as slave devices.

Referring to Figures 2 and 3, the first byte of AD5241/AD5242 is a Slave Address Byte. It has a 7-bit slave address and a R/$\overline{W}$ bit. The 5 MSBs are 01011 and the following two bits are determined by the state of the AD0 and AD1 pins of the device. AD0 and AD1 allow users to use up to four of these devices on one bus.

The 2-wire I^2C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high, Figure 2. The following byte is the Slave Address Byte, Frame 1, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address will respond by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. If the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. A Write operation contains an extra Instruction Byte more than the Read operation. Such Instruction Byte, Frame 2, in Write mode follows the Slave Address Byte. The MSB of the Instruction Byte labeled $\overline{A}$/B is the RDAC subaddress select. A "low" selects RDAC1 and a "high" selects RDAC2 for the dual-channel AD5242. Set $\overline{A}$/B to low for AD5241. The second MSB, RS, is the Midscale reset. A logic high of this bit moves the wiper of a selected RDAC to the center tap where $R_{WA} = R_{WB}$. The third MSB, SD, is a shutdown bit. A logic high on SD causes the RDAC open circuit at Terminal A while shorting wiper to Terminal B. This operation yields almost a zero Ω in rheostat mode or zero volt in potentiometer mode. This SD bit serves the same function as the $\overline{SHDN}$ pin except $\overline{SHDN}$ pin reacts to active low. The following two

bits are O_2 and O_1. They are extra programmable logic output that users can use to drive other digital loads, logic gates, LED drivers, and analog switches, etc. The three LSBs are DON'T CARE. See Figure 2.

3. After acknowledging the Instruction Byte, the last byte in Write mode is the Data Byte, Frame 3. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an "Acknowledge" bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL, Figure 2.
4. Unlike the Write mode, the Data Byte follows immediately after the acknowledgment of the Slave Address Byte in the Read mode, Frame 2. Data is transmitted over the serial bus in sequences of nine clock pulses (slight difference with the Write mode, there are eight data bits followed by a "No Acknowledge" bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL, Figure 3.
5. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In Write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 2). In Read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse which goes high to establish a STOP condition (see Figure 3).

A repeated Write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. During the Write cycle, each Data byte will update the RDAC output. For example, after the RDAC has acknowledged its Slave Address and Instruction Bytes, the RDAC output will be updated. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the Write mode has to start a whole new sequence with a new Slave Address, Instruction, and Data Bytes transferred again. Similarly, a repeated Read function of the RDAC is also allowed.

MULTIPLE DEVICES ON ONE BUS

Figure 5 shows four AD5242 devices on the same serial bus. Each has a different slave address since the state of their AD0 and AD1 pins are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I^2C-compatible interface. Note, a device will be addressed properly only if the bit information of AD0 and AD1 in the Slave Address Byte matches with the logic inputs at pins AD0 and AD1 of that particular device.

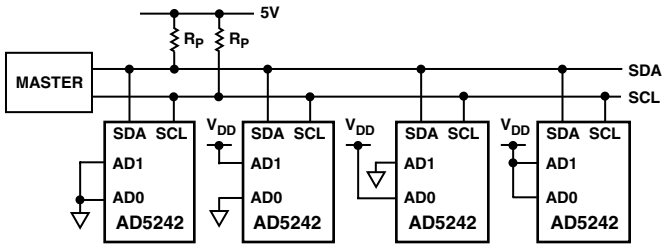


Figure 5. Multiple AD5242 Devices on One Bus

LEVEL SHIFT FOR BIDIRECTIONAL INTERFACE

While most old systems may be operated at one voltage, a new component may be optimized at another. When they operate the same signal at two different voltages, proper method of level-shifting is needed. For instance, one can use a 3.3 V E^2PROM to interface with a 5 V digital potentiometer. A level-shift scheme is needed in order to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E^2PROM. Figure 6 shows one of the techniques. M1 and M2 can be N-Ch FETs 2N7002 or low threshold FDV301N if V_{DD} falls below 2.5 V.

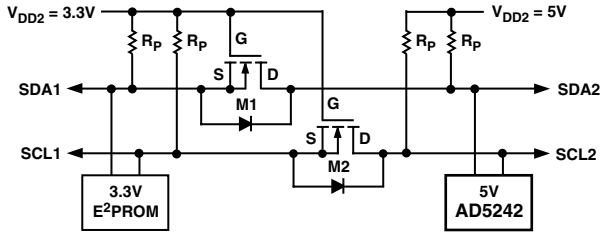


Figure 6. Level-Shift for Different Voltage Devices Operation

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 7. This applies to digital input pins SDA, SCL, and $\overline{SHDN}$.

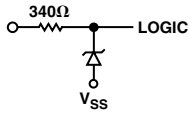


Figure 7. ESD Protection of Digital Pins

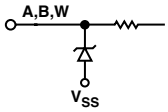


Figure 8. ESD Protection of Resistor Terminals

TEST CIRCUITS

Figures 9 to 17 define the test conditions used in the product specification table.

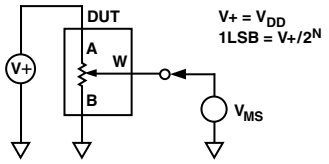


Figure 9. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

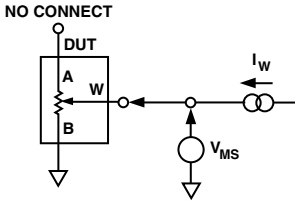


Figure 10. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

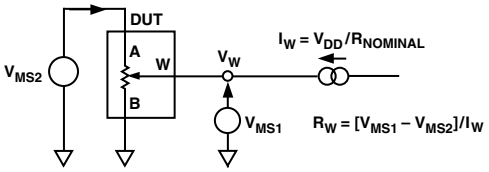


Figure 11. Wiper Resistance Test Circuit

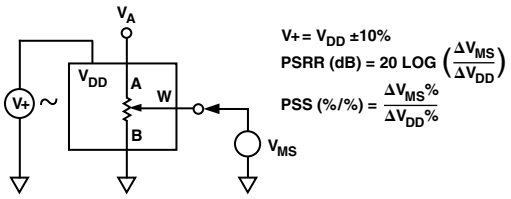


Figure 12. Power Supply Sensitivity Test Circuit (PSS, PSRR)

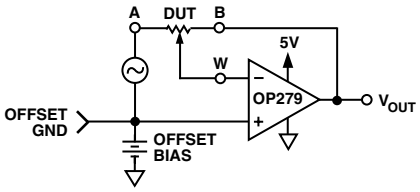


Figure 13. Inverting Gain Test Circuit

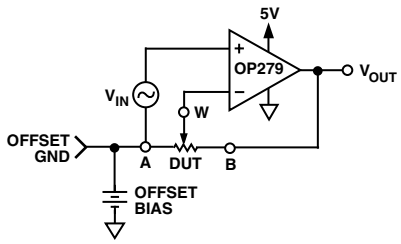


Figure 14. Noninverting Gain Test Circuit

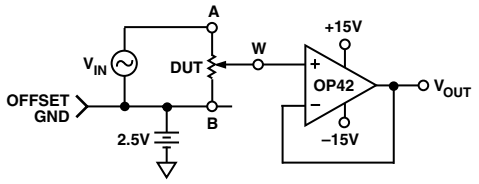


Figure 15. Gain vs. Frequency Test Circuit

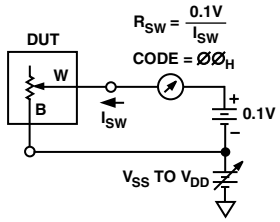


Figure 16. Incremental ON Resistance Test Circuit

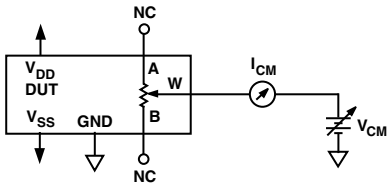


Figure 17. Common-Mode Leakage Current Test Circuit

DIGITAL POTENTIOMETER SELECTION GUIDE

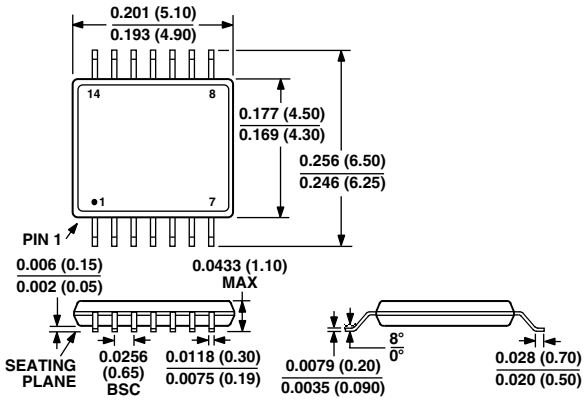
Part Number	Number of VRs per Package[1]	Terminal Voltage Range	Interface Data Control[2]	Nominal Resistance (kΩ)	Resolution (Number of Wiper Positions)	Power Supply Current (I_{DD})	Packages	Comments
AD5201*	1	±3 V, +5.5 V	3-Wire	10, 50	33	60 µA	µSOIC-10	Full AC Specs, Dual Supply, Pwr-On-Reset, Low Cost
AD5220	1	5.5 V	Up/Down	10, 50, 100	128	40 µA	PDIP, SO-8, µSOIC-8	No Rollover, Pwr-On-Reset
AD7376	1	±15 V, +28 V	3-Wire	10, 50, 100, 1000	128	100 µA	PDIP-14, SOL-16, TSSOP-14	Single 28 V or Dual ±15 V Supply Operation
AD5200*	1	±3 V, +5.5 V	3-Wire	10, 50	256	60 µA	µSOIC-10	Full AC Specs, Dual Supply, Pwr-On-Reset
AD8400	1	5.5 V	3-Wire	1, 10, 50, 100	256	5 µA	SO-8	Full AC specs
AD5241	1	±3 V, +5.5 V	2-Wire	10, 100, 1000	256	5 µA	SO-14, TSSOP-14	I^2C-Compatible, TC < 50 ppm/°C
AD5231*	1	±3 V, +5.5 V	3-Wire	10, 50, 100	1024	10 µA	TSSOP-16	*Nonvolatile* Memory, Direct Program, I/D, ±6 dB Settability
AD5222	2	±3 V, +5.5 V	Up/Down	10, 50, 100, 1000	128	80 µA	SO-14, TSSOP-14	No Rollover, Stereo, Pwr-On-Reset, TC < 50 ppm/°C
AD8402	2	5.5 V	3-Wire	1, 10, 50, 100	256	5 µA	PDIP, SO-14, TSSOP-14	Full AC Specs, nA Shutdown Current
AD5232*	2	±3 V, +5.5 V	3-Wire	10, 50, 100	256	10 µA	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5242	2	±3 V, +5.5 V	2-Wire	10, 100, 1000	256	5 µA	SO-16, TSSOP-16	I^2C-Compatible, TC < 50 ppm/°C
AD5262*	2	±5 V, +12 V	3-Wire	10, 50, 100	256	60 µA	TSSOP-16	Medium Voltage Operation, TC < 50 ppm/°C
AD5203	4	5.5 V	3-Wire	10, 100	64	5 µA	PDIP, SOL-24, TSSOP-24	Full AC specs, nA Shutdown Current
AD5233*	4	±3 V, +5.5 V	3-Wire	10, 50, 100	64	10 µA	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5204	4	±3 V, +5.5 V	3-Wire	10, 50, 100	256	5 µA	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Pwr-On-Reset
AD8403	4	5.5 V	3-Wire	1, 10, 50, 100	256	5 µA	PDIP, SOL-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5206	6	±3 V, +5.5 V	3-Wire	10, 50, 100	256	5 µA	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Pwr-On-Reset

NOTES
*Future product, consult factory for latest status.
[1]VR stands for variable resistor. This term is used interchangeably with RDAC, programmable resistor, and digital potentiometer.
[2]3-wire interface is SPI- and microwire-compatible. 2-wire interface is I^2C-compatible.

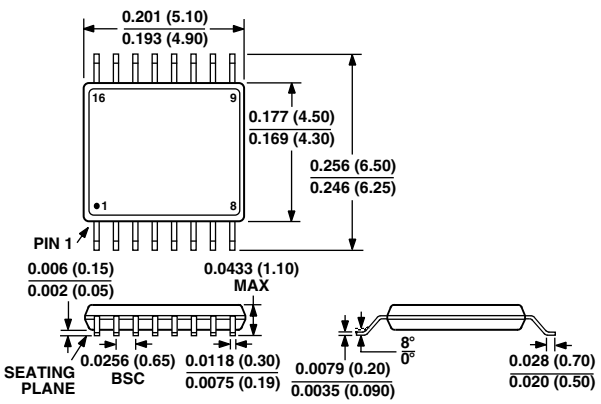
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

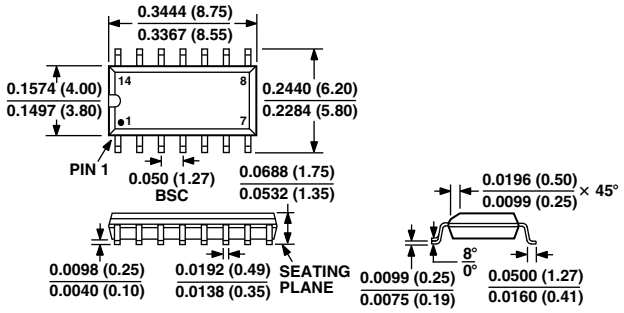
14-Lead TSSOP (RU-14)



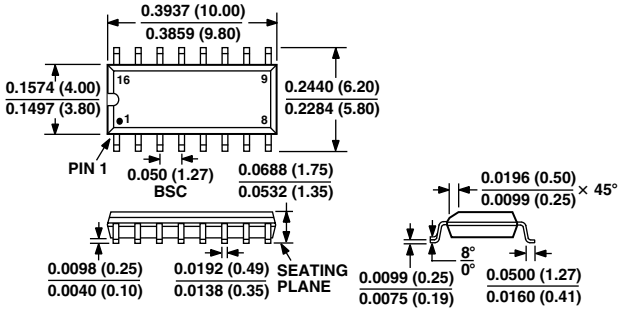
16-Lead TSSOP (RU-16)



14-Lead SOIC (R-14)



16-Lead SOIC (R-16A)



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