Nonvolatile Memory, Quad 64-Position Potentiometers

AD5233*

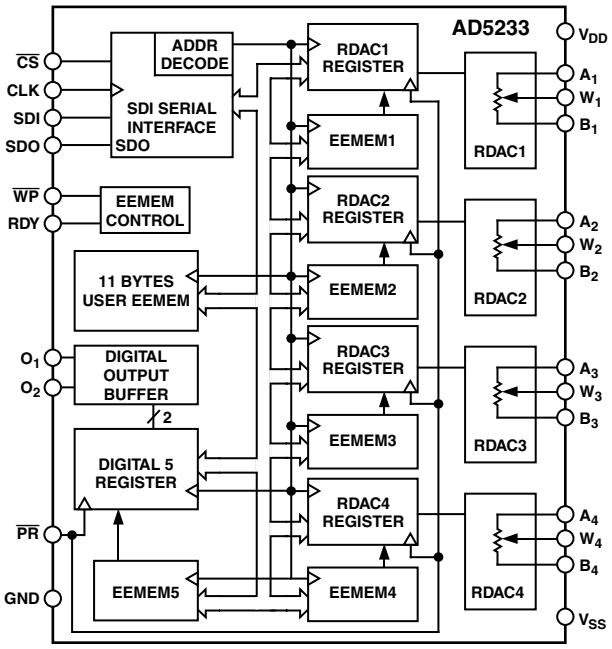
FEATURES

Nonvolatile Memory[1] Preset Maintains Wiper Settings
4-Channel Independent Programmable
64-Position Resolution
Full Monotonic Operation
10 kΩ, 50 kΩ, and 100 kΩ Terminal Resistance
Permanent Memory Write Protection
Wiper Settings Readback
Linear Increment/Decrement
Log Taper Increment/Decrement
Push Button Increment/Decrement Compatible
SPI Compatible Serial Interface with Readback Function
3 V to 5 V Single Supply or ±2.5 V Dual Supply
11 Bytes User Nonvolatile Memory for Constant Storage
100-Year Typical Data Retention T_A = 55°C

APPLICATIONS

Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage to Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching
Power Supply Adjustment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5233 provides a nonvolatile memory, digitally controlled set of potentiometers[2] with 64-position resolution. These devices perform the same electronic adjustment function as a mechanical potentiometer. The AD5233's versatile programming via a standard 3-wire serial interface allows sixteen modes of operation and adjustment including scratch pad programming, memory storing and retrieving, increment/decrement, log taper adjustment, wiper setting readback, and extra user defined EEMEM.

In the scratchpad programming mode, a specific setting can be programmed directly to the RDAC[2] register, which sets the resistance at terminals W–A and W–B. The RDAC register can also be loaded with a value previously stored in the EEMEM[1] register. The value in the EEMEM can be changed or protected. When changes are made to the RDAC register, the value of the new setting can be saved into the EEMEM. Thereafter, such value will be transferred automatically to the RDAC register during system POWER ON, which is enabled by the internal preset strobe. EEMEM can also be retrieved through direct programming and external preset pin control.

The linear step increment and decrement commands allows the setting in the RDAC register to be moved UP or DOWN, one step at a time. For logarithmic changes in wiper setting, a left/right bit shift command adjusts the level in ±6 dB steps.

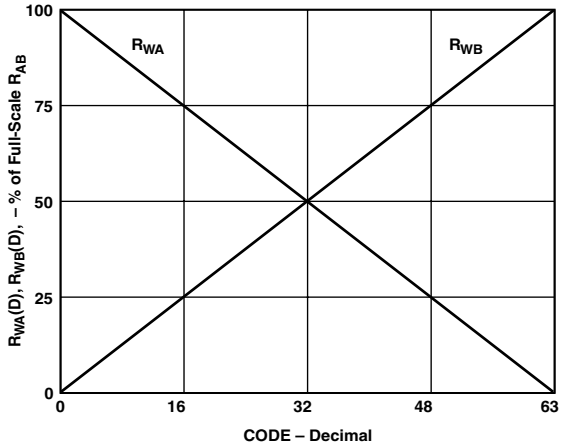


Figure 1. $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

The AD5233 is available in a thin TSSOP-24 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

*Patent pending

NOTES
[1] The terms nonvolatile memory and EEMEM are used interchangeably.
[2] The terms Digital Potentiometer and RDAC are used interchangeably.

REV. 0

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AD5233–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, and 100 kΩ VERSIONS

(V_{DD} = 3 V ±10%, or 5 V ±10%, and V_{SS} = 0 V, $V_A = V_{DD}$, V_B = 0 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC, MONOTONIC	–0.5	±0.1	+0.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–0.5	±0.1	+0.5	LSB
Nominal Resistor Tolerance	ΔR_{WB}	D = $3F_H$	–40		+20	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$			600		ppm/°C
Wiper Resistance	R_W	I_W = 100 µA Code = Half-Scale		15	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Resolution	N		6			Bits
Differential Nonlinearity[3]	DNL	MONOTONIC	–0.5	0.1	+0.5	LSB
Integral Nonlinearity[3]	INL		–0.5	0.1	+0.5	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = Half-Scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = Full-Scale	–1.5		0	%FS
Zero-Scale Error	V_{WZSE}	Code = Zero-Scale	0		+1.5	%FS
RESISTOR TERMINALS						
Terminal Voltage Range[4]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[5] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, Code = Half-Scale		35		pF
Capacitance[5] W	C_W	f = 1 MHz, measured to GND, Code = Half-Scale		35		pF
Common-Mode Leakage Current [5, 6]	I_{CM}	$V_W = V_{DD}/2$		0.015	1	µA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	with respect to GND, V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	with respect to GND, V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	with respect to GND, V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	with respect to GND, V_{DD} = 3 V			0.6	V
Input Logic High	V_{IH}	with respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V	2.0			V
Input Logic Low	V_{IL}	with respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{DD}			±2.5	µA
Input Capacitance[5]	C_{IL}			4		pF
Output Current[5]	I_{O1}, I_{O2}	V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C, Sourcing only		50		mA
		V_{DD} = 2.5 V, V_{SS} = 0 V, T_A = 25°C, Sourcing only		7		mA
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		3.5	10	µA
Programming Mode Current	$I_{DD(PG)}$	$V_{IH} = V_{DD}$ or V_{IL} = GND		40		mA
Read Mode Current[7]	$I_{DD(XFR)}$	$V_{IH} = V_{DD}$ or V_{IL} = GND	0.3	3	9	mA
Negative Supply Current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V				
		V_A = +2.5 V, V_B = –2.5 V		0.55	10	µA
Power Dissipation[8]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = GND		0.018	0.05	mW
Power Supply Sensitivity[5]	P_{SS}	ΔV_{DD} = 5 V ±10%		0.002	0.01	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[5, 9]						
Bandwidth	BW	–3 dB, R_{AB} = 10 kΩ/50 kΩ/100 kΩ		630/130/66		kHz
Total Harmonic Distortion	THD_W	V_A = 1 Vrms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.04		%
Total Harmonic Distortion	THD_W	V_A = 1 Vrms, V_B = 0 V, f = 1 kHz, R_{AB} = 50 kΩ, 100 kΩ		0.015		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, V_W = 0.50% error band, Code 000_H to 200_H for R_{AB} = 10 kΩ/50 kΩ/100 kΩ		0.6/2.2/3.8		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		9		nV/√Hz
Crosstalk (C_{W1}/C_{W2})	C_T	$V_A = V_{DD}$, V_B = 0 V, Measure V_W with Adjacent RDAC Making Full-Scale Code Change		–1		nV–s
Analog Crosstalk (C_{W1}/C_{W2})	C_{TA}	$V_{DD} = V_{A1}$ = +2.5 V, $V_{SS} = V_{B1}$ = –2.5 V, Measure V_{W1} with V_{W2} = 5 V p-p @ f = 10 kHz, Code1 = 20_H, Code 2 = $3F_H$, R_{AB} = 10 kΩ/50 kΩ/100 kΩ		–86/–73/–68		dB
INTERFACE TIMING CHARACTERISTICS (Applies to all parts)[5, 10]						
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulsewidth	t_4, t_5	Clock Level High or Low	10			ns
Data Setup Time	t_6	From Positive CLK Transition	5			ns
Data Hold Time	t_7	From Positive CLK Transition	5			ns
$\overline{CS}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[11]	t_{10}	R_P = 2.2 kΩ, C_L < 20 pF			50	ns
CLK to SDO Data Hold Time	t_{11}	R_P = 2.2 kΩ, C_L < 20 pF	0			ns
$\overline{CS}$ High Pulsewidth[12]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[12]	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.1	0.15	ms
Read/Store to Nonvolatile EEMEM[13]	t_{16}	Applies to Command 2_H, 3_H, 9_H			25	ms
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ns
Preset Pulsewidth (Asynchronous)	t_{PRW}	Not Shown in Timing Diagram	50			ns
Preset Response Time to RDY High	t_{PRESP}	$\overline{PR}$ Pulsed Low to Refreshed Wiper Positions		70		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[14]			100			K Cycles
Data Retention[15]				100		Years

NOTES

[1]Typicals represent average readings at 25°C and V_{DD} = 5 V.

[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. $I_W \cong 50\ \mu A$ @ V_{DD} = 2.7 V for the R_{AB} = 10 kΩ version, $I_W \cong 50\ \mu A$ for the R_{AB} = 50 kΩ and $I_W \cong 25\ \mu A$ for the R_{AB} = 100 kΩ version. See Test Circuit 1.

[3]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = V_{SS}$. DNL specification limits of –1 LSB minimum are Guaranteed Monotonic operating conditions. See Test Circuit 2.

[4]Resistor terminals A, B, and W have no limitations on polarity with respect to each other. Dual Supply Operation enables ground referenced bipolar signal adjustment.

[5]Guaranteed by design and not subject to production test.

[6]Common mode leakage current is a measure of the DC leakage from any terminal B and W to a common mode bias level of $V_{DD}/2$.

[7]Transfer (XFR) Mode current is not continuous. Current consumed while EEMEM locations are read and transferred to the RDAC register. See TPC 19.

[8]P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$)

[9]All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = –2.5 V

[10]See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both V_{DD} = 3 V and 5 V.

[11]Propagation delay depends on value of V_{DD}, R_{PULL_UP}, and C_L see applications text.

[12]Valid for commands that do not activate the RDY pin.

[13]RDY pin low only for commands 2, 3, 8, 9, 10, and the $\overline{PR}$ hardware pulse: CMD_8 ≅ 1 ms; CMD_9, 10 ≅ 0.12 ms; CMD_2, 3 ≅ 20 ms. Device operation at T_A = –40°C and V_{DD} < 3 V extends the save time to 35 ms.

[14]Endurance is qualified to 100,000 cycles as per JEDEC Std. 22, Method A117 and measured at –40°C, +25°C, and +85°C, typical endurance at 25°C is 700,000 cycles.

[15]Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 V will derate with junction temperature as shown in Figure 11 in the Flash/EE Memory description section of this data sheet. The AD5233 contains 9,646 transistors. Die size: 69 mil × 115 mil, 7,993 sq. mil.

Specifications subject to change without notice.

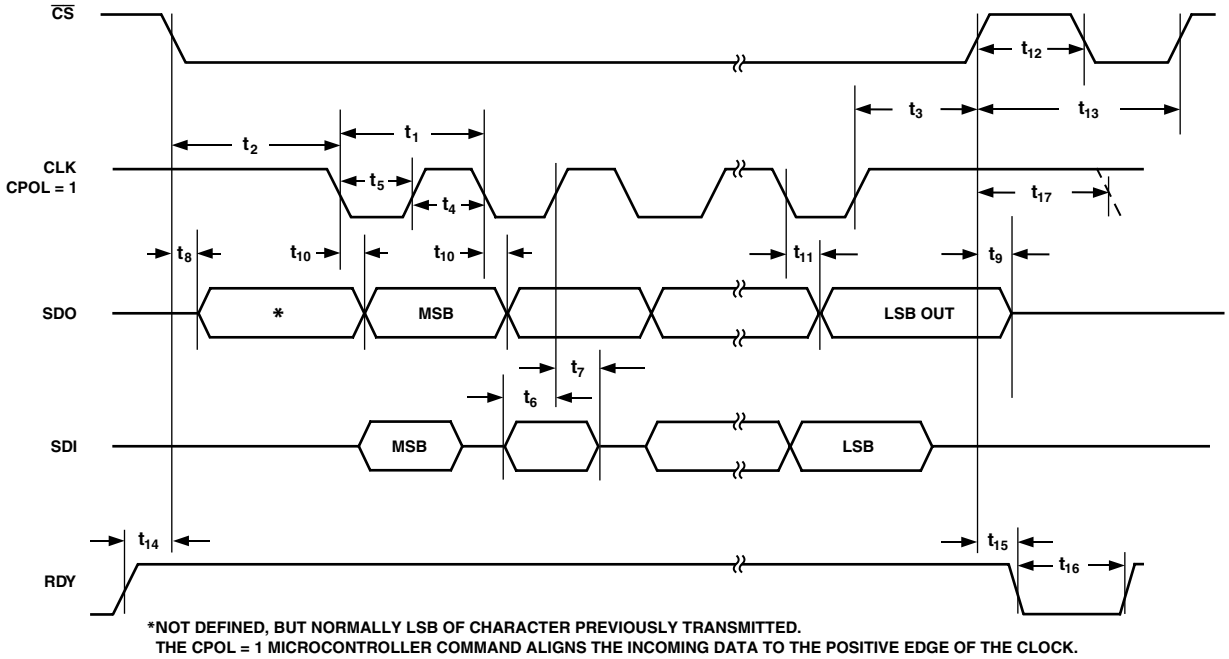


Figure 2a. CPHA = 1 Timing Diagram

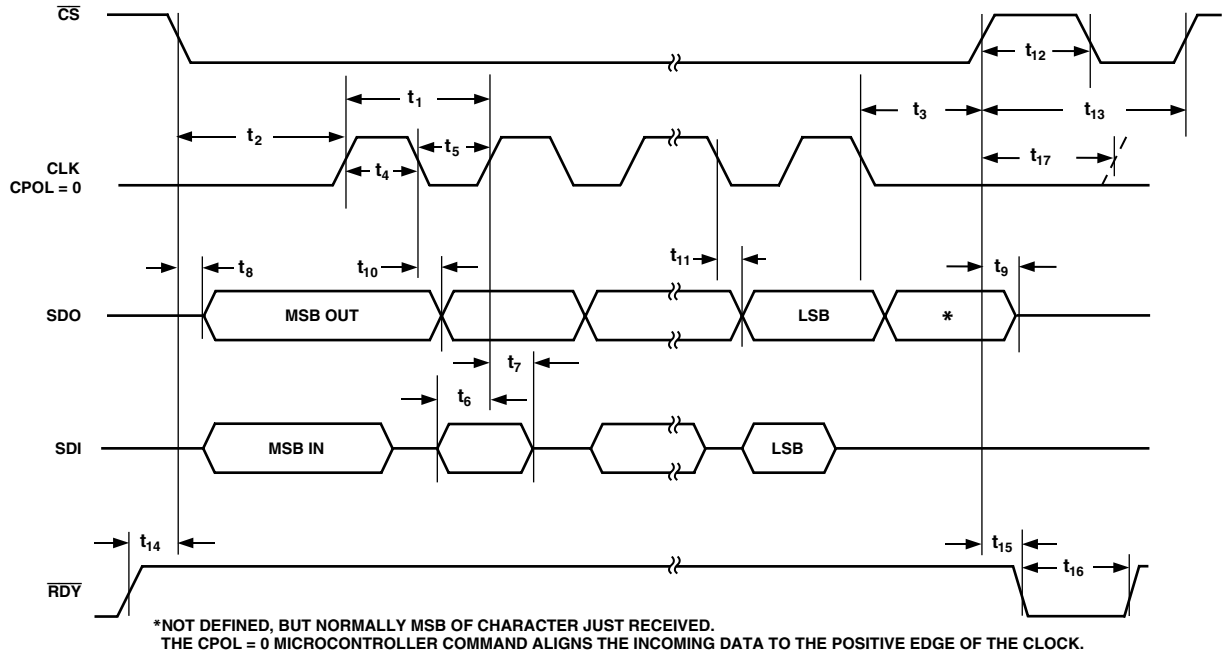


Figure 2b. CPHA = 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND ..... –0.3 V, +7 V
V_{SS} to GND ..... +0.3 V, –7 V
V_{DD} to V_{SS} ..... 7 V
V_A, V_B, V_W to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
A–B, A–W, B–W,
Intermittent[2] ..... ±20 mA
Continuous ..... ±2 mA
Digital Inputs and Output Voltage to GND ..–0.3 V, V_{DD} + 0.3 V
Operating Temperature Range[3] ..... –40°C to +85°C
Maximum Junction Temperature (T_J Max) ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

Thermal Resistance Junction-to-Ambient θ_{JA},
TSSOP-24 ..... 128°C/W
Thermal Resistance Junction-to-Case θ_{JC},
TSSOP-24 ..... 28°C/W
Package Power Dissipation = (T_J Max – T_A)/θ_{JA}

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[3] Includes programming of nonvolatile memory.

ORDERING GUIDE

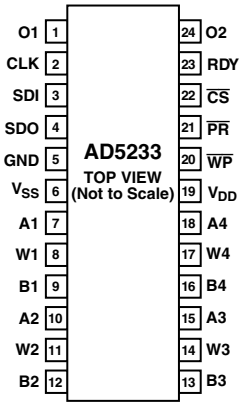
Model	Number of Channels	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity	Top Mark*
AD5233BRU10	4	10	–40°C to +85°C	TSSOP-24	RU-24	96	5233B10
AD5233BRU10-REEL7	4	10	–40°C to +85°C	TSSOP-24	RU-24	1,000	5233B10
AD5233BRU50	4	50	–40°C to +85°C	TSSOP-24	RU-24	96	5233B50
AD5233BRU50-REEL7	4	50	–40°C to +85°C	TSSOP-24	RU-24	1,000	5233B50
AD5233BRU100	4	100	–40°C to +85°C	TSSOP-24	RU-24	96	5233BC
AD5233BRU100-REEL7	4	100	–40°C to +85°C	TSSOP-24	RU-24	1,000	5233BC

*Line 1 contains ADI logo symbol and the date code YYWW, line 2 contains detail model number listed in this column.

CAUTION

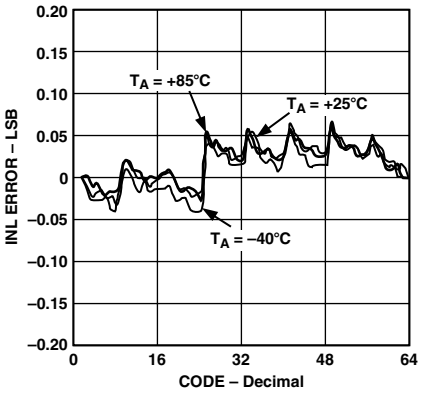
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5233 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

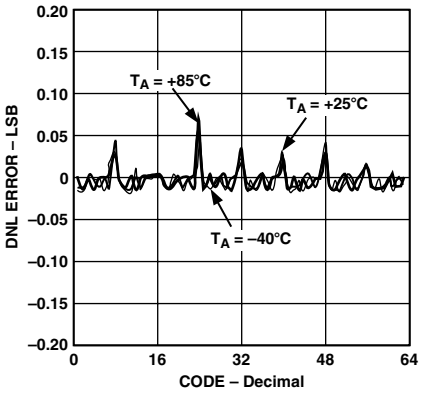


PIN FUNCTION DESCRIPTIONS

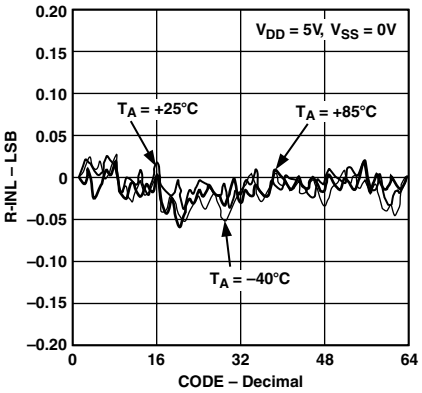
Pin No.	Mnemonic	Description
1	O1	Nonvolatile Digital Output #1. Address(O1) = 4_H, data bit position D0, Defaults to logic 1 initially.
2	CLK	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges.
3	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.
4	SDO	Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 and 10 activate the SDO output. See Table III, Instruction Operation Truth Table. Other commands shift out the previously loaded SDI bit pattern delayed by 16 clock pulses. This allows daisy-chain operation of multiple packages.
5	GND	Ground Pin, Logic Ground Reference
6	V_{SS}	Negative Supply. Connect to 0 V for single supply applications.
7	A1	A Terminal of RDAC1
8	W1	Wiper Terminal of RDAC1, address(RDAC1) = 0_H
9	B1	B Terminal of RDAC1
10	A2	A Terminal of RDAC2
11	W2	Wiper Terminal of RDAC2, address(RDAC2) = 1_H
12	B2	B Terminal of RDAC2
13	B3	B Terminal of RDAC3
14	W3	Wiper Terminal of RDAC3, address(RDAC3) = 2_H
15	A3	A Terminal of RDAC3
16	B4	B Terminal of RDAC4
17	W4	Wiper Terminal of RDAC4, address(RDAC4) = 3_H
18	A4	A Terminal of RDAC4
19	V_{DD}	Positive Power Supply Pin
20	$\overline{WP}$	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents except $\overline{PR}$ strobe, CMD_1, and CMD_8 will refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high.
21	$\overline{PR}$	Hardware Override Preset Pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 32_{10} until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
22	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
23	RDY	Ready. Active high open drain output. Identifies completion of commands 2, 3, 8, 9, 10, and $\overline{PR}$.
24	O2	Nonvolatile Digital Output #2. Address(O2) = 4_H, data bit position D1, Defaults to logic 1 initially.



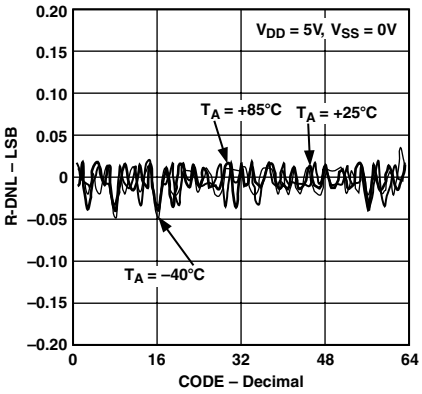
TPC 1. INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



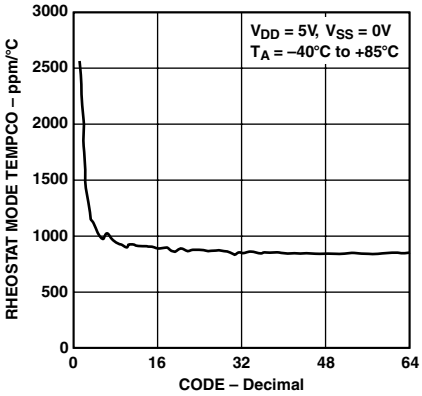
TPC 2. DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



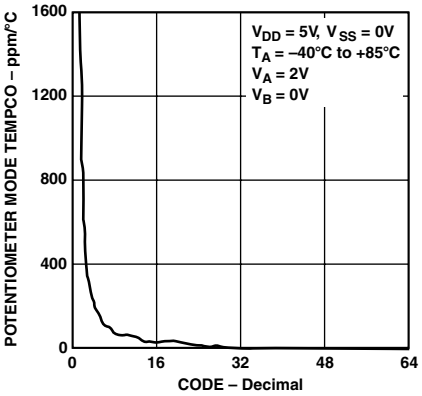
TPC 3. R-INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



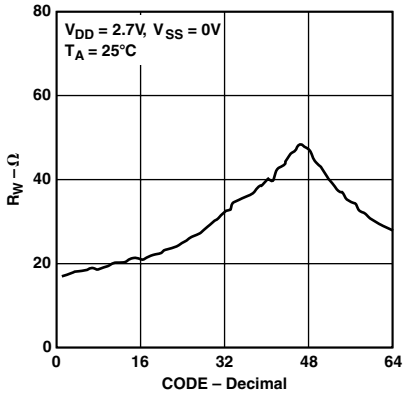
TPC 4. R-DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



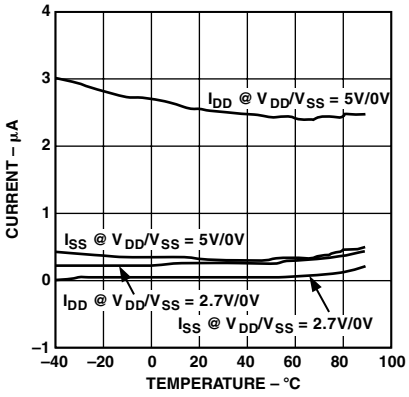
TPC 5. $\Delta R_{WB}/\Delta T$ vs. Code, R_{AB} = 10 kΩ



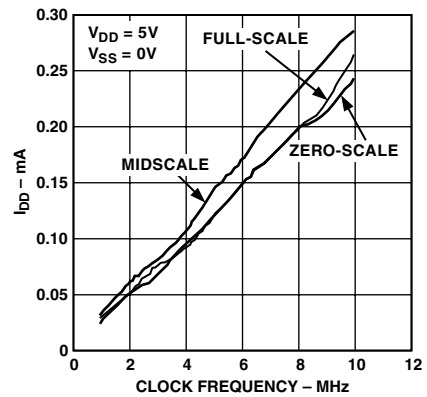
TPC 6. $\Delta V_{WB}/\Delta T$ vs. Code, R_{AB} = 10 kΩ



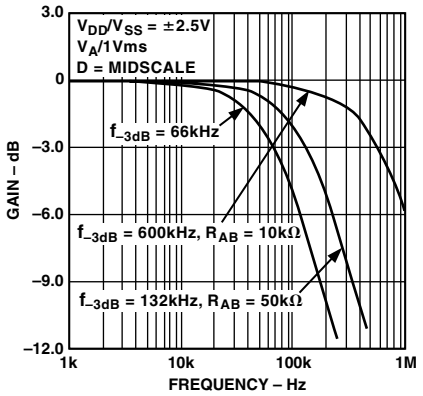
TPC 7. Wiper On-Resistance vs. Code



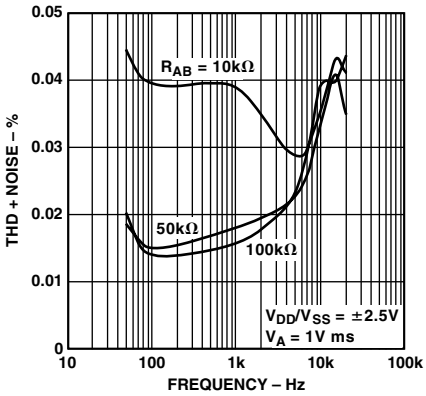
TPC 8. I_{DD} vs. Temperature, R_{AB} = 10 kΩ



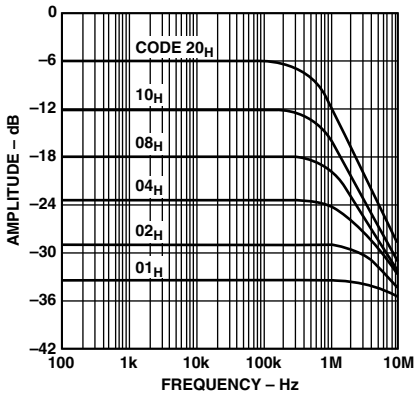
TPC 9. I_{DD} vs. Clock Frequency, R_{AB} = 10 kΩ



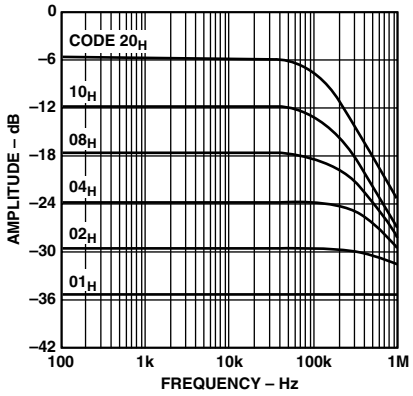
TPC 10. –3 dB Bandwidth vs. Resistance. Test Circuit 7.



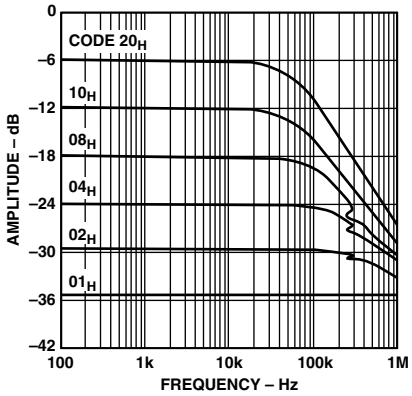
TPC 11. Total Harmonic Distortion vs. Frequency



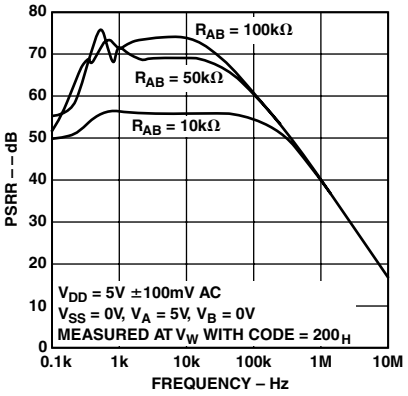
TPC 12. Gain vs. Frequency vs. Code, R_{AB} = 10 Ω. Test Circuit 7.



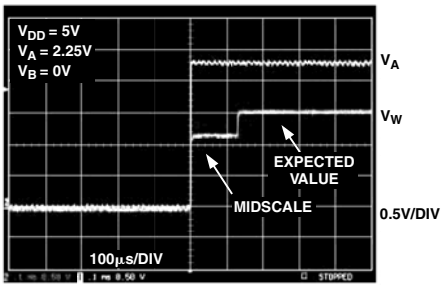
TPC 13. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ. Test Circuit 7.



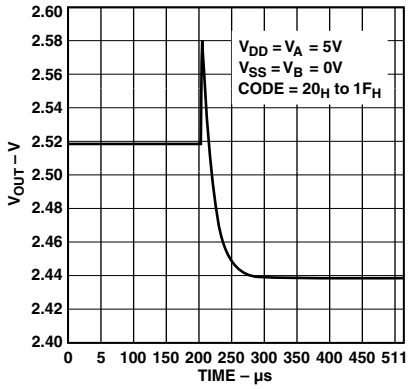
TPC 14. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ. Test Circuit 7.



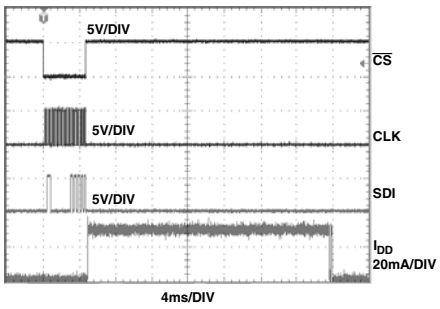
TPC 15. PSRR vs. Frequency



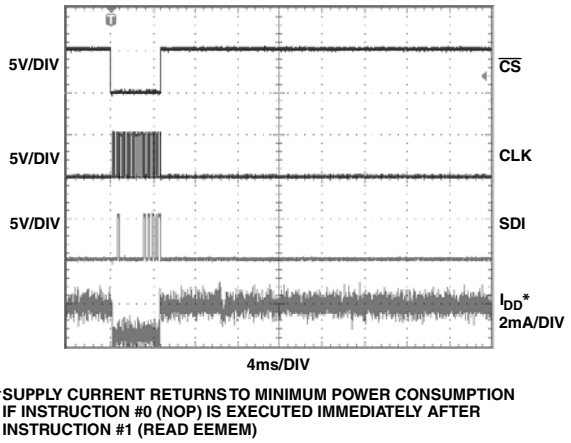
TPC 16. Power-On Reset, V_A = 2.25 V, Code = 101010_B



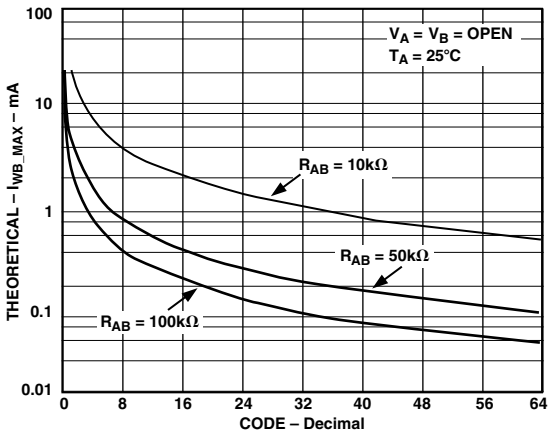
TPC 17. Midscale Glitch Energy, Code 20_H to $1F_H$



TPC 18. I_{DD} vs. Time (Save) Program Mode



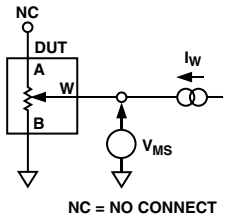
TPC 19. I_{DD} vs. Time (Read) Program Mode



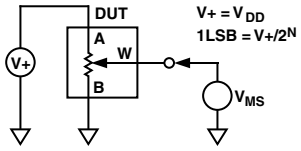
TPC 20. I_{MAX} vs. Code

TEST CIRCUITS

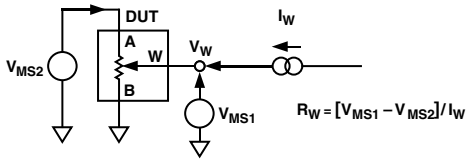
Test Circuits 1 to 10 define the test conditions used in the product specification's table.



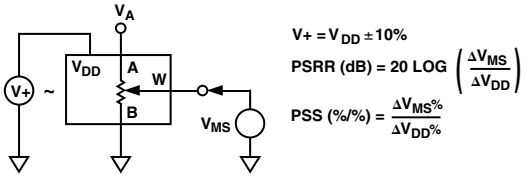
Test Circuit 1. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)



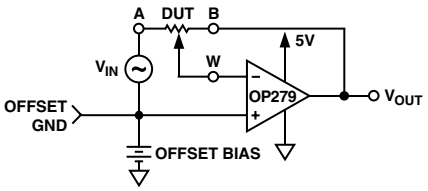
Test Circuit 2. Potentiometer Divider Nonlinearity Error (INL, DNL)



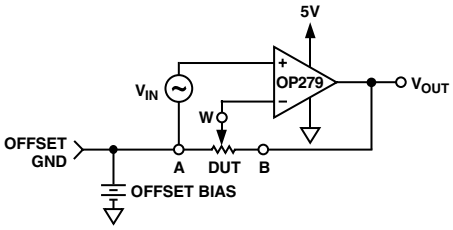
Test Circuit 3. Wiper Resistance



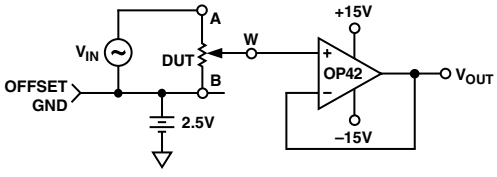
Test Circuit 4. Power Supply Sensitivity (PSS, PSRR)



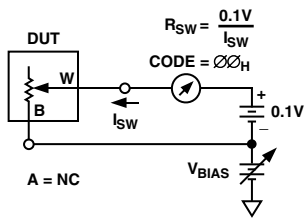
Test Circuit 5. Inverting Gain



Test Circuit 6. Noninverting Gain

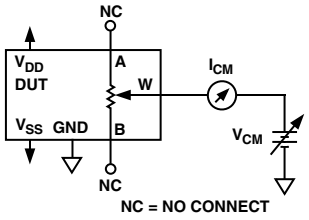


Test Circuit 7. Gain vs. Frequency

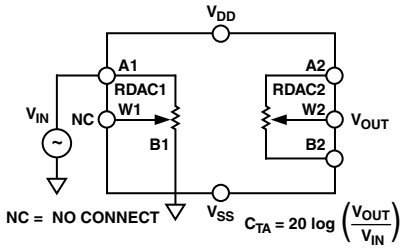


Test Circuit 8. Incremental ON Resistance

TEST CIRCUITS (continued)



Test Circuit 9. Common-Mode Leakage Current



Test Circuit 10. Analog Crosstalk

OPERATIONAL OVERVIEW

The AD5233 digital potentiometer is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The basic voltage range is limited to a $|V_{DD} - V_{SS}| < 5.5$ V. The digital potentiometer wiper position is determined by the RDAC register contents. The RDAC register acts as a scratch pad register allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The scratch pad register can be programmed with any position value using the standard SPI serial interface mode by loading the complete representative data word. Once a desirable position is determined this value can be saved into a EEMEM register. Thereafter the wiper position will always be set at that position for any future ON-OFF-ON power supply sequence. The EEMEM save process takes approximately 25 ms, during this time the shift register is locked preventing any changes from taking place. The RDY pin indicates the completion of this EEMEM save.

There are 16 instructions which facilitates users' programming needs, (refer to Table III). The instructions are:

0. Do nothing
1. Restore EEMEM setting to RDAC
2. Save RDAC setting to EEMEM
3. Save user data or RDAC setting to EEMEM
4. Decrement 6 dB
5. Decrement all 6 dB
6. Decrement one step
7. Decrement all one step
8. Reset EEMEM setting to RDAC
9. Read EEMEM to SDO
10. Read Wiper Setting to SDO
11. Write data to RDAC
12. Increment 6 dB
13. Increment all 6 dB
14. Increment one step
15. Increment all one step

Scratch Pad and EEMEM Programming

The scratch pad register (RDAC register) directly controls the position of the digital potentiometer wiper. When the scratch pad register is loaded with all zeros the wiper will be connected to the B-Terminal of the variable resistor. When the scratch pad register is loaded with midscale code (one-half of full-scale position) the wiper will be connected to the middle of the variable resistor. And when the scratch pad is loaded with full-scale code, all one's, the wiper will connect to the A-Terminal. Since the scratch pad register is a standard logic register, there is no restriction on the number of changes allowed. The EEMEM registers have a program erase/write cycle limitation described in the Flash/EEMEM Reliability section.

Basic Operation

The basic mode of setting the variable resistor wiper position (programming the scratch pad register) is accomplished by loading the serial data input register with the command instruction #11, which includes the desired wiper position data. When the desired wiper position is determined, the user may load the serial data input register with the command instruction #2, which makes a copy of the desired wiper position data into the nonvolatile EEMEM register. After 25 ms the wiper position will be permanently stored in the nonvolatile EEMEM location. Table I provides an application-programming example listing the sequence of serial data input (SDI) words and the serial data output appearing at the SDO pin in hexadecimal format.

Table I. Set and Save RDAC data to EEMEM Register

SDI	SDO	Action
$B010_H$	$XXXX_H$	Loads data 10_H into RDAC1 register, Wiper W1 moves to 1/4 full-scale position.
$20xx_H$	$B010_H$	Saves copy of RDAC1 register contents into EEMEM1 register.

At system power ON, the scratch pad register is automatically refreshed with the value last saved in the EEMEM register. The factory preset EEMEM value is midscale but thereafter, the EEMEM value can be changed by user.

During operation, the scratch pad (wiper) register can also be refreshed with the current contents of the nonvolatile EEMEM register under hardware control by pulsing the $\overline{PR}$ pin without activating instruction 1 or 8. Beware that the $\overline{PR}$ pulse first sets the wiper at midscale when brought to logic zero, and then on the positive transition to logic high, it reloads the RDAC wiper register with the contents of EEMEM. Many additional advanced programming commands are available to simplify the variable resistor adjustment process (see Table III). For example, the wiper position can be changed one step at a time by using the Increment/Decrement instruction or by 6 dB at a time with the Shift Left/Right instruction command. Once an Increment, Decrement or Shift command has been loaded into the shift register, subsequent $\overline{CS}$ strobes will repeat this command. This is useful for push button control applications. See the advanced control modes section following the Instruction Operation Truth Table. A serial data output SDO pin is available for daisy chaining and for readout of the internal register contents. The serial input data register uses a 24-bit [instruction/address/data] WORD format.

EEMEM Protection

Write protect ($\overline{WP}$) disables any changes of the scratch pad register contents regardless of the software commands, except that the EEMEM setting can be refreshed and overwrite $\overline{WP}$ by using commands 8 and $\overline{PR}$. pulse. Therefore, the write-protect ($\overline{WP}$) pin provides a hardware EEMEM protection feature. To disable $\overline{WP}$, it is recommended to execute a NOP command before returning $\overline{WP}$ to logic high.

Digital Input/Output Configuration

All digital inputs are ESD protected high input impedance that can be driven directly from most digital sources. Active at logic low, $\overline{PR}$ and $\overline{WP}$ must be biased to V_{DD} if they are not used. There are no internal pull-up resistors present on any digital input pins. Since the device may be detached from the driving source once it is programmed, adding pull-up resistance in the digital input pins is a good way to avoid falsely triggering the floating pins in a noisy environment.

The SDO and RDY pins are open drain digital outputs where pull-up resistors are needed only if using these functions. A resistor value in the range of 1 kΩ to 10 kΩ is a proper choice which balances the power and switching speed trade off.

Serial Data Interface

The AD5233 contains a four-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). The AD5233 uses a 16-bit serial data word loaded MSB first. The format of the SPI-compatible word is shown in Table II. The chip select $\overline{CS}$ pin needs to be held low until the complete data word is loaded into the SDI pin. When $\overline{CS}$ returns high, the serial data word is decoded according to the instructions in Table III. The Command Bits (Cx) control the operation of the digital potentiometer. The Address Bits (Ax) determine which register is activated. The Data Bits (Dx) are the values that are loaded into the decoded register. To program RDAC 1–4, only the 6 LSB databits are used. Table V provides an address map of the EEMEM locations. The last instruction executed prior to a period of no programming activity should be the No Operation (NOP) instruction 0. This will place the internal logic circuitry in a minimum power dissipation state.

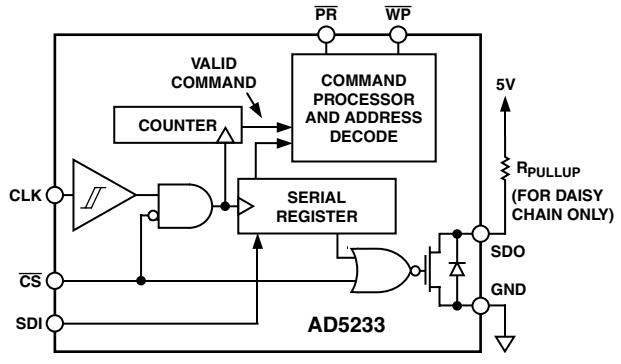


Figure 3. Equivalent Digital Input-Output Logic

The equivalent serial data input and output logic is shown in Figure 3. The open drain output SDO is disabled whenever chip select $\overline{CS}$ is logic high. The SPI interface can be used in two slave modes CPHA = 1, CPOL = 1, and CPHA = 0, CPOL = 0. CPHA, and CPOL refer to the control bits, which dictate SPI timing in these MicroConverter®s and microprocessors: ADuC812/824, M68HC11, and MC68HC16R1/916R1. ESD protection of the digital inputs is shown in Figures 4a and 4b.

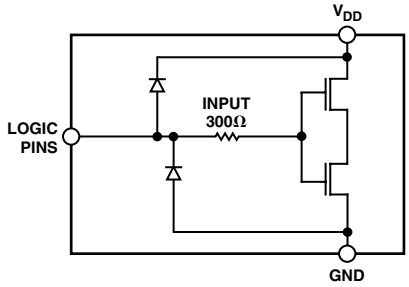


Figure 4a. Equivalent ESD Digital Input Protection

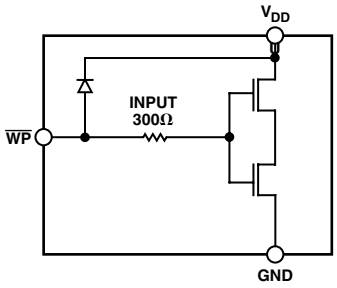


Figure 4b. Equivalent $\overline{WP}$ Input Protection

Daisy-Chain Operation

The serial data output pin (SDO) serves two purposes. It can be used to read out the contents of the wiper setting and EEMEM values using instructions 10 and 9 respectively. The remaining 14 instructions (#0–#8, #11–#15) are valid for daisy chaining multiple devices in simultaneous operations. Daisy chaining minimizes the number of port pins required from the controlling IC (see Figure 5). The SDO pin contains an open drain N-Ch FET that requires a pull-up resistor, if this function is used. As shown in Figure 5, users need to tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may require an additional time delay between subsequent packages. When two AD5233s are daisy chained 32 bits of data are required. The first 16 bits go to U2 and the second 16 bits go to U1. The 16 bits are formatted to contain the 4-bit instruction, followed by the 4-bit address, then 8-bits of data. The $\overline{CS}$ should be kept low until all 32 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation.

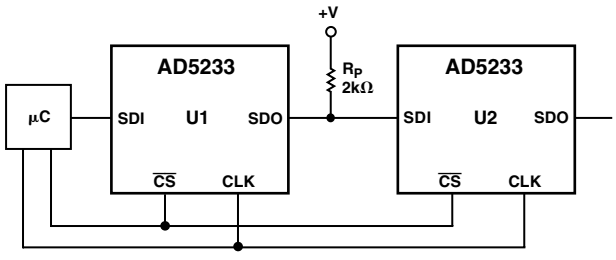


Figure 5. Daisy Chain Configuration Using SDO

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Table II. 16-Bit Serial Data Word

	MSB			Instruction Byte					LSB		Data Byte					
RDAC	C3	C2	C1	C0*	0	0	A1	A0	X	X	D5	D4	D3	D2	D1	D0
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

*Command bits are C0 to C3. Address bits are A3-A0. Data bits D0 to D5 are applicable to RDAC wiper register whereas D0 to D7 are applicable to EEMEM register. Command instruction codes are defined in Table III.

Table III. Instruction Operation Truth Table[1, 2, 3]

Inst. No.	Instruction Byte 0 B16 C3	C2	C1	C0	A3	A2	A1	B8 A0	Data Byte 0 B7 D7	B6 D6	B5 D5	B4 D4	B3 D3	B2 D2	B1 D1	B0 D0	Operation
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: Do Nothing. See Table X for programming example.
1	0	0	0	1	0	0	A1	A0	X	X	X	X	X	X	X	X	Write content of EEMEM to RDAC Register. This command leaves device in the Read Program power state. To return part to the idle state, perform NOP instruction #0. See Table X.
2	0	0	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	SAVE WIPER SETTING: Write contents of RDAC at address A1 A0 to EEMEM. See Table IX.
3[4]	0	0	1	1	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of Serial Register Data Byte 0 (total 8-bit) to EEMEM(ADDR). See Table XII.
4[5]	0	1	0	0	0	0	A1	AO	X	X	X	X	X	X	X	X	Decrement 6 dB: Right Shift contents of RDAC Register, stops at all "Zeros."
5[5]	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement all 6 dB: Right Shift contents of all RDAC Registers, stops at all "Zeros."
6[5]	0	1	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Decrement content of RDAC Register by "One," stops at all "Zero."
7[5]	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement contents of all RDAC Registers by "One," stops at all "Zero."
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	RESET: Load all RDACs with their corresponding EEMEM previously-saved values
9	1	0	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	X	Transfer content of EEMEM(ADDR) to Serial Register Data Byte 0 and previously stored data can be read out from SDO pin. See Table XIII.
10	1	0	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Transfer content of RDAC (ADDR) to Serial Register Data Byte 0 and wiper setting can be read out from SDO pin. See Table XIV.
11	1	0	1	1	0	0	A1	A0	X	X	D5	D4	D3	D2	D1	D0	Write content of Serial Register Data Byte 0 (total 6-bit) to RDAC. See Table VIII.
12[5]	1	1	0	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Increment 6 dB: Left Shift content of RDAC Register, stops at all "Ones." See Table XI.
13[5]	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment all 6 dB: Left Shift contents of RDAC Registers, stops at all "Ones."
14[5]	1	1	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Increment content of RDAC Register by "One," stops at all "Ones." See Table IX.
15[5]	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment contents of all RDAC Registers by "One," stops at all "Ones."

NOTES
[1]The SDO output shifts out the last 16-bits of data clocked into the serial register for daisy-chain operation. Exception, any instruction that follows Instruction #9 or #10, see details of these instruction for proper usage.
[2]The RDAC register is a volatile scratch pad register that is automatically refreshed at power ON from the corresponding non-volatile EEMEM register.
[3]Execution of the above Operations takes place when the $\overline{CS}$ strobe returns to logic high.
[4]Instruction #3 write one data byte (8-bit data) to EEMEM. But in the cases of addresses 0, 1, 2, 3 only the last 6 bits are valid for wiper position setting.
[5]The increment, decrement and shift commands ignore the contents of the shift register Data Byte 0.

Terminal Voltage Operation Range

The AD5233 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes (see Figure 6).

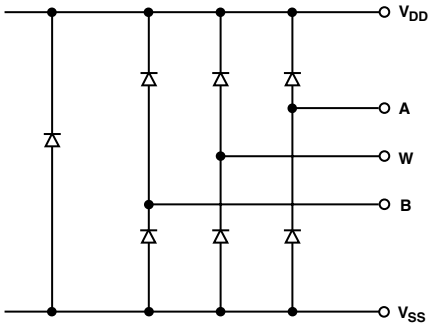


Figure 6. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5233 device is primarily used as a digital ground reference that needs to be tied to the PCB's common ground. The digital input control signals to the AD5233 must be referenced to the device ground pin (GND), and satisfy the logic level defined in the specification table of this data sheet. An internal level shift circuit ensures that the common-mode voltage range of the three-terminals extends from V_{SS} to V_{DD} regardless of the digital input level.

Power Up Sequence

Since there are diodes to limit the voltage compliance at terminals A, B, and W (see Figure 6) it is important to power V_{DD}/V_{SS} first before applying any voltages to terminals A, B, and W. Otherwise, the diode will be forward biased such that V_{DD}/V_{SS} will be powered unintentionally. For example, applying 5 V across terminals A and B prior to V_{DD} will cause the V_{DD} terminal to exhibit 4.3 V. It is not destructive to the device, but it may affect the rest of the user's system. As a result, the ideal power up sequence is in the following order: GND, V_{DD}, V_{SS}, Digital Inputs, and $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and Digital Inputs is not important as long as they are powered after V_{DD}/V_{SS}.

Regardless of the power up sequence and the ramp rates of the power supplies, once V_{DD}/V_{SS} are powered, the power-on reset remains effective, which retrieves EEMEM saved values to the RDAC registers.

Latched Digital Outputs

A pair of digital outputs, O1 and O2, are available on the AD5233 that provide a nonvolatile logic 0 or logic 1 setting. O1 and O2 are standard CMOS logic outputs shown in Figure 7. These outputs are ideal to replace functions often provided by DIP switches. In addition, they can be used to drive other standard CMOS logic controlled parts that need an occasional setting change. O1 and O2, are defaulted to logic 1 initially.

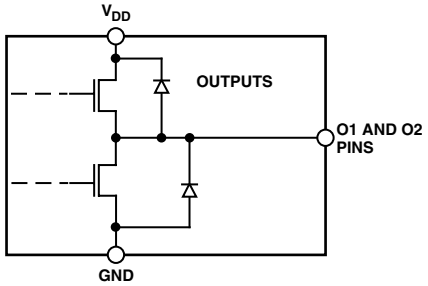


Figure 7. Logic Outputs O1 and O2.

ADVANCED CONTROL MODES

The AD5233 digital potentiometer contains a set of user programming features to address the wide applications available to these universal adjustment devices. Key programming features include:

- Scratch Pad Programming to any desirable values
- Nonvolatile memory storage of the present scratch pad RDAC register value into the EEMEM register
- Increment and Decrement instructions for RDAC wiper register
- Left and right Bit Shift of RDAC wiper register to achieve 6 dB level changes
- Eleven extra bytes of user addressable nonvolatile memory

Linear Increment and Decrement Commands

The increment and decrement commands (#14, #15, #6, #7) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to just send an increment or decrement command to the device. For the increment command, executing instruction #14 with proper address will automatically move the wiper to the next resistance segment position. Instruction #15 performs the same function except that address does not need to be specified. All RDACs are changed at the same time.

Logarithmic Taper Mode Adjustment (±6 dB/Step)

Four programming instructions produce logarithmic taper increment and decrement wiper. These settings are activated by the 6 dB increment and 6 dB decrement instructions #12, #13, #4, and #5 respectively. For example, starting at zero scale, executing eight increment instructions #12 will move the wiper in 6 dB per step from the 0% to full scale R_{AB}. The 6 dB increment instruction doubles the value of the RDAC register content each time the command is executed. When the wiper position is near the maximum setting, the last 6 dB increment instruction causes the wiper to go to the full-scale 63_{10} code position. Further 6 dB per increment instruction will no longer change the wiper position beyond its full scale. 6 dB step increment and decrement are achieved by shifting the bit internally to the left and right respectively. The following information explains the nonideal ±6 dB step adjustment at certain conditions. Table IV illustrates the operation of the shifting function on the RDAC register data bits. Each line going down the table represents a successive shift operation. Note that the left shift #12 and #13 commands were modified such that if the data in the RDAC register is equal to zero, and the data is left shifted, the RDAC register is then set

to code 1. Similarly, if the data in the RDAC register is greater than or equal to mid-scale, and the data is left shifted, then the data in the RDAC register is automatically set to full-scale. This makes the left shift function as ideal logarithmic adjustment as is possible.

The right shift #4 and #5 commands will be ideal only if the LSB is zero (i.e. ideal logarithmic—no error). If the LSB is a one then the right shift function generates a linear half LSB error, which translates to a numbers of bits dependent logarithmic error as shown in Figure 8. The plot shows the error of the odd numbers of bits for AD5233.

Table IV. Detail Left and Right Shift Functions for 6 dB Step Increment and Decrement

Left Shift (+6 dB/Step) ↓

Left Shift	Right Shift
00 0000	11 1111
00 0001	01 1111
00 0010	00 1111
00 0100	00 0111
00 1000	00 0011
01 0000	00 0001
10 0000	00 0000
11 1111	00 0000
11 1111	00 0000

↓ Right Shift (–6 dB/Step)

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each Right Shift #4 and #5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in Figure 8 shows plots of Log_Error [i.e. $20 \times \log_{10}$ (error/code)] AD5233. For example, code 3 Log_Error = $20 \times \log_{10}$ (0.5/3) = –15.56 dB, which is the worst case. The plot of Log_Error is more significant at the lower codes.

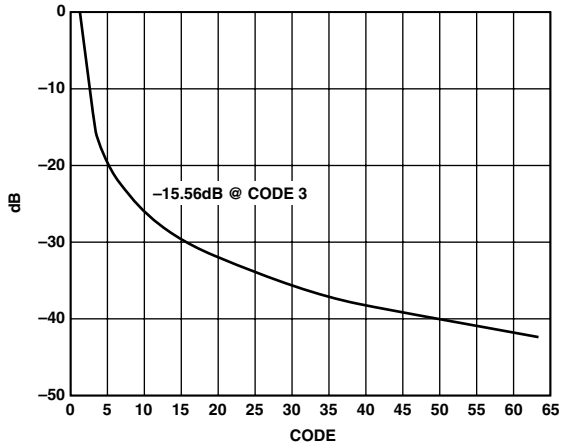


Figure 8. Plot of Log_Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits is Ideal)

The AD5233 contains additional internal user storage registers (EEMEM) for saving constants and other 8-bit data. Table V provides an address map of the internal storage registers shown in the functional block diagram as EEMEM1, EEMEM2, and 11 bytes of USER EEMEM.

Table V. EEMEM Address Map

EEMEM Number	Address	EEMEM Content For
1	0000	RDAC1[1, 2]
2	0001	RDAC2[1, 2]
3	0010	RDAC3[1, 2]
4	0011	RDAC4[1, 2]
5	0100	O1 and O2[3]
6	0101	USER1[4]
7	0110	USER2
:	:	:
15	1110	USER10
16	1111	USER11

NOTES
[1]RDAC data stored in the EEMEM location is transferred to the RDAC REGISTER at Power ON, or when instructions Inst#1, #8, and $\overline{PR}$ are executed.
[2]Execution of instruction #1 leaves the device in the Read Mode power consumption state. After the last Instruction #1 is executed, the user should perform a NOP, Instruction #0 to return the device to the low power idling state.
[3]O1 and O2 data stored in EEMEM locations are transferred to their corresponding DIGITAL REGISTER at Power ON, or when instructions #1 and #8 are executed.
[4]USER <#> are internal nonvolatile EEMEM registers available to store and retrieve constants and other 8-bit information using Inst#3 and Inst#9 respectively.

RDAC STRUCTURE

The patent pending RDAC contains multiple strings of equal resistor segments, with an array of analog switches, that act as the wiper connection. The number of positions is the resolution of the device. The AD5233 has 64 connection points allowing it to provide better than 1.5% set ability resolution. Figure 9 shows an equivalent structure of the connections between the three terminals of the RDAC. The SW_A and SW_B will always be ON, while one of the switches SW(0) to SW($2^N - 1$) will be ON one at a time depending on the resistance position decoded from the Data Bits. Since the switch is not ideal, there is a 15 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage or the higher the temperature, the higher the resulting wiper resistance. Users should be aware of the wiper resistance dynamics if accurate prediction of the output resistance is needed.

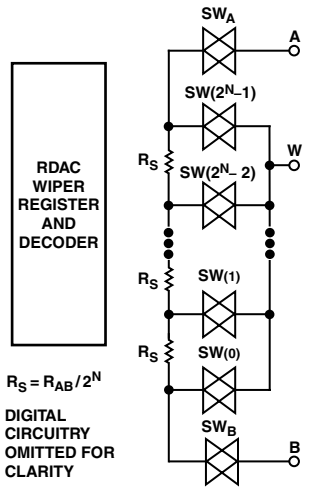


Figure 9. Equivalent RDAC Structure (Patent Pending)

PROGRAMMING THE VARIABLE RESISTOR

RHEOSTAT OPERATION

The nominal resistance of the RDAC between terminals A-and-B, R_{AB}, are available with 10 kΩ, 50 kΩ and 100 kΩ with 64 positions (6-bit resolution). The final digit(s) of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50, 100 kΩ = 100.

The 6-bit data word in the RDAC latch is decoded to select one of the 64 possible settings. The following discussion describes the calculation of resistance R_{WB} at different codes of a 10 kΩ part. For V_{DD} = 5 V, the wipers first connection starts at the B terminal for data 00_H. $R_{WB}(0)$ is 15 Ω because of the wiper resistance and it is independent to the nominal resistance. The second connection is the first tap point where $R_{WB}(1)$ becomes 156 Ω + 15 Ω = 171 Ω for data 01_H. The third connection is the next tap point representing $R_{WB}(2)$ = 312 + 15 = 327 Ω for data 02_H and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(63)$ = 9858 Ω. See Figure 9 for a simplified diagram of the equivalent RDAC circuit. When R_{WB} is used, the A-terminal can be let floating or tied to the wiper.

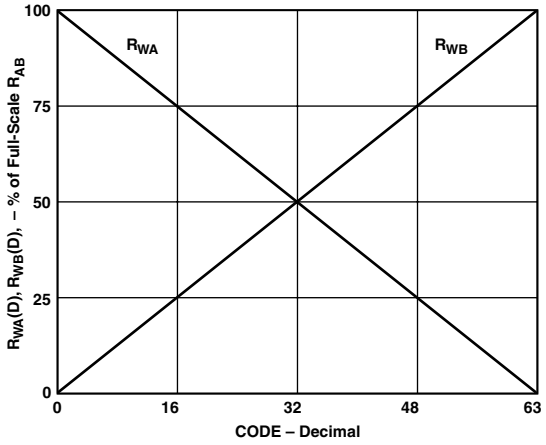


Figure 10. $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

The general equation, which determines the programmed output resistance between W and B, is:

$$R_{WB}(D) = \frac{D}{64} \times R_{AB} + R_W \quad (1)$$

Where *D* is the decimal equivalent of the data contained in the RDAC register, R_{AB} is the Nominal Resistance between terminals A-and-B, and R_W is the wiper resistance.

For example, the following output resistance values will be set for the following RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ Digital Potentiometers):

Table VI. $R_{WB}(D)$ at Selected Codes for R_{AB} = 10 kΩ

D (DEC)	$R_{WB}(D)$ (Ω)	Output State
63	9858	Full-scale
32	5015	Mid-scale
1	171	1 LSB
0	15	Zero-scale (Wiper contact resistance)

Note that in the zero-scale condition a finite wiper resistance of 15 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

Like the mechanical potentiometer the RDAC replaces, the AD5233 parts are totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. Figure 10 shows the symmetrical programmability of the various terminal connections. When R_{WA} is used, the B–terminal can be let floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(D) = \frac{64 - D}{64} \times R_{AB} + R_W \quad (2)$$

For example, the following output resistance values will be set for the following RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ Digital Potentiometers):

Table VII. $R_{WA}(D)$ at Selected Codes for R_{AB} = 10 kΩ

D (DEC)	$R_{WA}(D)$ (Ω)	Output State
63	171	Full-scale
32	5015	Mid-scale
1	9858	1 LSB
0	10015	Zero-scale

Channel-to-channel R_{AB} matching is better than 1%. The change in R_{AB} with temperature has a 600 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer can be configured to generate an output voltage at the wiper terminal which is proportional to the input voltages applied to terminals A and B. For example connecting A–terminal to 5 V and B–terminal to ground produces an output voltage at the wiper which can be any value starting at 0 V up to 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 2^N position resolution of the potentiometer divider.

Since AD5233 can also be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltages applied to terminals A and B is:

$$V_W(D) = \frac{D}{64} \times V_{AB} + V_B \quad (3)$$

Equation 3 assumes V_W is buffered so that the effect of wiper resistance is nulled. Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors and not the absolute value, therefore, the drift improves to 15 ppm/°C. There is no voltage polarity restriction between terminals A, B, and W as long as the terminal voltage (V_{TERM}) stays within $V_{SS} < V_{TERM} < V_{DD}$.

PROGRAMMING EXAMPLES

The following programming examples illustrate the typical sequence of events for various features of the AD5233. Users should refer to Table III for the instructions and data word format. The Instruction numbers, addresses, and data appearing at SDI and SDO pins are displayed in hexadecimal format in the following examples.

Table VIII. Scratch Pad Programming

SDI	SDO	Action
$B010_H$	$XXXX_H$ Wiper W1	Loads data 10_H into RDAC1 register, moves to 1/4 full-scale position

Table IX. Incrementing RDAC1 Followed by Storing the Wiper Setting to EEMEM1

SDI	SDO	Action
$B010_H$	$XXXX_H$	Loads data 10_H into RDAC1 register, Wiper W1 moves to 1/4 full-scale position
$E0XX_H$	$B010_H$	Increments RDAC1 register by one to 11_H
$E0XX_H$	$E0XX_H$	Increments RDAC1 register by one to 12_H Continue until desired wiper position reached
$20XX_H$	$XXXX_H$	Saves RDAC1 register data into EEMEM1 Optionally tie $\overline{WP}$ to GND to protect EEMEM values

Table X. Restoring EEMEM1 Value to RDAC1 Register

EEMEM value for RDAC can be restored by Power On, Strobing $\overline{PR}$ pin, or two different commands as shown below

SDI	SDO	Action
$10XX_H$	$XXXX_H$	Restores EEMEM1 value to RDAC1 register
$00XX_H$	$10XX_H$	NOP. Recommended command to minimize power consumption
$8XXX_H$	$00XX_H$	Reset EEMEM1 value to RDAC1 register

Table XI Using Left Shift by One to Increment 6 dB Step

SDI	SDO	Action
$C0XX_H$	$XXXX_H$	Moves wiper to double the present data contained in RDAC1 register

Table XII. Storing Additional User Data in EEMEM

SDI	SDO	Action
$35AA_H$	$XXXX_H$	Stores data AA_H into spare EEMEM6 location USER1 (Allowable to address in 11 locations with maximum 8 bits of Data)
3655_H	$35AA_H$	Stores data 55_H into spare EEMEM7 location USER2. (Allowable to address 11 locations with maximum 8 bits of data)

Table XIII. Reading Back Data from Various Memory Locations

SDI	SDO	Action
$95XX_H$	$XXXX_H$	Prepares data read from USER1 location
$00XX_H$	$95AA_H$	NOP instruction #0 sends 16-bit word out of SDO where the last 8 bits contain the contents of USER1 location. NOP command ensures device returns to idle power dissipation state

Table XIV. Reading Back Wiper Settings

SDI	SDO	Action
$B020_H$	$XXXX_H$	Sets RDAC1 to mid-scale
$C0XX_H$	$B020_H$	Doubles RDAC1 from mid-scale to full-scale (Left Shift Instruction)
$A0XX_H$	$C0XX_H$	Prepares reading wiper setting from RDAC1 register
$XXXX_H$	$A03F_H$	Readback full-scale value from RDAC1 register

FLASH/EEMEM RELIABILITY

The Flash/EE Memory array on the AD5233 is fully qualified for two key Flash/EE memory characteristics, namely Flash/EE Memory Cycling Endurance and Flash/EE Memory Data Retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many Program, Read, and Erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events. These events are defined as:

1. Initial page erase sequence
2. Read/verify sequence
3. Byte program sequence
4. Second read/verify sequence

During reliability qualification Flash/EE memory is cycled from 00_H to $3F_H$ until a first fail is recorded signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the specification pages of this data sheet, the AD5233 Flash/EE Memory Endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of –40°C to +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the AD5233 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described above, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full-specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 V, will derate with T_J as shown in Figure 11. For example, the data is retained for 100 years at 55°C operation, but reduces to 15 years at 85°C operation. Beyond such limit, the part must be reprogrammed so that the data can be restored.

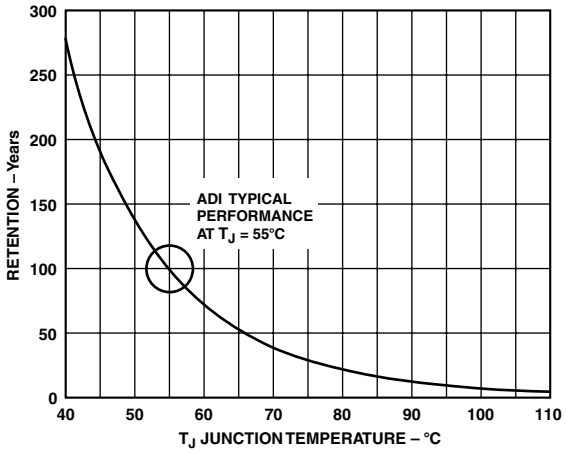


Figure 11. Flash/EE Memory Data Retention

APPLICATIONS

Bipolar Operation From Dual Supplies

The AD5233 can be operated from dual supplies ±2.5 V, which enables control of ground referenced AC signals or bipolar operation. AC signals, as high as V_{DD}/V_{SS}, can be applied directly across terminals A–B with the output taken from terminal W, see Figure 12 for a typical circuit connection.

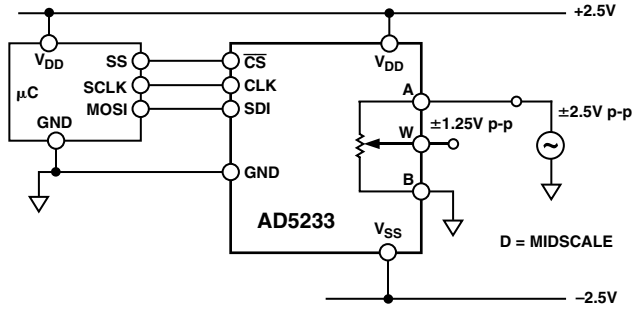


Figure 12. Bipolar Operation from Dual Supplies

Gain Control Compensation

Digital Potentiometer is commonly used in gain control such as the noninverting gain amplifier shown in Figure 13.

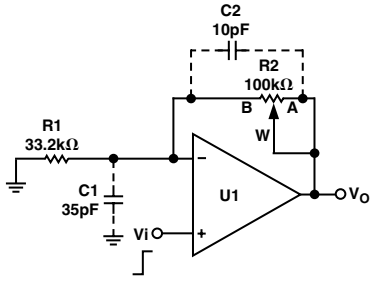


Figure 13. Typical Noninverting Gain Amplifier

Notice that when RDAC B terminal parasistic capacitance is connected to the op amp noninverting node, it introduces a zero for the $1/\beta_O$ term with 20 dB/dec whereas a typical opamp GBP has –20 dB/dec characteristics. A large R2 and finite C1 can cause this Zero's frequency to be falling well below the crossover frequency. Hence the rate of closure becomes 40 dB/dec and the system has a 0° phase margin at the crossover frequency. The output may ring or oscillate if an input is a rectangular pulse or step function. Similarly, it is also likely to ring when the switching between two gain values, this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the Zero's frequency far enough to overcome the problem, a better approach is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2. As a result, one may use the relationship above and scale C2 as if R2 is at its maximum value. Doing so may overcompensate and compromise the performance when R2 is set at low values. On the other hand, it will avoid the ringing or oscillation at the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of few pF to no more than few tenths of pF is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown), their effect at this node is less significant and the compensation can be avoided in most cases.

High Voltage Operation

The Digital Potentiometer can be placed directly in the feedback or input path of an op amp for gain control, provided that the voltage across terminals A–B, W–A, or W–B does not exceed |5 V|. When high voltage gain is needed, users should set a fixed gain in an op amp operated at high voltage, and let the digital potentiometer control the adjustable input, Figure 14 shows a simple implementation. Similarly, a compensation capacitor C may be needed to dampen the potential ringing when the digital potentiometer changes steps. This effect is prominent when stray capacitance at the inverting node is augmented by large feedback resistor. In general, a few picofarad capacitor C is adequate to combat the problem.

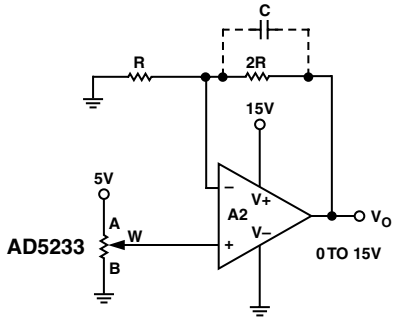


Figure 14. 15 V Voltage Span Control

Programmable Voltage Reference

For voltage divider mode operation, Figure 15, it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB}. Not only does the buffer serve the purpose of impedance conversion, but also allows heavier loads to be driven.

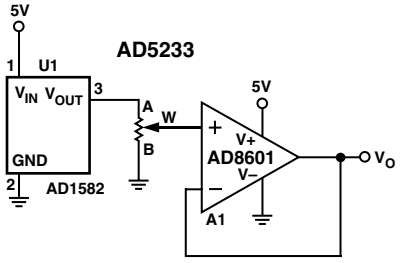


Figure 15. Programmable Voltage Reference

Bipolar Programmable Gain Amplifier

There are several ways to achieve bipolar gain, Figure 16 shows one versatile implementation. Digital potentiometer U1 sets the adjustment range; therefore the wiper voltage V_{W2} can be programmed between V_i and $-KV_i$ at a given U2 setting. Configuring A_2 as an noninverting amplifier yields a linear transfer function:

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D_2}{64} \times (1 + K) - K\right) \quad (4)$$

where K is the ratio of R_{WB}/R_{WA} which is set by *U1* and D = Decimal Equivalent of the Input Code.

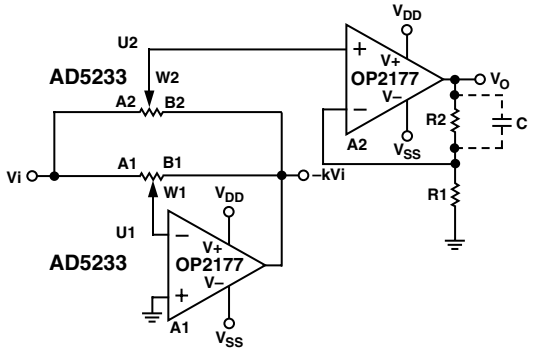


Figure 16. Bipolar Programmable Gain Amplifier

In the simpler (and much more usual) case, where K = 1, a pair of matched resistors can replace U1. Equation 4 simplifies to:

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{2D_2}{64} - 1\right) \quad (5)$$

Table XV shows the result of adjusting D, with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 64 step resolution.

Table XV. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9R1
0	–1	–2	–10
16	–0.5	–1	–5
32	0	0	0
48	0.5	1	5
63	0.968	1.937	9.680

Programmable Low-Pass Filter

Digital potentiometer AD5233 can be used to construct a second order Sallen Key Low-Pass Filter, Figure 17. The design equations are:

$$\frac{V_O}{V_i} = \frac{\omega_O^2}{S^2 + \frac{\omega_O}{Q}S + \omega_O^2} \quad (6)$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}} \quad (7)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (8)$$

where Q = Q factor, ω_O = resonant frequency, R1 and R2 = R_{WB1} and R_{WB2} respectively. To achieve maximally flat bandwidth where Q = 0.707, let C1 be twice the size of C2 and let R1 = R2. Users can first select some convenient values for the capacitors, then gang and move R1 and R2 together to adjust –3 dB corner frequency. Instructions #5, #7, #13, and #15 of the AD5233 make these change simple to implement.

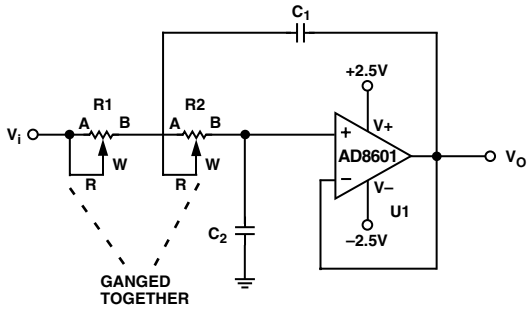


Figure 17. Sallen Key Low-Pass Filter

Programmable State-Variable Filter

One of the standard circuits used to generate a low-pass, high-pass, or bandpass filter is the state variable active filter. The digital potentiometer AD5233 allows full programmability of the frequency, gain, and the Q of the filter outputs. Figure 18 shows the filter circuit using a 2.5 V virtual ground, which allows a ±2.5 Vp input and output swing. RDAC2 and 3 set the LP, HP, and BP cutoff and center frequencies respectively. RDAC2 and RDAC3 should be programmed with the same data (as with ganged potentiometers) to maintain the best circuit Q.

The transfer function of the Bandpass Filter is:

$$\frac{V_{BP}}{V_i} = \frac{A_O \frac{\omega_O}{Q} S}{S^2 + \frac{\omega_O}{Q}S + \omega_O^2} \quad (9)$$

where A_O is the gain.

For $R_{WB2(D2)} = R_{WB3(D3)}$, R1 = R2, and C1 = C2:

$$\omega_O = \frac{1}{R_{WB2}C1} \quad (10)$$

$$A_O = -\frac{R_{WB1}}{R_{WA1}} \quad (11)$$

$$Q = \frac{R_{WA4}}{R_{WB4}} \times \frac{R_{WB1}}{R1} \quad (12)$$

Figure 19 shows the measured filter response at the bandpass output as a function of the RDAC2 and RDAC3 settings which produce a range of center frequencies from 2 kHz to 20 kHz. The filter gain response at the bandpass output is shown in Figure 20. At a center frequency of 2 kHz, the gain is adjusted over –20 dB to +20 dB range determined by RDAC1. Circuit Q is adjusted by RDAC4 and RDAC1. The suitable op amps for this application are OP4177, AD8604, OP279, and AD824.

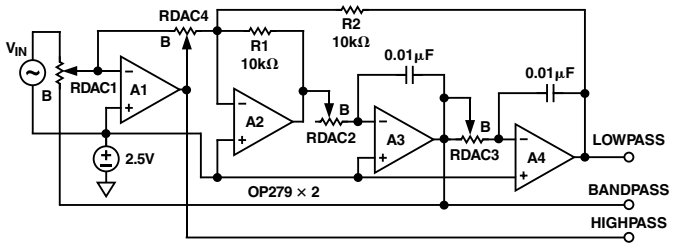


Figure 18. Programmable Stable Variable Filter

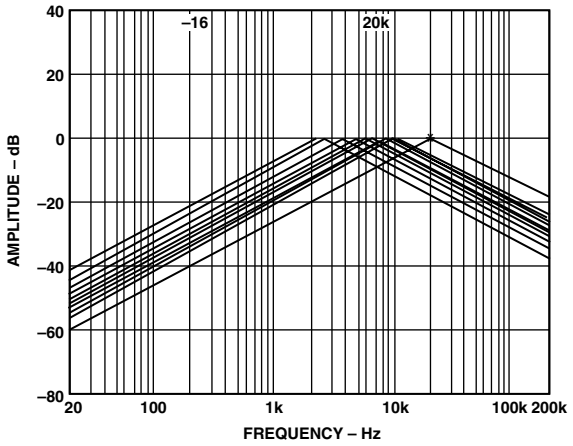


Figure 19. Programmed Center Frequency Bandpass Response

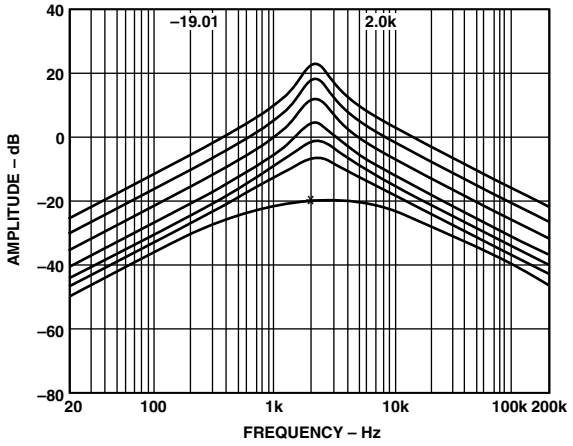


Figure 20. Programmed Amplitude Bandpass Response

Programmable Oscillator

In a classic Wien-bridge oscillator, Figure 21, the Wien network (R, R′, C, C′) provides positive feedback, while R1 and R2 provide negative feedback. At the resonant frequency, f_O, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. If the op amp is chosen with relatively high gain bandwidth product, the frequency response of the op amp can be neglected. With R = R′, C = C′, and R2 = R2A // (R2B + R_{DIODE}), the oscillation frequency is:

$$\omega_O = \frac{1}{RC} \text{ or } f_O = \frac{1}{2\pi RC} \quad (13)$$

where R is equal R_{WA} such that:

$$R = \frac{64 - D}{64} R_{AB} \quad (14)$$

At resonance, setting

$$\frac{R2}{R1} = 2 \quad (15)$$

balances the bridge. In practice, R2/R1 should be set slightly larger than 2 to ensure the oscillation can start. On the other hand, the alternate turn-on of the diodes D_1 and D_2 ensures R2/R1 to be smaller than 2 momentarily and therefore stabilizes the oscillation.

Once the frequency is set, the oscillation amplitude can be tuned by R2B since:

$$\frac{2}{3} V_O = I_D R2B + V_D \quad (16)$$

V_O, I_D, and V_D are interdependent variables. With proper selection of R2B, an equilibrium will be reached such that V_O converges. R2B can be in series with a discrete resistor to increase the amplitude but the total resistance cannot be too large to saturate the output. In this configuration, R2B can be adjusted from minimum to full scale with amplitude varied from ±0.6 V to ±0.9 V. Using 2.2 nF for C and C′, 10 kΩ dual digital potentiometer, with R and R′ set to 8 kΩ, 4 kΩ, and 700 Ω, oscillation occurs at 8.8 kHz, 17.6 kHz, and 100 kHz respectively, see Figure 22.

In both circuits in Figure 17 and 21, the frequency tuning requires that both RDACs to be adjusted to the same settings. Since the two channels may be adjusted one at a time, an intermediate state will occur that may not be acceptable for certain applications. Of course, the increment/decrement all instructions #5, #7, #13, #15 can be used. Different devices can also be used in daisy-chained mode so that parts can be programmed to the same setting simultaneously.

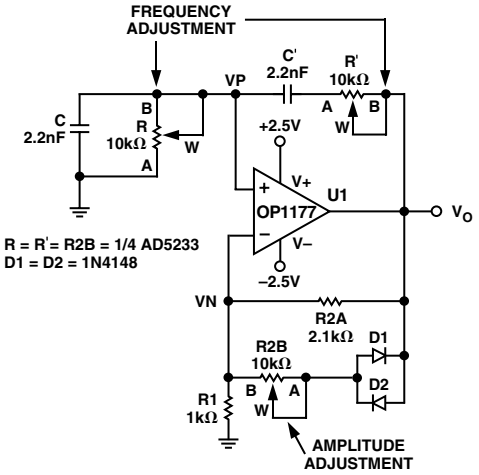


Figure 21. Programmable Oscillator with Amplitude Control

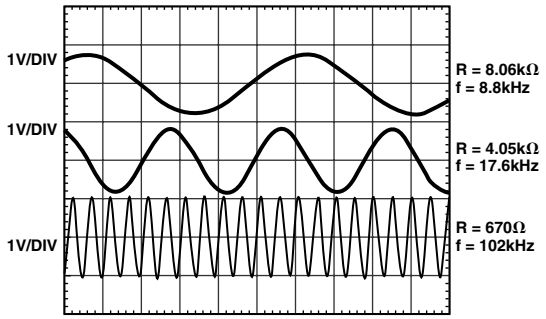


Figure 22. Programmable Oscillation

Programmable Voltage Source with Boosted Output
For applications require high current adjustment such as laser diode driver or turnable laser, a boosted voltage source can be considered, see Figure 23.

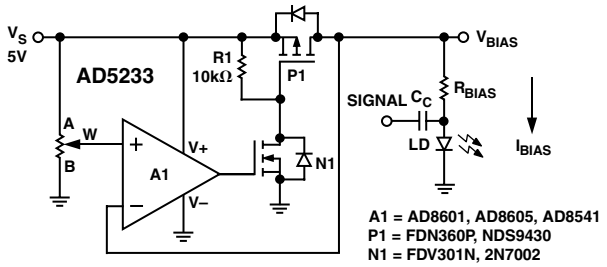


Figure 23. Programmable Booster Voltage Source

In this circuit, the inverting input of the opamp forces the V_{BIAS} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the P-Ch FET P1. The N-Ch FET N1 simplifies the opamp driving requirement. A1 needs to be rail-to-rail input type. Resistor R1 is needed to prevent P1 for not turning off once it is on. The choice of R1 is a balance between the power loss of this resistor and the output turn off time. N1 can be any general purpose signal FET; on the other-hand, P1 is driven in the saturation state and therefore its power handling must be adequate to dissipate $(V_S - V_{BIAS}) \times I_{BIAS}$ power. This circuit can source maximum of 100 mA at 5 V supply. Higher current can be achieved with P1 in larger package. Note that a single N-Ch FET can replace P1, N1, and R1 altogether. However, the output swing will be limited unless separate power supplies are used. For precision applications, a voltage reference such as ADR423, ADR292, and AD1584, can be applied at the input of the digital potentiometer.

Programmable 4 mA-to-20 mA Current Source
A programmable 4 mA-to-20 mA current source can be implemented with the circuit shown in Figure 24. REF191 is a unique low supply headroom precision reference that can deliver the 20 mA needed at 2.048 V. The load current is simply the voltage across terminals B-to-W of the digital pot divided by R_S.

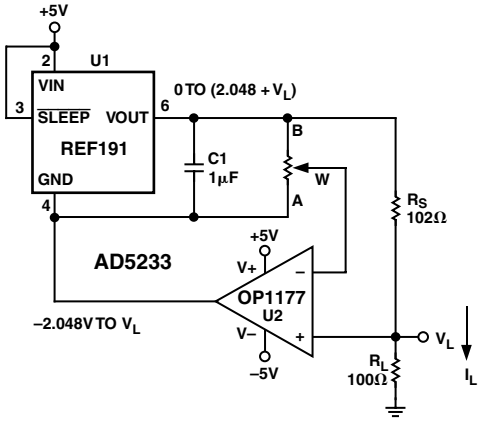


Figure 24. Programmable 4-to-20 mA Current Source

The circuit is simple, but beware two things. First, dual supply op amps are ideal because the ground potential of REF191 can swing from –2.048 V at zero-scale to V_L at full-scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of system will be reduced. Second, the voltage compliance at V_L is limited to 2.5 V or equivalently a 125 Ω load. Should higher voltage compliance be needed, users may consider digital potentiometers AD5260, AD5280, and AD7376. Figure 25 shows an alternate circuit for high voltage compliance.

Programmable Bidirectional Current Source
For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution, Figure 25. If the resistors are matched, the load current is

$$I_L = \frac{\left(\frac{R2A + R2B}{R1}\right)}{R2B} \times V_W \qquad (17)$$

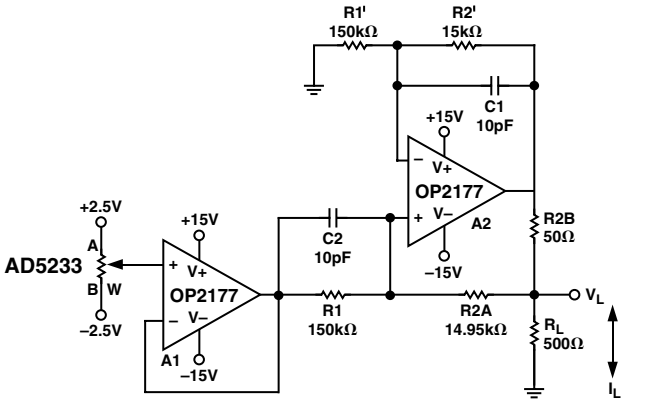


Figure 25. Programmable Bidirectional Current Source

R_{2B} in theory can be made as small as needed to achieve the current needed within A2 output current driving capability. In this circuit OP2177 delivers ±5 mA in both directions and the voltage compliance approaches 15 V. If there are no C1 and C2, if can be shown that the output impedance becomes

$$Z_O = \frac{R1'\,R2B\left(R1 + R2A\right)}{R1R2' - R1'\left(R2A + R2B\right)} \qquad (18)$$

Z_O can be infinite if resistors R1′ and R2′ match precisely with R1 and R2A + R2B respectively. On the other hand, Z_O can be negative if the resistors are not matched. As a result, C1 and C2, in the range of 1 F to 10 pF are needed to prevent the oscillation.

Resistance Scaling
AD5233 offers 10 kΩ, 50 kΩ, and 100 kΩ nominal resistance. For users who need lower resistance while maintaining the number of adjustment step, they can parallel multiple devices. For example, Figure 26 shows a simple scheme of paralleling two AD5233 channels. To adjust half of the resistance linearly per step, users need to program both devices coherently with the same settings.

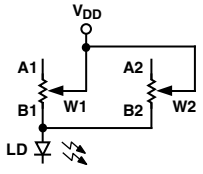


Figure 26. Reduce Resistance by Half with Linear Adjustment Characteristics

In voltage divider mode, a much lower resistance can be achieved by paralleling a discrete resistor as shown in Figure 27. The equivalent resistance become:

$$R_{WBeq} = \frac{D}{64}\left(R1 \| R2\right) + R_W \qquad (19)$$

$$R_{WA\,eq} = \left(1 - \frac{D}{64}\right)\left(R1 \| R2\right) + R_W \qquad (20)$$

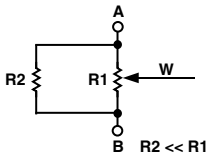


Figure 27. Lowering the Nominal Resistance

Figures 26 and 27 show that the digital potentiometer steps change linearly. On the other hand, log taper adjustment is usually preferred in applications like audio control. Figure 28 shows another way of resistance scaling. In this configuration, the smaller the R2 with respect to R1, the more the pseudo log taper characteristic behaves.

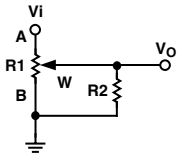


Figure 28. Resistor Scaling with Pseudo Log Adjustment Characteristics

Doubling The Resolution

Borrowing from ADI's patented RDAC segmentation technique, we can configure three channels of AD5233 as shown in Figure 29 by paralleling a discrete resistor R_p ($R_p = R_{AB}/64$) with RDAC3, we can double the resolution of AD5233 from 6-bit to 12-bit. We may think of moving RDAC1 and RDAC2 together forms the coarse 6-bit resolution, then moving RDAC3 forms the finer 6-bit resolution. As a result, the effective resolution becomes 12-bit. Nevertheless, the precision of this circuit remains only 6-bit accurate and the programming can be complicated.

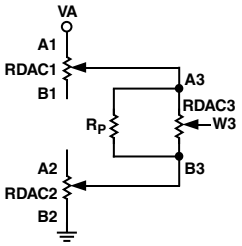


Figure 29. Doubling AD5233 from 6-Bit to 12-Bit

Resistance Tolerance, Drift, and Temperature Coefficient Mismatch Considerations

In the rheostate mode operation such as gain control, Figure 30, the tolerance mismatch between the digital potentiometer and the discrete resistor can cause repeatability issue among various systems. Because of the inherent matching of the silicon process, it is practical to apply the dual or multiple channel device in this type of applications. As such, R1 should be replaced by one of the channels of the digital potentiometer and programmed to a specific value. R2 can be used for the adjustable gain. Although it adds cost, this approach minimizes the tolerance and temperature coefficient mismatch between R1 and R2. In addition, this approach also tracks the resistance drift over time. As a result, all these non-ideal parameters become less sensitive to the system variations.

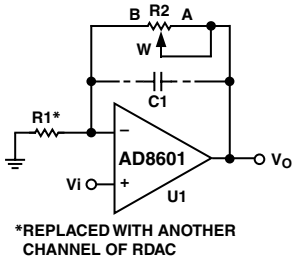


Figure 30. Linear Gain Control with Tracking Resistance Tolerance, and Temperature Coefficient

Notice the circuit in Figure 31 can also be used to track the tolerance, temperature coefficient, and drift in this particular application. The characteristic of the transfer function is however a pseudo-logarithmic, rather than a linear, gain function.

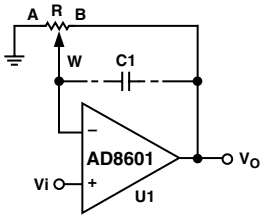


Figure 31. Nonlinear Gain Control with Tracking Resistance Tolerance and Drift

RDAC CIRCUIT SIMULATION MODEL

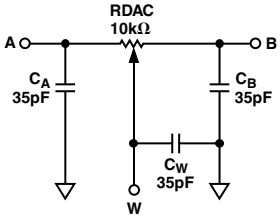


Figure 32. RDAC Circuit Simulation Model for RDAC = 10 kΩ

The internal parasitic capacitances and the external load dominate the ac characteristics of the RDACs. Configured as a potentiometer divider the –3 dB bandwidth of the AD5233 (10 kΩ resistor) measures 630 kHz at half scale. TPC 10 provides the large signal BODE plot characteristic. A parasitic simulation model is shown in Figure 32. Listing I provides a macro-model net list for the 10 kΩ RDAC:

Listing I. Macro-model Net List for RDAC

```
.PARAM D=64, RDAC=10E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A       0               35E-12
RAW     A       W          {(1-D/64)*RDAC+15}
CW      W       0                35-12
RBW     W       B            {D/64*RDAC+15}
CB      B       0               35E-12
*
.ENDS DPOT
```

DIGITAL POTENTIOMETER FAMILY SELECTION GUIDE*

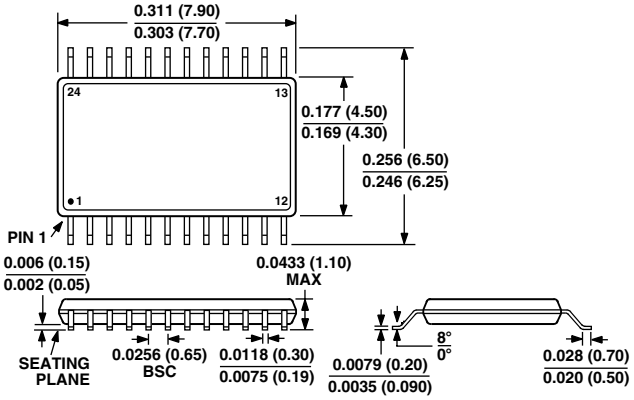
Part Number	Number of VRs per Package	Terminal Voltage Range (V)	Interface Data Control	Nominal Resistance (kΩ)	Resolution (No. of Wiper Positions)	Power Supply Current (I_{DD}) (μA)	Packages	Comments
AD5201	1	±3, +5.5	3-Wire	10, 50	33	40	μSOIC-10	Full ac Specs, Dual Supply, Pwr-On-Reset, Low Cost
AD5220	1	5.5	UP/DOWN	10, 50, 100	128	40	PDIP, SO-8, μSOIC-8	No Rollover, Pwr-On-Reset
AD7376	1	±15, +28	3-Wire	10, 50, 100, 1000	128	100	PDIP-14, SOL-16, TSSOP-14	Single 28 V or Dual ±15 V Supply Operation
AD5200	1	±3, +5.5	3-Wire	10, 50	256	40	μSOIC-10	Full ac Specs, Dual Supply, Pwr-On-Reset
AD8400	1	5.5	3-Wire	1, 10, 50, 100	256	5	SO-8	Full ac Specs
AD5260	1	±5, +15	3-Wire	20, 50, 200	256	60	TSSOP-14	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5241	1	±3, +5.5	2-Wire	10, 100, 1000	256	50	SO-14, TSSOP-14	I^2C Compatible, TC < 50 ppm/°C
AD5231	1	±2.75, +5.5	3-Wire	10, 50, 100	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5222	2	±3, +5.5	UP/DOWN	10, 50, 100, 1000	128	80	SO-14, TSSOP-14	No Rollover, Stereo, Pwr-On-Reset, TC < 50 ppm/°C
AD8402	2	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SO-14, TSSOP-14	Full ac Specs, nA Shutdown Current
AD5207	2	±3, +5.5	3-Wire	10, 50, 100	256	40	TSSOP-14	Full ac Specs, Dual Supply, Pwr-On-Reset, SDO
AD5232	2	±2.75, +5.5	3-Wire	10, 50, 100	256	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5235	2	±2.75, +5.5	3-Wire	25, 250	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, TC < 50 ppm/°C
AD5242	2	±3, +5.5	2-Wire	10, 100, 1000	256	50	SO-16, TSSOP-16	I^2C Compatible, TC < 50 ppm/°C
AD5262	2	±5, +15	3-Wire	20, 50, 200	256	60	TSSOP-16	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5203	4	5.5	3-Wire	10, 100	64	5	PDIP, SOL-24, TSSOP-24	Full ac Specs, nA Shutdown Current
AD5233	4	±2.75, +5.5	3-Wire	10, 50, 100	64	20	TSSOP-24	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5204	4	±3, +5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full ac Specs, Dual Supply, Pwr-On-Reset
AD8403	4	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SOL-24, TSSOP-24	Full ac Specs, nA Shutdown Current
AD5206	6	±3, +5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full ac Specs, Dual Supply, Pwr-On-Reset

*For the most current information on Digital Potentiometers, check the website at: www.analog.com/DigitalPotentiometers

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Thin Surface Mount TSSOP Package (RU-24)



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