ANALOG DEVICES

64-Position OTP I²C Compatible Digital Potentiometer

Preliminary Technical Data   AD5171

FEATURES

- **Set & Forget One Time Programmable Wiper Set**
- **64-Position**
- **End-to-End Resistance 5k, 10k, 50k, 100kΩ**
- **Compact SOT23-8 (2.9 x 3mm) Package**
- **I²C interface**
- **Full Read/write of wiper register**
- **Extra Package address decode pin A0**
- **Power ON Reset to Midscale**
- **I_{DD} ~ 0.01 μA**
- **Single Supply +2.7V to +5.5V**
- **Low Temperature Coefficient 35ppm/°C**
- **Wide Operating Temperature –40°C to +125°C**

Applications

- **Permanent Factory PCB Setting**
- **Resistor Adjustment & Final Set**
- **Replacement of Trimmers® in new designs**
- **Pressure, Temperature, Position, Chemical and Optical Sensor Calibration**
- **RF Amplifier biasing**
- **Automotive Electronics Adjustment**
- **Gain Control and Offset Adjustment**

GENERAL DESCRIPTION

The AD5171 provides a compact 2.9x3mm packaged solution for 64-position OTP adjustment applications. This device performs the same electronic adjustment function as a mechanical trimmer® or a variable resistor. Available in four different end-to-end resistance values (5k, 10k, 50k, 100kΩ) these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments.

These devices will provide variable resistance under 2-wire I²C compatible program control in servo adjustment factory applications. Once the final value is determined. The user programs a permanent write command freezing the wiper position at the desired setting (analogous to placing epoxy on a mechanical

trimmer). This one time program sets a validation bit, which can be read through the I²C interface. Once this acknowledge bit is set the wiper position can not be changed due to power supply sequencing, temperature, RF fields, ESD exposure, when maintained within its absolute maximum ratings. For applications that require continuous infrequent adjustment of wiper resistance settings, see the AD523x/AD525x families of nonvolatile memory digital potentiometers.

Operating from a 2.7 to 5.5 volt power supply consuming less than 1uA allows for usage in portable battery operated applications.

FUNCTIONAL DIAGRAM
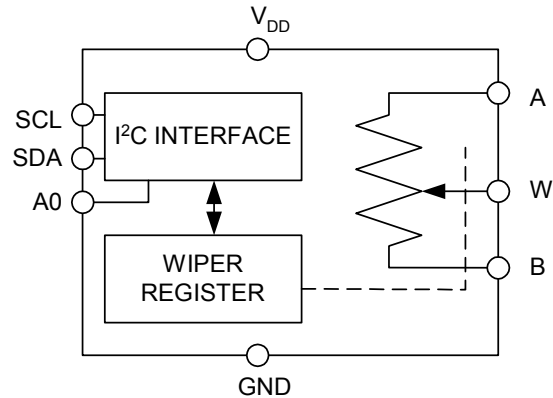
PIN CONFIGURATION
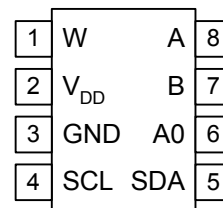
Notes:
1. The terms digital potentiometers, VR, and RDAC are used interchangeably.

64 Position Digital Potentiometer AD5171

AD5171 ELECTRICAL CHARACTERISTICS 5K, 10K, 50K, 100KΩ VERSION (V_{DD} = +5V $\pm$ 10%, or +3V $\pm$ 10%, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = No Connect	-1	±0.25	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = No Connect	-2	±0.5	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	-30		30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		35		ppm/°C
Wiper Resistance	R_W	V_{DD} = +5V		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N		8			Bits
Differential Nonlinearity[4]	DNL		−1	±1/4	+1	LSB
Integral Nonlinearity[4]	INL		−2	±1/2	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80$_H$		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF$_H$	−1.5	-0.5	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00$_H$	0	+0.5	+1.5	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 80$_H$		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 80$_H$		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5V		0.01	5	μA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD} / 2		1		nA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = +3V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = +3V			0.6	V
Input Current	I_{IL}	V_{IN} = 0V or +5V			±1	μA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_{LOGIC}		2.7		5.5	V
Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0V	-0.3		5.5	V
Supply Current	I_{DD}	V_{IH} = +5V or V_{IL} = 0V		5		μA
Power Dissipation[8]	P_{DISS}	V_{IH} = +5V or V_{IL} = 0V, V_{DD} = +5V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5V ±10%, Code = Midscale	-0.01	0.001	+0.01	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth –3dB	BW_10K	R_{AB} = 10KΩ, Code = 80$_H$		600		KHz
Bandwidth –3dB	BW_50K	R_{AB} = 50KΩ, Code = 80$_H$		100		KHz
Total Harmonic Distortion	THD$_W$	V_A = 1Vrms, V_B = 0V, f=1KHz, R_{AB} = 10KΩ		0.003		%
V_W Settling Time (10KΩ/50KΩ)	t_S	V_A = 5V, V_B = 0V, ±1 LSB error band		2/9		μs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5KΩ, RS = 0		9		nV√Hz

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Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 6,12)						
SCL Clock Frequency	f_{SCL}				400	KHz
t_{BUF} Bus free time between STOP & START	t1		1.3			µs
$t_{HD;STA}$ Hold Time (repeated START)	t2	After this period the first clock pulse is generated	0.6			µs
t_{LOW} Low Period of SCL Clock	t3		1.3			µs
t_{HIGH} High Period of SCL Clock	t4		0.6		50	µs
$t_{SU;STA}$ Setup Time For START Condition	t5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t7		100			ns
t_F Fall Time of both SDA & SCL signals	t8				300	ns
t_R Rise Time of both SDA & SCL signals	t9				300	ns
$t_{SU;STO}$ Setup time for STOP Condition	t10		0.6			µs

NOTES:

1. Typicals represent average readings at +25°C and V_{DD} = +5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
3. $V_{AB} = V_{DD}$, Wiper (V_W) = No connect
4. INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and V_B = 0V. DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions.
5. Resistor terminals A,B,W have no limitations on polarity with respect to each other.
6. Guaranteed by design and not subject to production test.
7. Measured at the A terminal. A terminal is open circuited in shutdown mode.
8. P_{DISS} is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation
9. All dynamic characteristics use V_{DD} = +5V.
10. See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F = 2ns$(10% to 90% of +3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using V_{LOGIC} = +5V.
11. The AD5171 contains xxxx transistors. Die Size: 30.7mil x 76.8 mil, 2358sq. mil.
12. See timing diagram for location of measured values.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5171 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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ABSOLUTE MAXIMUM RATINGS[1] (T_A = +25°C, unless otherwise noted)

V_{DD} to GND .... -0.3, +7V

V_A, V_B, V_W to GND .... V_{DD}

I_{MAX} ....±20mA[2]

Digital Inputs & Output Voltage to GND..............0V, +7V

Operating Temperature Range..............-40°C to +125°C

Maximum Junction Temperature ($T_{J\,MAX}$)..............+150°C

Storage Temperature.............................-65°C to +150°C

Lead Temperature (Soldering, 10 sec) ....+300°C

Thermal Resistance[3] $\theta_{JA,}$

　　　SOT23-8 .... 230°C/W

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance

3. Package Power Dissipation (T_{JMAX}-T_A)/ θ_{JA}

ORDERING GUIDE

Model#	R (Ω)	Package Description	Package Option	Brand
AD5171BRJ5	5K	SOT23-8	RJ-8	D12
AD5171BRJ10	10K	SOT23-8	RJ-8	D13
AD5171BRJ50	50K	SOT23-8	RJ-8	D14
AD5171BRJ100	100K	SOT23-8	RJ-8	D15

REV PrB, 20 FEB' 03

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Write Mode:

S	0	1	0	1	1	0	A0	W	A	X	RS	SD	X	X	X	X	X	A	DX	DX	D5	D4	D3	D2	D1	D0	A	P
			Slave Address Byte										Instruction Byte								Data Byte							

Read Mode:

S	0	1	0	1	1	0	A0	R	A	DX	DX	D5	D4	D3	D2	D1	D0	A	P
			Slave Address Byte									Data Byte							

S = Start Condition
P = Stop Condition
A = Acknowledge
X = Don't Care
W = Write
R = Read

RS = Reset wiper to Midscale 20_H
SD = Shutdown connects wiper to B terminal and open circuits A terminal. It does not change contents of wiper register.
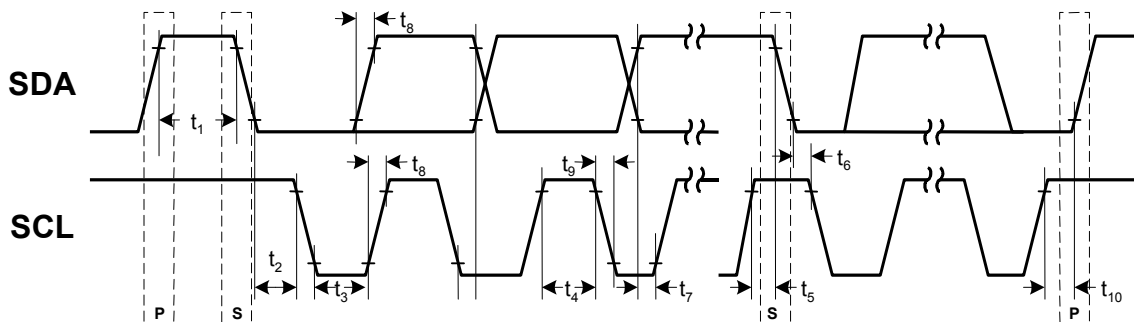**D5,D4,D3,D2,D1,D0** = Data Bits

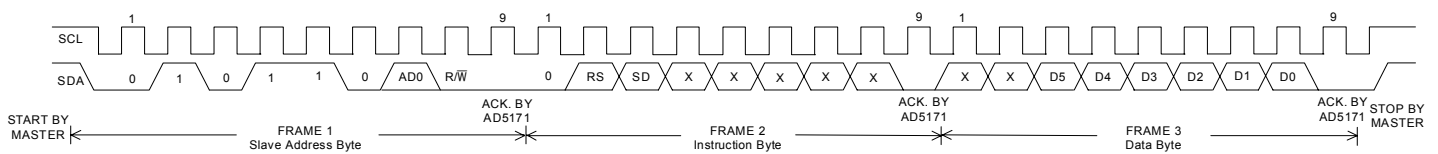*Figure 1. Detail Timing Diagram*
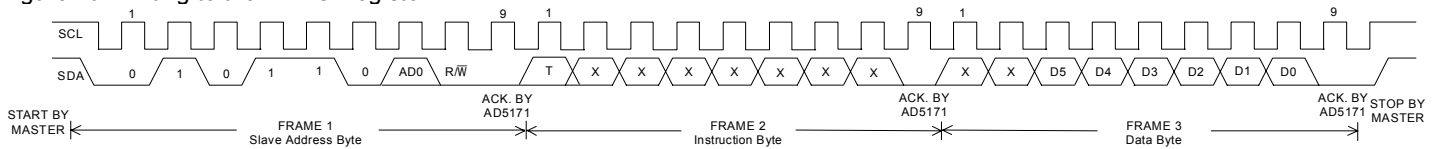

Figure 2a. Writing to the RDAC Register

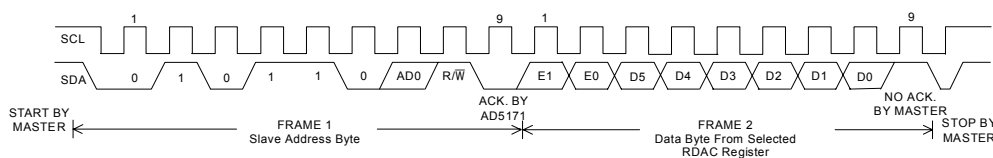*Figure 2b. Activating One Time Programming*

*Figure 3. Reading Data from a Previously Selected RDAC Register in Write Mode*

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TABLE 1: AD5171 PIN Descriptions

Pin	Name	Description
1	W	W Terminal
2	V_{DD}	Positive Power Supply
3	GND	Ground
4	SCL	Serial Clock Input, positive edge triggered
5	SDA	Serial Data Input/Output
6	A0	Programmable address bit 0 for multiple package decoding
7	B	B Terminal
8	A	A Terminal

PIN CONFIGURATION

1	W	A	8
2	V_{DD}	B	7
3	GND	A0	6
4	SCL	SDA	5
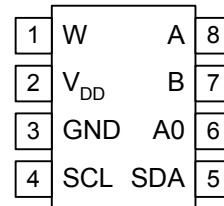
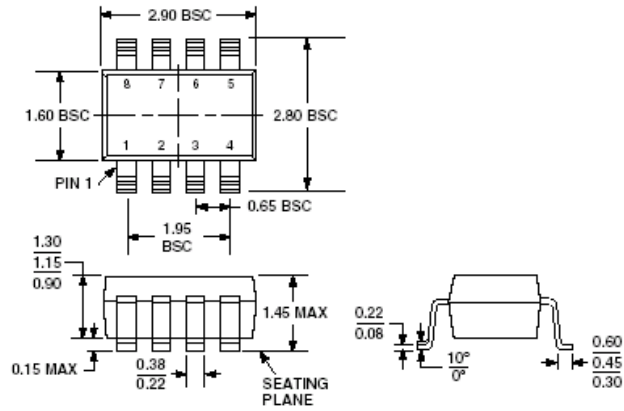# 64 Position Digital Potentiometer   AD5171

OUTLINE DIMENSIONS

8-Lead Plastic Surface-Mount Package [SOT-23]
RJ-8
Dimensions shown in millimeters

COMPLIANT TO JEDEC STANDARDS MO-178BA