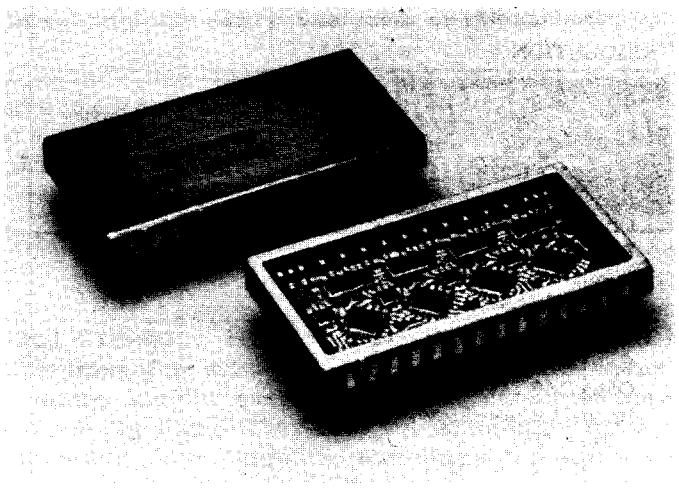
ANALOG DEVICES

μP Compatible Multiplying Quad 14-Bit D/A Converter

AD396

FEATURES
Four, Pre-Trimmed, 14-Bit CMOS DACs
Double Buffered for Simultaneous Update
Precision Output Amplifiers for Voltage Out
Full Four Quadrant Multiplication – Independently Pinned Out DAC Reference
Monotonicity Guaranteed Over Full MIL Temp. Range
Low Power – 780mW Max
Small 28 Lead, Hermetic Double DIP Package
MIL-STD-883 Processing Available



PRODUCT DESCRIPTION

The AD396 is a high-speed microprocessor compatible Quad 14-bit digital-to-analog converter. The AD396 contains four 14-bit, low power multiplying digital-to-analog converters followed by precision voltage output amplifiers all in a compact 28-pin hybrid package. The design is based on a proprietary latched 14-bit CMOS DAC chip which reduces chip count and provides high reliability.

The AD396 (K, T) is laser-trimmed to ±1LSB max differential and integral linearity, and to full-scale accuracy of ±0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DACs. Address lines A0, and A1, control internal register loading and transfer.

The AD396 outputs ($V_{REF} = +10V$) provide a ±10V bipolar output range with positive-true offset binary input coding.

The AD396 is packaged in a 28-lead double DIP package and is available for operation over the 0 to +70°C and −55°C to +125°C temperature range.

The AD396 is for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

PRODUCT HIGHLIGHTS

1. The AD396 offers a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full-scale accuracy of ±0.05%. Settling time to ±1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by the AD396.
6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DACs reference (V_{REFIN}).
9. The AD396S, T features guaranteed accuracy and linearity over the −55°C to +125°C temperature range.
10. MIL-STD-883 processing is available. See Analog Devices Military Data Sheet for further information.
11. Protection against power supply surges is included within the AD396.

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SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD396JD/SD[1] MIN	TYP	MAX	AD396KD/TD[1] MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	μA
RESOLUTION			14			14	Bits
OUTPUT							
Voltage Range[3]		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1	±2		±1/2	±1	LSB
Differential Linearity Error		±1/2	±1		±1/2	±1	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5]							
0 to +70°C		±1	±2		±1/2	±1	LSB
−55°C to +125°C		±2	±4		±1	±2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ±1/2LSB)							
V_{REFIN} = +10V, Change All Digital Inputs from +5.0V to 0V		10	15		10	15	μs
V_{REFIN} = 0 to 5V Step, All Digital Inputs = 0V		10	15		10	15	μs
Reference Feedthrough Error[6]		5			5		mV p-p
Digital-to-Analog Glitch Impulse[7]		250			250		nV sec
Crosstalk							
Digital Input (Static)[8]		1/2			1/2		LSB
Reference[9]		4.0			4.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	22		20	22	mA
$-V_S$		18	28		18	28	mA
Power Dissipation		570	780		570	780	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]AD396S and T grades are available to MIL-STD-883, Method 5008, Class B.
[2]Timing specifications appear in Table IV and Figure 3.
[3]Code tables and graphs appear on Theory of Operation page.
[4]FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range.
[5]Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.
[6]For AD396 (bipolar), DAC register loaded with 00 0000 0000 0000, V_{REFIN} = 20V p-p, 60 and 400Hz.
[7]This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.
[8]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.
[9]Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.
[10]The AD396 can be used with supply voltages as low as ±11.4V, Figure 7.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

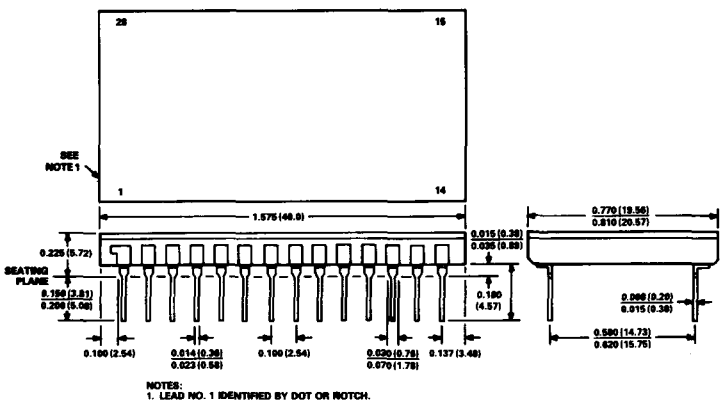
$+V_S$ to DGND	−0.3V to +17V
$-V_S$ to DGND	+0.3V to −17V
Digital Inputs (Pins 1-16) to DGND	−0.3V to +7V
V_{REFIN} to DGND	±25V
AGND to DGND	+0.3V to $+V_S$
Analog Outputs (Pins 18, 21, 24, 27)	Indefinite Short to AGND or DGND
	Momentary Short to $\pm V_S$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stess rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

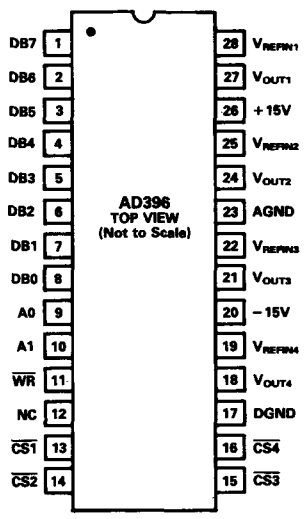


NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD396 with the inherent reliability of intergrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protect the chips from hazardous environments. To further insure reliabilty, the AD396S,T/883B are fully compliant to MIL-STD-883 Class B, Method 5008. See Analog Devices Military Data Sheet for further information.

PIN CONFIGURATION



PIN	FUNCTION	DESCRIPTION
1	DB7	DATA BIT 7
2	DB6	DATA BIT 6
3	DB5	DATA BIT 5/DATA BIT 13 (DAC MSB)
4	DB4	DATA BIT 5/DATA BIT 12
5	DB3	DATA BIT 3/DATA BIT 11
6	DB2	DATA BIT 2/DATA BIT 10
7	DB1	DATA BIT 1/DATA BIT 9
8	DB0	DATA BIT 0/DATA BIT 8
9	A0	ADDRESS LINE 0
10	A1	ADDRESS LINE 1
11	$\overline{WR}$	WRITE INPUT. ACTIVE LOW
12	NC	NO CONNECTION
13	$\overline{CS1}$	CHIP SELECT DAC 1. ACTIVE LOW
14	$\overline{CS2}$	CHIP SELECT DAC 2. ACTIVE LOW
15	$\overline{CS3}$	CHIP SELECT DAC 3. ACTIVE LOW
16	$\overline{CS4}$	CHIP SELECT DAC 4. ACTIVE LOW
17	DGND	DIGITAL GROUND
18	V_{OUT4}	DAC 4 VOLTAGE OUTPUT
19	V_{REFIN4}	DAC 4 REFERENCE INPUT
20	−15V	−15V SUPPLY INPUT
21	V_{OUT3}	DAC 3 VOLTAGE OUTPUT
22	V_{REFIN3}	DAC 3 REFERENCE INPUT
23	AGND	ANALOG GROUND
24	V_{OUT2}	DAC 2 VOLTAGE OUTPUT
25	V_{REFIN2}	DAC 2 REFERENCE INPUT
26	+15V	+15V SUPPLY INPUT
27	V_{OUT1}	DAC 1 VOLTAGE OUTPUT
28	V_{REFIN1}	DAC 1 REFERENCE INPUT

ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Price (100s)
AD396JD	0 to +70°C	±16LSB	±2LSB	$160
AD396KD	0 to +70°C	± 8LSB	±1LSB	$186
AD396SD	−55°C to +125°C	±16LSB	±2LSB	$384
AD396TD	−55°C to +125°C	± 8LSB	±1LSB	$451

Theory of Operation

The AD396 quad DAC provides four-quadrant multiplication. It is a hybrid comprised of four monolithic 14-bit CMOS multiplying DACs and eight precision output amplifiers. Each of the four independent-buffered channels has an independent reference input capable of accepting a separate dc or ac signal for multiplying or for function generation applications. The CMOS DACs act as digitally programmable attenuators when used with a varying input signal or, if used with a fixed dc reference, the DAC would act as a standard bipolar output DAC. In addition, each DAC has data latches to buffer the converter when connected to a microprocessor data bus.

MULTIPLYING MODE

Figure 1 shows the transfer function for the AD396. The diagram indicates an area over which many different combinations of the reference input and digital input can result in a particular analog output voltage. The highlighted transfer line in the diagram indicates the transfer function for a fixed reference at the input. The digital codes above the diagram indicates the mid and endpoints of the function. The relationship between the reference input (V_{REFIN}), the digital input code, and the analog output is given in Table I below. Note that the reference input signal sets the slope of the transfer function (and determines the full-scale output at code 111..111) while the digital input selects the horizontal position in each diagram.

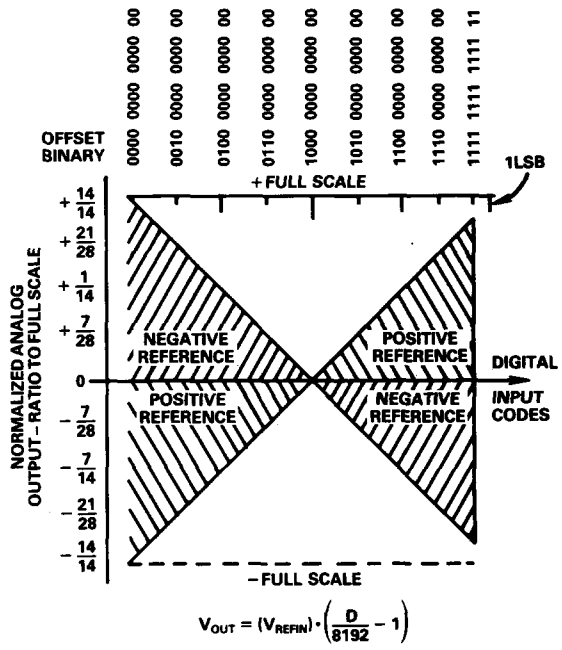


Figure 1. AD396 as a Four-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111 11	$+1 \cdot (V_{REFIN}) \left\{\frac{8191}{8192}\right\}$	+9.9988V	+FULL SCALE – 1LSB
1100	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{\frac{4096}{8192}\right\}$	+5.000V	+1/2 SCALE
1000	0000	0000 01	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{8192}\right\}$	+1.22V	+1LSB
1000	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{8192}\right\}$	+0.000V	ZERO
0111	1111	1111 11	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{8192}\right\}$	-1.22V	-1LSB
0100	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{\frac{4096}{8192}\right\}$	-5.000V	-1/2 SCALE
0000	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{\frac{8192}{8192}\right\}$	-10.000V	-FULL SCALE

Table I. AD396 Bipolar Code Table

DATA AND CONTROL SIGNAL FORMAT

The AD396 accepts 14-bit data by loading two separate input registers off an 8-bit data bus, and then loading the internal DAC register. The LS (least significant) register is loaded with the bottom 8-bits of the 14-bit word by selecting the appropriate address lines (see Table II). The MS (most significant) register is loaded with the top 6-bits in a similar manner. The $\overline{CS}$ and $\overline{WR}$ line must also be asserted to load the registers. The internal DAC register can then be loaded with the 14-bit data word. The appropriate DAC or DACs are selected by asserting $\overline{CS1}$-$\overline{CS4}$ (see Table III). If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincidentally, all four DAC outputs will be updated to the value located in the DAC register. When $A_1 = 0$ and $A_0 = 0$ all DAC registers are transparent so by placing all 0s or 1s on the data inputs the user can load the DACs to zero or full scale in one write operation. This provides simple system calibration.

$\overline{WR}$	$\overline{CS}$	A1	A0	Function
X	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

Table II. Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Register
1	0	1	1	Load DAC 2 From Data Register
1	1	0	1	Load DAC 3 From Data Register
1	1	1	0	Load DAC 4 From Data Register
0	0	0	0	All DACs Simultaneously Loaded

Table III. DAC Select Matrix

TIMING

The AD396 timing is shown in Figure 3, and has a few restrictions as stated in Table IV. $\overline{WR}$ must maintain a minimum pulse width of 240ns for desired operation to occur. When loading data in from the data bus, data must be stable for at least 80ns before returning $\overline{WR}$ to a high state. The Data must be held constant for at least 30ns after $\overline{WR}$ goes high to assure latching of valid data. DAC settling time is measured from the falling edge of the $\overline{WR}$ command.

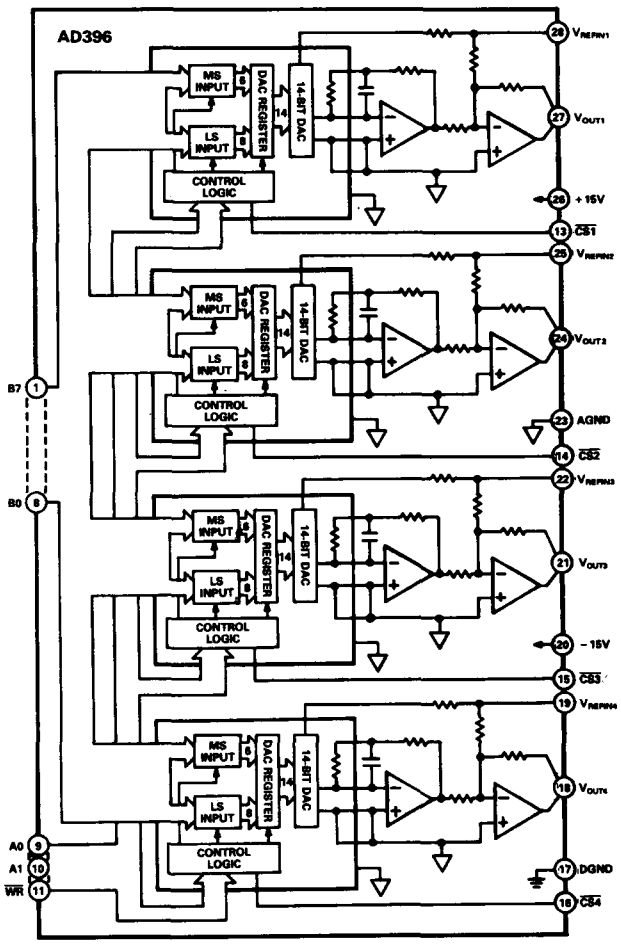


Figure 2. AD396 Block Diagram

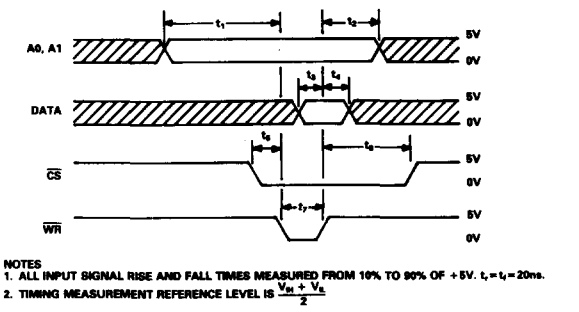


Figure 3. AD396 Timing Diagram

(V_{CC} = +15V, V_{EE} = −15V, V_{REF} = +10V)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C, T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	60	70	80	ns min	Data Setup Time
t_4	20	20	30	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select to Write Setup Time
t_6	0	0	0	ns min	Chip Select to Write Hold Time
t_7	170	200	240	ns min	Write Pulse Width

Table IV. Timing Characteristics

Analog Circuit Details

GROUNDING RULES

The AD396 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (Pin 17) and AGND (Pin 23). The DGND pin is the return for the supply currents of the AD396 and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the circuitry which drives the digital inputs.

Pin 23, AGND, is the high-quality analog ground connection. This pin should serve as the reference point for all analog circuitry associated with the AD396. It is recommended that any analog signal path carrying significant currents have its own return connection to Pin 23 as shown in Figure 4.

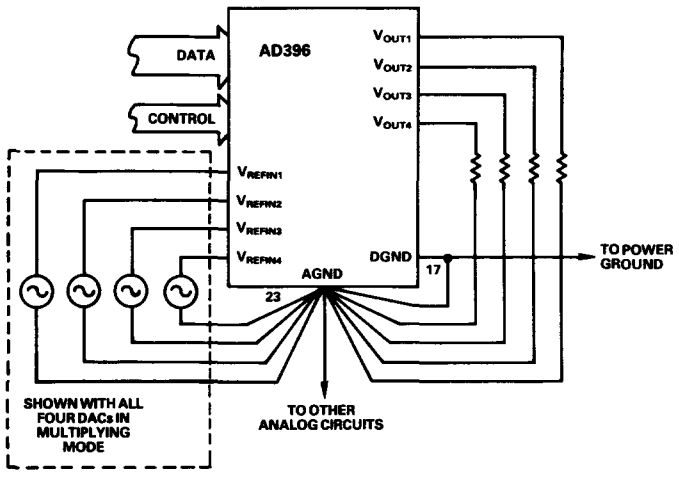


Figure 4. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the DAC outputs are accurately developed between the output pin and Pin 23 (AGND), delivering these signals to remote loads can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD396 packages are used. Figure 5 illustrates the parasitic impedances which influence output accuracy.

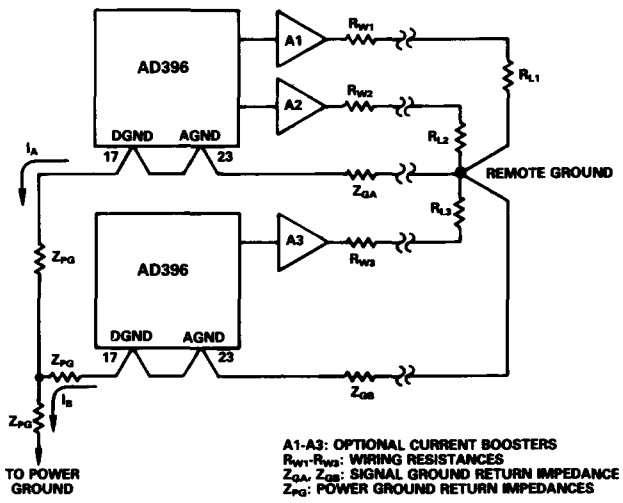


Figure 5. Grounding Errors in Multiple-AD396 Systems

An ouput buffer configured as a subtractor as shown in Figure 6 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote gound directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

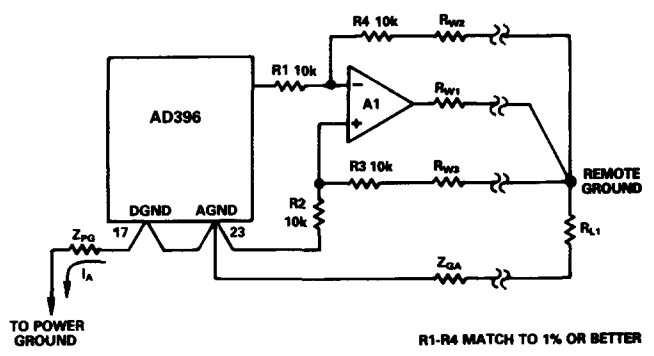


Figure 6. Use of Subtractor Amplifier to Preserve Accuracy

OPERATION FROM ±12V SUPPLIES

The AD396 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4 swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 1 millivolt per LSB).

Figure 7 shows a suggested circuit to set up a ±8.192V output range. To help prevent poor gain drift due to possible mismatch between R_{IN} and $R_{THEVENIN}$ of the divider network it is recommended to buffer the potentiometer wiper voltage with an OP-07.

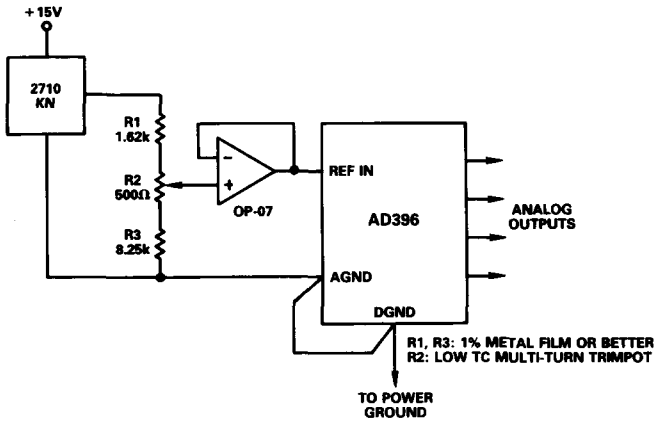


Figure 7. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

POWER SUPPLY DECOUPLING

The power supplies used with the AD396 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD396 supply pins and the AGND pin. If an output booster is used, its supplies should also be decoupled to the load ground.

IMPROVING FULL-SCALE STABILITY

In large systems using multiple DACs, it may be desirable for all devices to share a common reference. A precision reference can greatly improve system accuracy and temperature stability.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C. The combination of the AD2710LN and AD396 shown in Figure 8 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

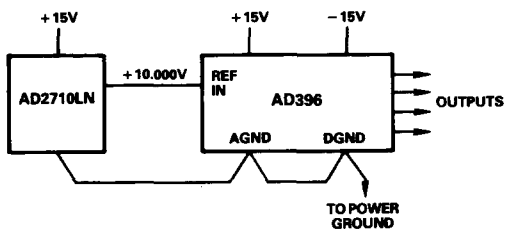


Figure 8. Low Drift AD396 Configuration

Applications

SPACE SAVINGS WITH THE AD396

The AD396 offers significant space savings for many users by offering four 14-bit DACs complete with latches and output amplifiers in one 28-pin double-width package. The AD396 was compared, for space saving, to another dual multiplying DAC the AD7537 which did not include output amplifiers. The AD396 was also compared to a competitor's 12-bit fixed reference DAC with input latches and output amplifiers contained within the package. In addition the AD396 is a 14-bit DAC opposed to the other two which are 12-bit DACs. A sample PC board layout was done for both the AD396 and two AD7537s with its support circuitry, as can be seen in Figures 9 and 10. The space saved by using the AD396 Quad Dac is at least three to one, and as much as four to one (see Table V). The AD396 is the clear winner in space savings over comparably functioning DACs, and has an extra two bits of resolution.

SPACE	AD396 QUAD	FOUR DACs	TWO AD7537s
DAC	25,000 mil	110,000 mil^2	30,000 mil^2
OP-AMPS			
RESISTORS	0	0	48,000 mil^2
TOTAL	25,000 mil^2	110,000 mil^2	78,000 mil^2

Table V. Space Comparison

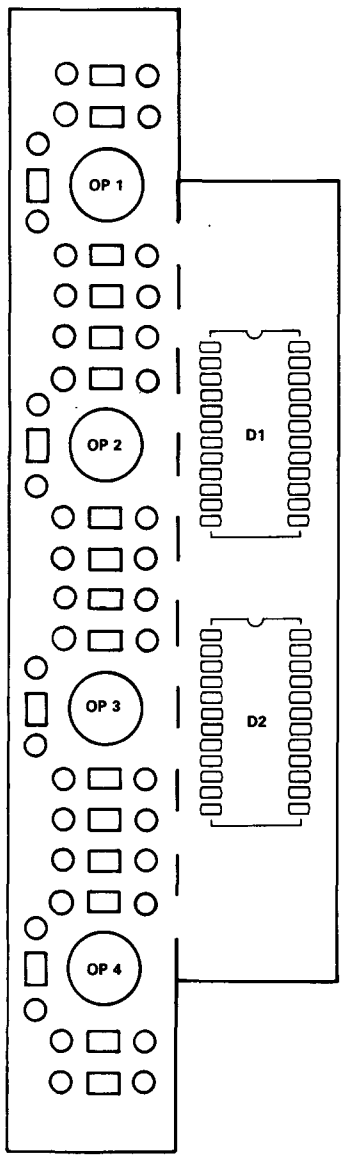


Figure 9. Bipolar Quad Multiplying DAC PC Board Layout

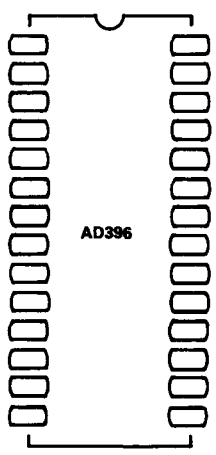


Figure 10. AD396 Quad DAC PC Board Layout

Applications

USING THE AD396 IN AUTOMATIC TEST EQUIPMENT

Most Automatic Test Equipment requires multiple accurate analog voltage thresholds which must be under microprocessor control. The AD396 is useful in such an application where space is at a premium and accuracy is essential.

The circuit in Figure 11 demonstrates how the AD396 is used to set up four different voltage thresholds (1 threshold per DAC).

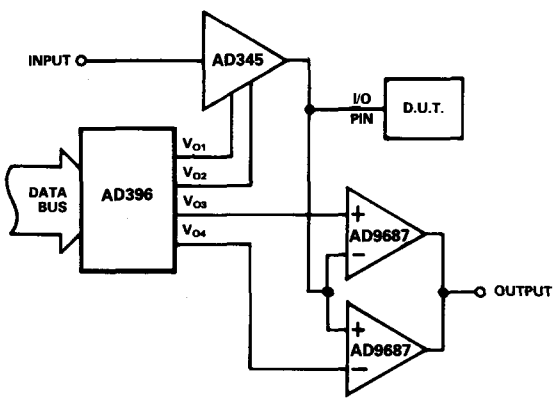


Figure 11. AD396 in ATE Systems

A fixed reference is used for the V_{REFIN} input of each of the multiplying DACs. The digital code corresponding to the desired voltage output is put on the bus, and the $\overline{\text{CHIP SELECT}}$ for the proper DAC is asserted. Two of the four DACs are used to set logic thresholds on the AD345 pindriver. The AD345 pindriver will then accurately test the logic thresholds on an I/O pin of the DUT (Device Under Test). The pindriver tests the pin by driving the pin to the proper logic thresholds set by the DACs.

The response from the I/O pin will then enter the AD9687 dual comparator. The other two DACs are used to set the voltage threshold for either a Logic HI (2.2V-5.0V) or a Logic LO (0V-0.8V). This is done by placing the upper voltage limit on the positive terminal of the higher comparator, and the lower voltage limit on the negative terminal of the lower comparator. The response can then be accurately tested if it is either a Logic HI or LO by looking if the output value of the pin falls within the designated window.

THE AD396 IN SYNCHRO-TO-DIGITAL CONVERTERS

The AD396 is useful in navigation systems where a Synchro-to-Digital Converter is needed. The Synchro-to-Digital Converter is used to measure angular position and is needed to measure pitch in the x-y-z axes and roll in the x-y-z axes. An S-D converter has three inputs and two converters are needed for this application. Each S-D converter uses two multiplying DACs and the accuracy of the S-D converter depends on the accuracy of the multiplying DAC.

The outputs of the transformer are Vsinwt(sinθ) and Vsinwt(cosθ). These two outputs are applied to the V_{REF} inputs of the DACs whose digital input words are proportional to the sine and cosine of angle θ as shown in Figure 12. The output of the cosine multiplier is given by Vsinwt(sinθ)(cosϕ), and the output of the the sine multiplier is given by Vsinwt(cosθ)(sinϕ).
These signals are subtracted by the error amplifier to give the error signal which is:

$$\text{Vsinwt}(\sin\theta\cos\phi - \cos\theta\sin\phi) = \text{Vsinwt}(\sin\theta - \phi)$$

This error signal is demodulated by the phase sensitive detector which utilizes the system reference voltage and a dc error signal proportional to sin(θ-ϕ) is produced. The dc error signal is fed back via an integrator and V.C.O. to drive the up-down counter until the error signal is nulled. The contents of the up-down counter give a binary representation of the angular position. For more information on synchro-to-digital conversion the reader is referred to Analog Devices Synchro & Resolver Conversion Handbook.

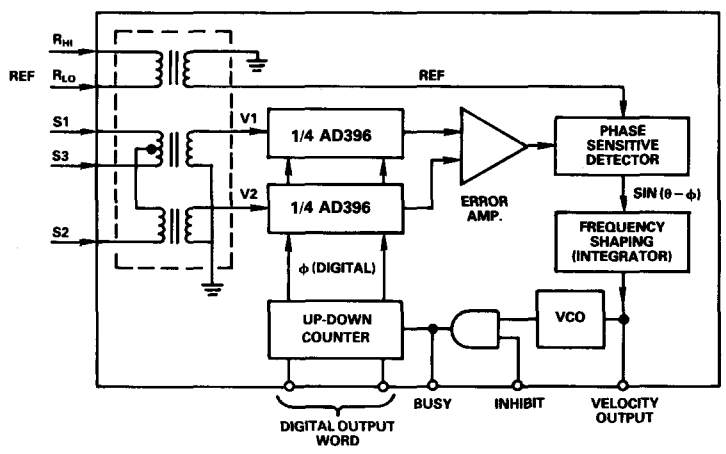


Figure 12. A Tracking Synchro-to-Digital Converter

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