ANALOG DEVICES

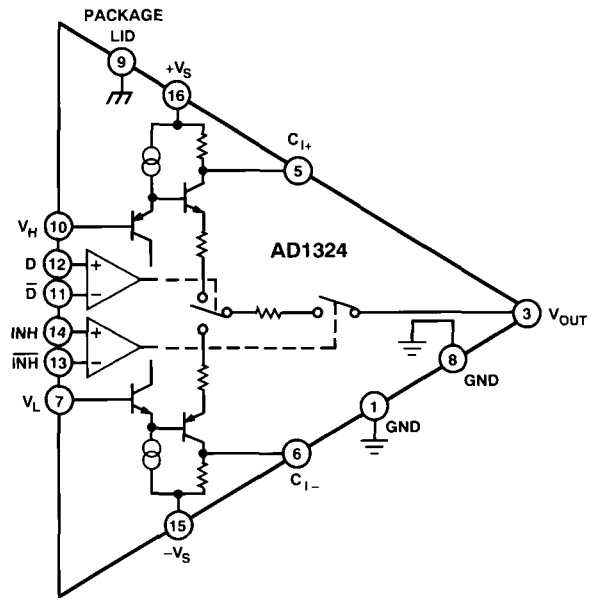
Ultrahigh Speed Pin Driver with Inhibit Mode

AD1324

FEATURES
200 MHz Driver Operation
Driver Inhibit Function
200 ps Edge Matching
Guaranteed Industry Specifications
50 Ω Output Impedance
2 V/ns Slew Rate
Variable Output Voltages for ECL, TTL and CMOS
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation & Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1324 is a complete high speed pin driver designed for use in digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long term reliability in an ultrasmall 16-lead, hermetically sealed gull wing package.

Featuring unity gain programmable output levels of −2 V to +7 V with output swing capability of less than 100 mV to 9 V, the AD1324 is designed to stimulate ECL, TTL and CMOS logic families. The 200 MHz (2.5 ns pulsewidth) data rate capacity, and matched output impedance allows for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (inhibit mode) electrically removing the driver from the path, through the inhibit mode feature. The pin driver leakage current in inhibit is typically 50 nA, and output charge transfer entering inhibit is typically less than 15 pC.

The AD1324 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry is implemented utilizing high speed differential inputs with a common-mode range of 3 volts. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 15 μA of bias current, the AD1324 can be directly coupled to the output of a digital-to-analog converter.

The AD1324 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0°C to +70°C.

AD1324—SPECIFICATIONS (All measurements made in free air at +25°C. Output load 10 kΩ/6 pF with $+V_S$ = +10 V, $-V_S$ = −5.2 V unless otherwise specified)

Parameter	AD1324KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Input Voltage, Any Input	−3.0		+5.5	Volts	
Differential Input Range	0.4	ECL	3.0	Volts	
Bias Current	−1350	+200	+500	μA	
REFERENCE INPUTS					See Note 1
V_{HIGH} Range (V_H)	−2.5		+7.5	Volts	
V_{LOW} Range (V_L)	−2.5		+7.5	Volts	
Bias Currents	−40	±15	40	μA	
Bias Current Change		2	10	μA	See Note 2
OUTPUT CHARACTERISTICS					See Notes 1, 3
Logic High Range	−1.6		+7.0	Volts	
Logic Low Range	−2.0		+6.6	Volts	
Amplitude [$V_H - V_L$]	0.4		+9.0	Volts	
Accuracy					
Initial Offset	−200		+200	mV	
Gain Error	−3.0	−1.0	0.0	% of V_{SET}	
Linearity Error					See Note 4
−1.0 V to +5.6 V	−(0.2% + 10)		(0.2% + 10)	% of V_{SET} + mV	V_L
−1.0 V to +6.0 V	−(0.2% + 10)		(0.2% + 10)	% of V_{SET} + mV	V_H
−2.0 V to −1.0 V	−(0.2% + 40)		(0.2% + 40)	% of V_{SET} + mV	V_L, V_H
+6.0 V to +7.0 V	−(0.2% + 40)		(0.2% + 40)	% of V_{SET} + mV	V_H
+5.6 V to +7.0 V	−(0.2% + 40)		(0.2% + 40)	% of V_{SET} + mV	V_L
Output Voltage Drift		0.5		mV/°C	
Current Drive					
Static	30			mA	
Dynamic	100			mA	See Note 5
Current Limit	35		85	mA	Output to GND
Output Resistance	48.5	50.0	51.5	Ω	See Note 6
Leakage Current in Inhibit Mode					
−1 V to +6 V	−1	±0.25	+1	μA	T_J = 95°C ± 5°C; See Note 7
−2 V to +7 V	−10		+10	μA	T_J = 95°C ± 5°C; See Note 7
DYNAMIC PERFORMANCE					See Note 8
Driver Mode					
Delay Time	0.9	1.2	1.5	ns	See Note 9
Prop Delay TC		1.0		ps/°C	
Delay Time Matching Edge-to-Edge	0	50	250	ps	
Rise & Fall Times					See Note 10
1 V Swing	0.4	0.6	0.8	ns	Measurement 20%–80%
2 V Swing	1.0	1.2	1.4	ns	Measurement 10%–90%
3 V Swing	1.4	1.7	2.0	ns	Measurement 10%–90%
5 V Swing	2.3	2.6	2.9	ns	Measurement 10%–90%
9 V Swing		5.5	6.5	ns	Measurement 10%–90%
Toggle Rate	200			MHz	ECL Output
Large Signal Slew Rate		1.5		V/ns	
Minimum Pulsewidth, V_{OUT} = 2 V		2.0		ns	See Figure 11
Overshoot & Preshoot					
1 V to 7 V	−(3% V_O) −50		+(3%V_O) +50	mV	% of V_{OUT} Swing; See Note 11
Settling Time					
1 V to 7 V, ±(1% × V_O)			15	ns	See Note 11
Delay Time vs. PW		100		ps	See Note 12
DYNAMIC PERFORMANCE					
Inhibit Mode Delay Time					See Note 13
Drive-to-Inhibit	1.0	1.3	1.6	ns	
Inhibit-to-Drive	1.4	1.9	2.4	ns	
Delay Time Matching					
Edge-to-Edge	0	100	400	ps	1 V Swing
Overshoot & Preshoot			300	mV	
Output Capacitance		3.5	5	pF	
Output Charge Going into Inhibit Mode		5		pC	

Parameter	AD1324KZ Min	Typ	Max	Units	Comments
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range		15.2	15.6	Volts	
Supply Range					See Note 14
Positive Supply	+8.0	+10.0	+11.0	Volts	
Negative Supply	−7.2	−5.2	−4.2	Volts	
Current					
Positive Supply	42	82	100	mA	
Negative Supply	−100	−82	−42	mA	
PSRR		5	20	mV/V	$+V_S$, $-V_S$ = ±2.5%

NOTES

[1]The output voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different values of V_{OUT} such as −1 V to +8 V or −4 V to +5 V as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

[2]V_H and V_L inputs have internal buffers which reduce the input bias current requirements. These buffers also reduce the amount of bias current change when the output switches logic levels.

[3]V_H must remain at least 400 mV more positive than V_L for specified performance. V_H may be as much as 5 V more negative than V_L, with degraded performance.

[4]Linearity testing is performed in 1 V increments over the following ranges:
V_L Linearity: V_H fixed at +7.0 V, V_L = −2.0 V to +6.6 V;
V_H Linearity: V_L fixed at −2.0 V, V_H = −1.6 V to +7.0 V.
Linearity error includes the error due to interaction for a minimum amplitude of 400 mV. Interaction error testing is performed with V_H = −0.6 V, V_L = −1.0 V and with V_H = +6.0 V, V_L = +5.6 V.

[5]Transient output current can easily exceed the AD1324's steady-state current limit when driving capacitive loads. The transient output current capability can be increased by connecting 0.039 μF capacitors between Pin 5 and $+V_S$ and between Pin 6 and $-V_S$. This will prevent the driver from current limiting by providing the "edge" current necessary when driving capacitive loads. These capacitors will not affect the driver's dc current limit.

[6]Driver output impedance is 50 Ω for a 3 V p–p signal into a 50 Ω load.

[7]While in inhibit mode, the output voltage must not go more than 6 V above V_{HIGH} or 6 V below V_{LOW}.

[8]The driver output has 2 ns length of 50 Ω coaxial cable attached with a 10 kΩ/6 pF probe, 1 GHz bandwidth or equivalent at the far end.

[9]Delay times are measured from the crossing of differential ECL levels at the input to the 50% point of an 800 mV driver output with V_H and V_L set at ±400 mV, respectively.

[10]Rise and fall time performance guaranteed over the output range of $+V_S$ −4 V to $-V_S$ +4.2 V except for 9 V swing, which is measured over the output range of $+V_S$ −3 V to $-V_S$ + 3.2 V.

[11]Due to uncontrolled inductances in the test socket, overshoot, preshoot and settling time cannot be 100% tested. These characteristics are guaranteed by characterization data .

[12]Delay matching vs. PW is defined as the amount of change in propagation delay, with respect to the leading edge, due to change in pulsewidth of the input signal. The specification applies over the pulsewidth range of 2.5 ns to 100 ns.

[13]Inhibit mode delay times are measured from the crossing of differential (ECL) INH inputs to a 200 mV crossing at the pin driver's output connected to 2 ns length of 50 Ω coaxial cable. The cable is terminated to ground through a 50 Ω resistor. The measurement is made at the 50 Ω resistor to GND with a 10 kΩ/6 pF scope probe.

[14]A supply range of 15.2 V must be maintained to guarantee a 9 V output swing.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- $+V_S$ to GND . . . . . +13 V
- $-V_S$ to GND . . . . . −8.2 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from D to $\overline{D}$ . . . . . 4.75 V
- Difference from INH to $\overline{INH}$ . . . . . 4.75 V
- D, $\overline{D}$, INH, $\overline{INH}$ . . . . . $+V_S$ − 13 V, $-V_S$ + 11.5 V
- V_H to V_L . . . . . −1 V, +9 V
- V_H, V_L . . . . . $+V_S$ − 13.2 V, $-V_S$ + 13.2 V

Driver Output
- Voltage . . . . . $+V_S$ − 13.2 V, $-V_S$ + 13.2 V
- Short Circuit to GND . . . . . Indefinite

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 20 sec)† . . . . . +300°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†To ensure lead coplanarity (±0.002 inches) and solderability handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

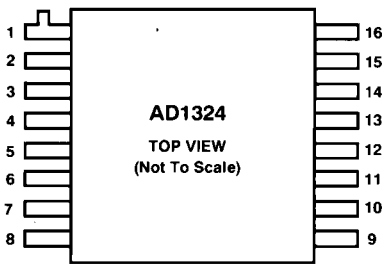
ORDERING GUIDE

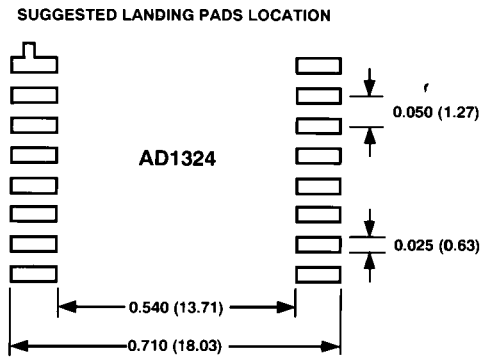
Model	Temperature Range	Description	Package Option*
AD1324KZ	0 to +70°C	16-Lead Gull Wing	Z-16A

*For outline information see Package Information section.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).





PIN DESCRIPTION

Pin No.	Symbol	Function
1	GND	Circuit Ground
2	N/C	No Connection
3	V_{OUT}	Driver Output
4	N/C	No Connection
5	C_{I+}	Positive Decouple
6	C_{I-}	Negative Decouple
7	V_L	Voltage Logic Low
8	GND	Internal Ground*
9	LID	Lid Connection*
10	V_H	Voltage Logic High
11	$\overline{D}$	Driver Input
12	D	Driver Input
13	$\overline{INH}$	Inhibit Input
14	INH	Inhibit Input
15	$-V_S$	Negative Supply
16	$+V_S$	Positive Supply

*It is recommended to connect Pins 8 and 9 to Circuit Ground.

OFFSET ERROR
The offset error for logic high is determined by holding the output of the driver at logic high, and applying zero volts to the logic high reference input. The driver output value represents the offset "high" error. The same approach is used to identify offset "low" error.

$$V_{HIGH\ OFFSET} = V_{OUT}$$

where:

V_H = 0 V
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

GAIN ERROR
Defined as the ratio of the driver's output voltage to its logic set level voltage and is expressed in terms of percent of set level. The gain error is typically seen as 1.0% and is always in the negative direction with respect to the logic set level.

$$V_{HIGH\ GAIN}\ (\%) = \frac{V_{OUT} - V_H - V_{HIGH\ OFFSET}}{V_H} \times 100$$

where:

V_H = 5.0 V + $V_{HIGH\ OFFSET}$
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

LINEARITY ERROR
The deviation of the transfer function from a reference line. For the AD1324, the linearity error is calculated by subtracting the worst case gain error from the best case gain error (for the specified range) and dividing the result by two. This method guarantees that the maximum linearity error for any set level within the specified range will be within the specified limits.

$$V_{HIGH\ LINEARITY}\ (\%) = \frac{V_{HIGH\ GAIN}\ (max) - V_{HIGH\ GAIN}\ (min)}{2} \times 100$$

DELAY TIME
The amount of time it takes the input signal to propagate through the driver and be converted to the desired logic levels. The measurement technique is defined in the notes and is shown in Figure 2.

EDGE-TO-EDGE MATCHING
Edge-to-edge matching is the difference, in time, between the delay time of the rising edge and the falling edge.

MINIMUM PULSEWIDTH
Defined as the smallest pulse applied to the input of the driver which can maintain an output signal amplitude of 2 V. The minimum pulsewidth is measured at the 50% point of the waveform.

OVERSHOOT AND PRESHOOT
The amount by which the driver's output voltage exceeds the desired set voltage. Preshoot is similar to overshoot but is the amount by which the driver's output goes above or below the initial voltage when driving to the new set level (or inhibit mode). See Figure 3.

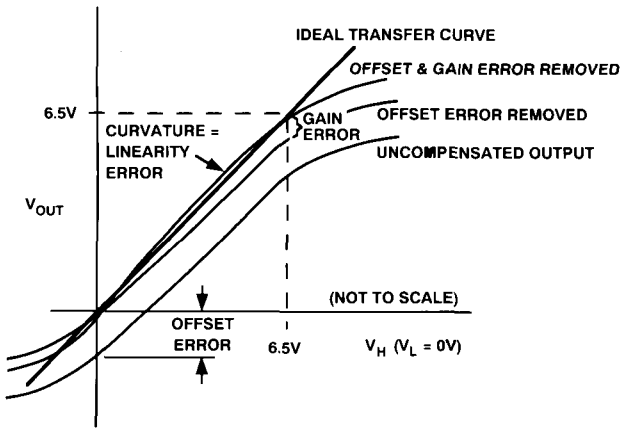


Figure 1. Definition of Terms

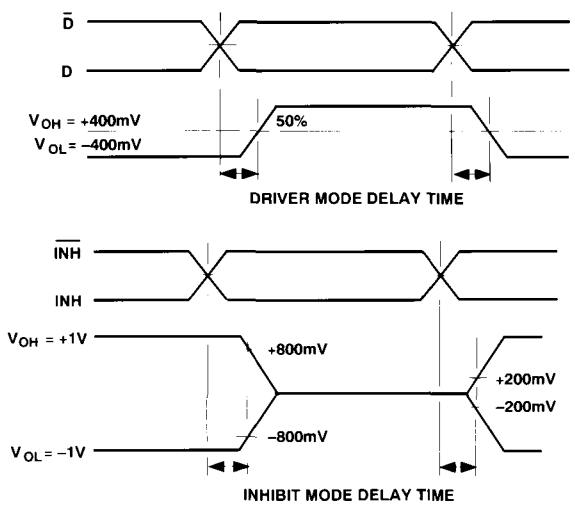


Figure 2. Timing Diagram for Driver and Inhibit Propagation Delay

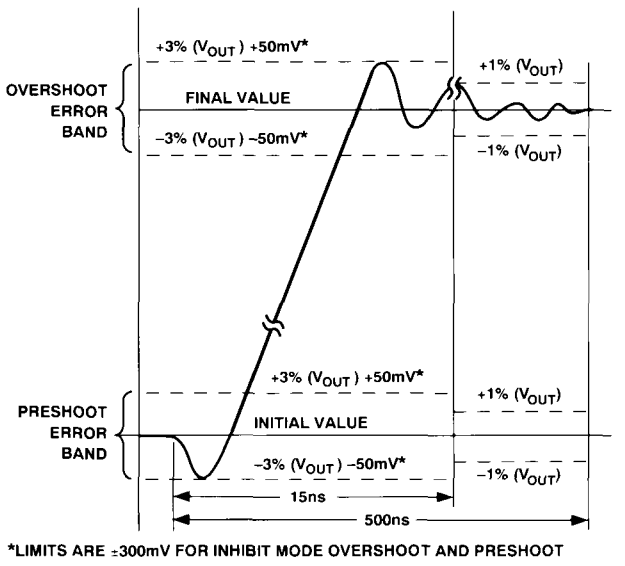


Figure 3. Definition of Waveform Aberrations

AD1324—Typical Performance

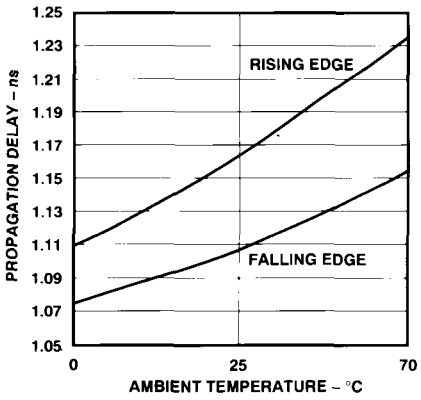


Figure 4. Driver Propagation Delay vs. Temperature

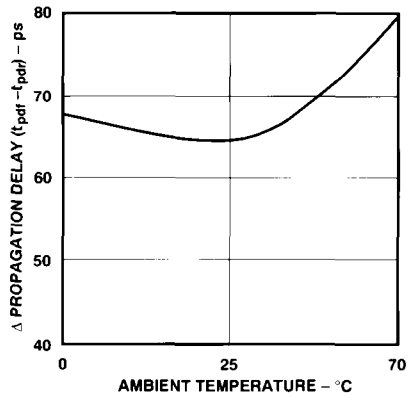


Figure 5. Propagation Delay Edge Matching vs. Temperature

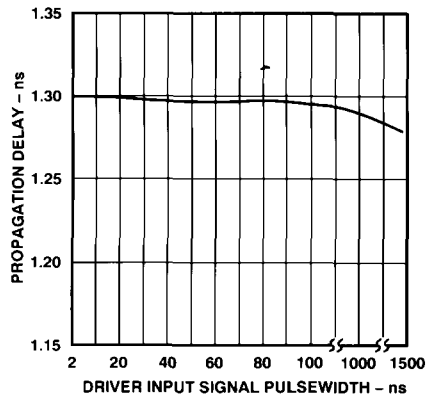


Figure 6. Propagation Delay vs. Input Signal Pulsewidth

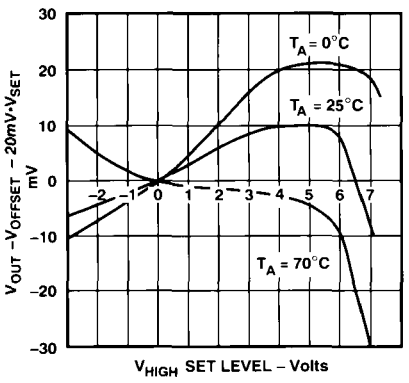


Figure 7. Change in V_{HIGH} over Temperature

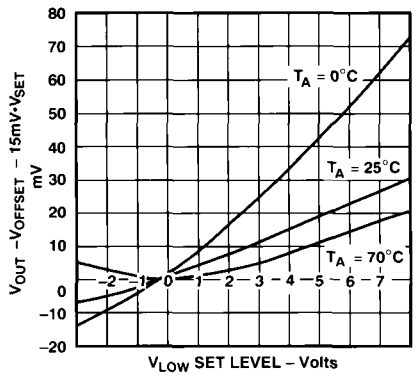


Figure 8. Change in V_{LOW} over Temperature

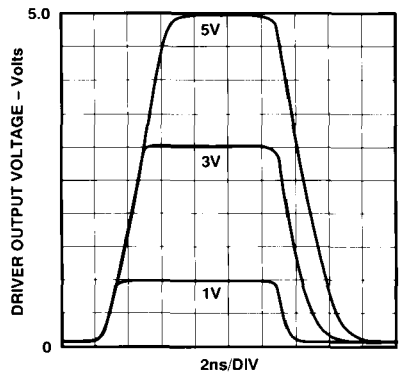


Figure 9. 10 ns Output Pulse at 1 V, 3 V and 5 V

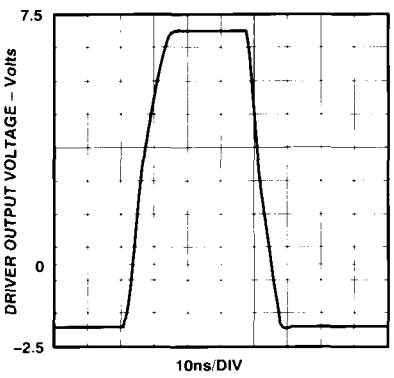


Figure 10. V_{OUT} = 9 V as Seen at the End of a 50 ns, 50 Ω Cable

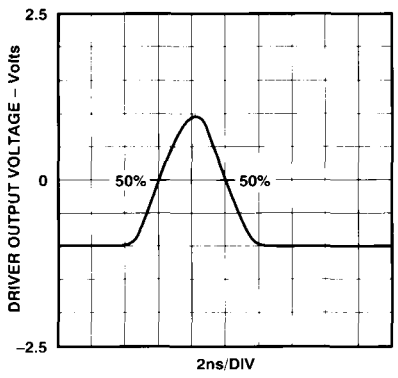


Figure 11. Minimum (Data) Pulsewidth as Defined by V_{OUT} = 2 V, 50% Crossing ≤ 2 ns

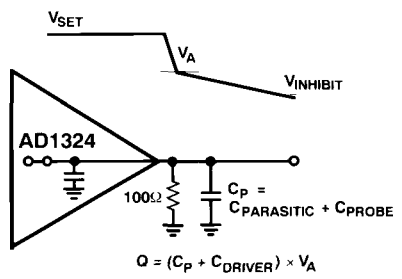


Figure 12. Charge into Inhibit Test Setup

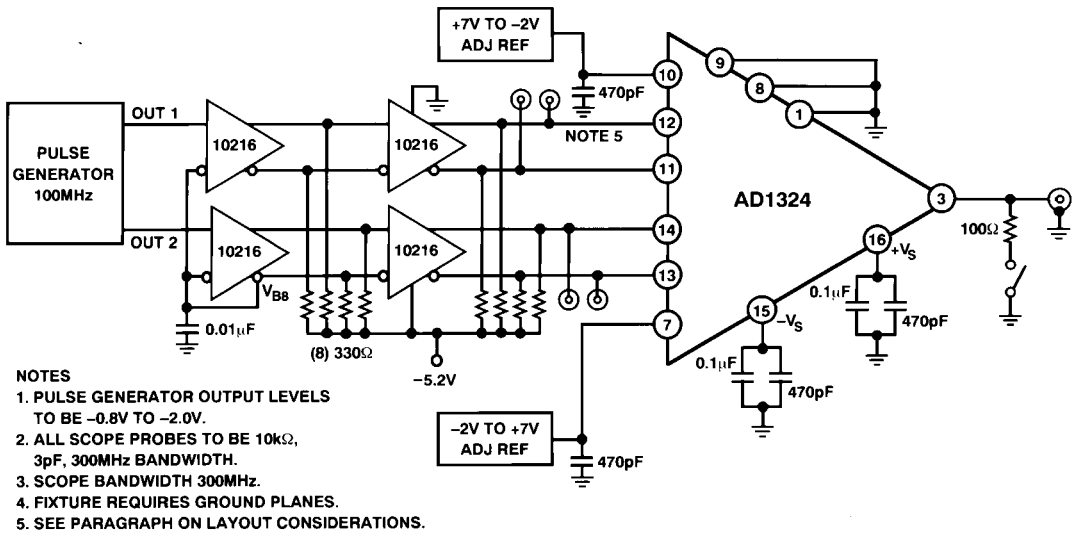


Figure 13. AD1324 Test Setup

FUNCTIONAL DESCRIPTION

The AD1324 is a complete high speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and combine these to drive the device to be tested.

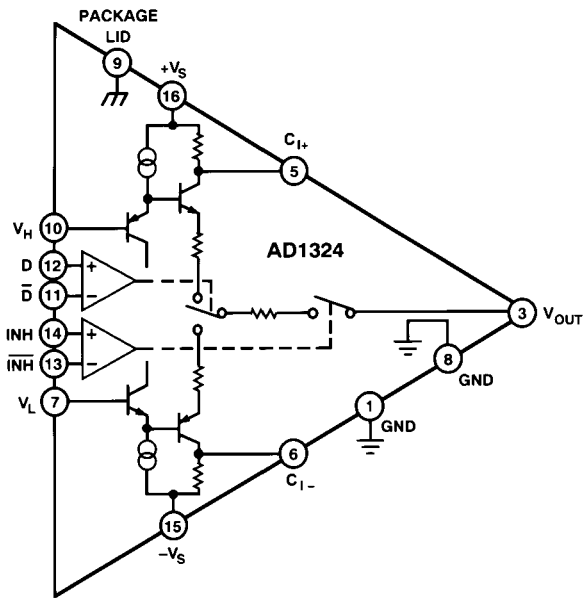


Figure 14. AD1324 Block Diagram

The circuit configuration for the AD1324 is outlined in Figure 14. Simply stated, a pin driver performs the function of a precise, high speed level translator with an output which can be disabled. The AD1324 accepts differential digital information utilizing a high speed differential design on the D and INH inputs providing precise timing at logic crossover and high noise immunity. The wide input voltage range allows for ECL operation with power supplies at 0 to −5.2 V, +2 V to −3.2 V or +5 V to 0 V. Where timing is less critical TTL or CMOS logic levels may be used to toggle the AD1324. By biasing the D and INH inputs to approximately +1.3 V for TTL and 1/2 V_{CC} for CMOS, the D and INH inputs can be directly driven from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the INH input is low. When inhibit is asserted the output is disconnected and any activity on the input does not affect the output.

Analog information is provided to the pin driver through the V_H and V_L terminals as reference voltages. These analog voltages are buffered internally using unity gain followers. The resulting gain and linearity errors are provided in the specification table. System timing requirements are achieved through a specified 1.2 ns, ±300 ps driver propagation delay, defined preshoot and overshoot, and a dynamically trimmed 50 Ω output impedance.

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple the power supplies of an active device, it is absolutely essential for a high power, high speed device such as the AD1324. The engineer merely has to consider the current pulse demand from the power supply when a dynamic current change of −100 mA to +100 mA is required in only a few nanoseconds. Therefore, a 470 pF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor should also be situated between the power supplies and ground. However, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 470 pF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 15.

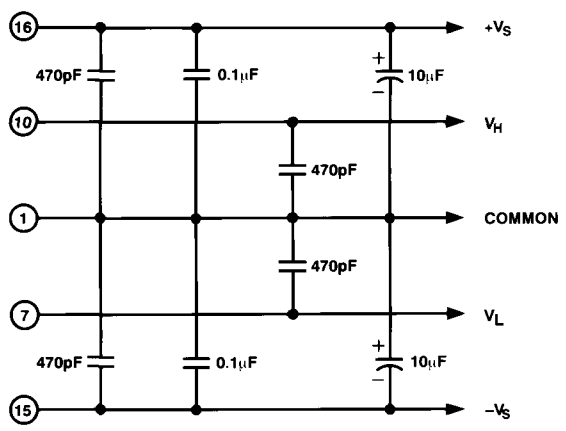


Figure 15. Basic Circuit Decoupling

An equally important consideration is the use of microwave stripline techniques on the output of the AD1324. Failure to preserve the 50 Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the wave shape. Care should be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

THERMAL CONSIDERATIONS

The AD1324 is provided in a 0.450″ × 0.450″, 16 lead (bottom brazed) gull wing, surface mount package with a typical junction-to-case thermal resistance of 17.5°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1324 in this package is shown in Figure 16. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1, 2].

NOTES
[1]lfm is air flow in Linear Feet/Minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

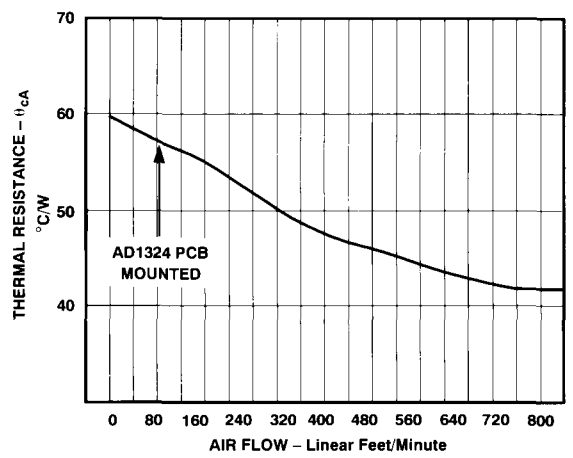


Figure 16. Case-to-Ambient Thermal Resistance vs. Air Flow

APPLICATIONS

The AD1324 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 18 is a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1324 pin driver, AD1317 high speed dual comparator, AD1315 active load, and the AD75069 octal 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 200 MHz in a data mode or 100 MHz in the I/O mode, yet fit into a neat trim package.

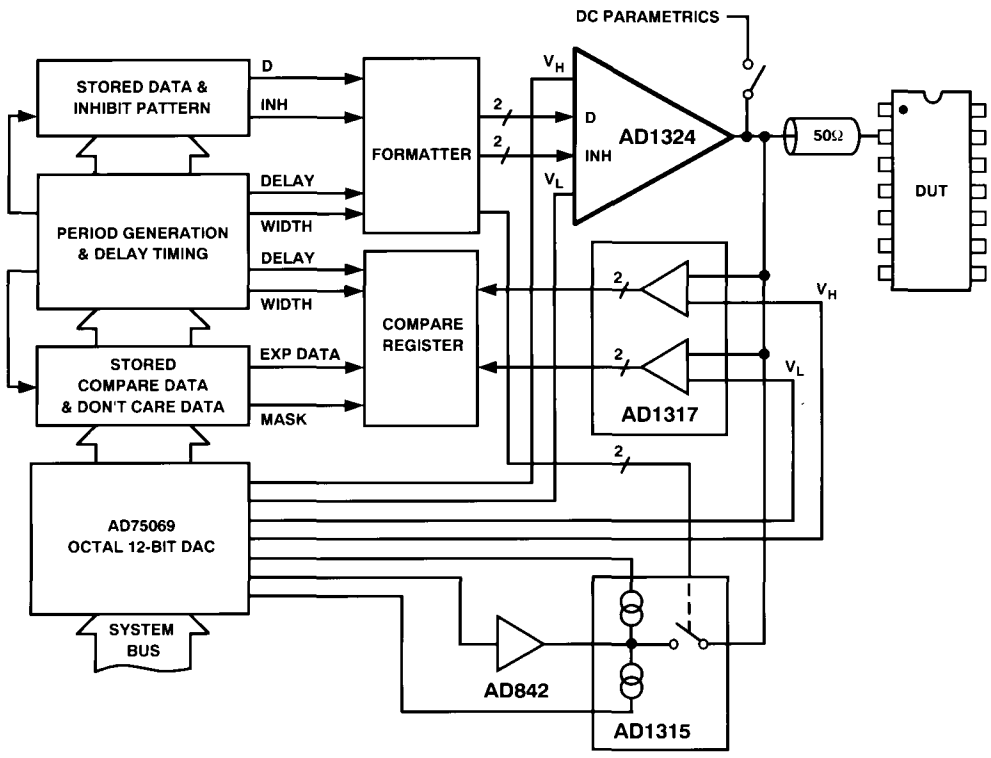


Figure 17. High Speed Digital Test System Block Diagram

AD1324 EVALUATION BOARD

Introduction

The AD1324EB evaluation board was developed to aid in quickly evaluating the performance of the AD1324. Included is complete documentation of the evaluation board along with suggestions on equipment to use and measurement limitations.

Overview

The AD1324 is a high speed pin driver used in automatic test equipment

The device has true differential inputs for both the drive and inhibit which can be driven from either TTL or ECL logic levels (ECL is recommended). Standard ECL design and layout techniques should be used.

The device runs from dual power supplies +10 V and −5.2 V. It is very important that these power supplies are decoupled properly at the device pin. (High frequency oscillations will couple through to the device output.)

The reference input pins are dc inputs; therefore they also should be decoupled properly. The reference input range is −2 V to +7 V.

The output slew rate is 2 V/ns for large signals and has a repetition rate for an ECL level of 200 MHz minimum.

Equipment

The Drive and Inhibit inputs should be driven with standard ECL levels. If the full performance of the AD1324 needs to be evaluated, the generator must be able to supply an ECL level at frequencies greater than 200 MHz. Motorola's MC10216 is used on the evaluation board to simulate the actual application. V_{BB} is used on the MC10216 as the logic reference and the outputs have 330 ohm pulldowns to V_{EE}.

Five power supplies are required: DUT_V_{CC}, DUT_V_{EE}, V_{HIGH}, V_{LOW} and ECL_V_{EE}. DUT_V_{CC} requires +10 V at 100 mA minimum; DUT_V_{EE} requires −5.2 V at 100 mA minimum; ECL_V_{EE} requires −5.2 V at 150 mA minimum. V_{HIGH} and V_{LOW} require −2 V to +7 V at 5 mA (each).

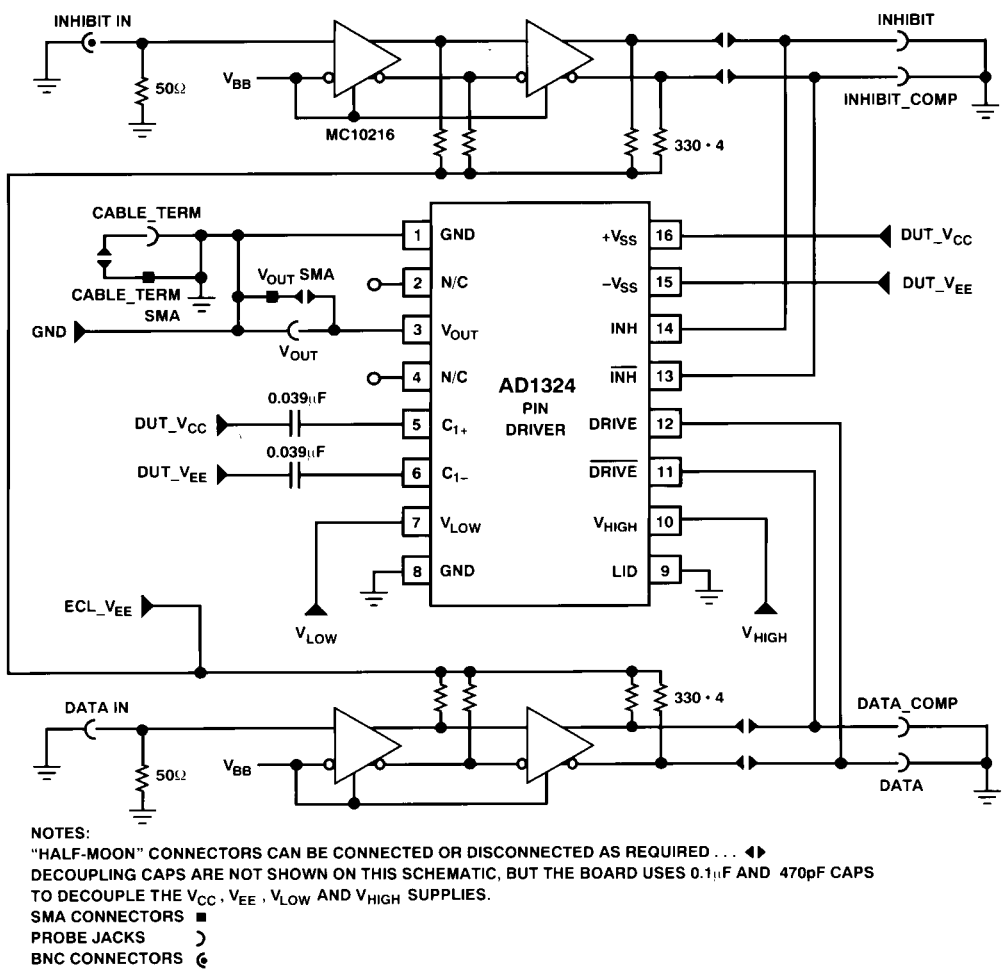


Figure 18. AD1324EB Evaluation Board Schematic

The output performance of the pin driver can only be measured properly with a scope which has the proper bandwidth for the required application. The input impedance and the bandwidth of the scope probe should be taken into consideration when evaluating the performance of the device. The resultant bandwidth of the system is the rms value of the components in the system.

The characterizations performed by Analog Devices were performed using the following equipment: Tektronix 11402 mainframe (1 GHz BW), P6203 probe (1 GHz, 2 pF, 10 kΩ), and 11A71 plug-in (1 GHz BW, 50 Ω).

The Hewlett-Packard 54120 and 54110 were also evaluated with 500 Ω, 1.2 pF passive probes and the Data Precision 6100 with their model 640 FET probe (50 kΩ, 4 pF). When measuring the performance of waveforms close to or exceeding the bandwidth of a scope, it is not uncommon for the results between scopes to be different because of aberrations and slew rates.

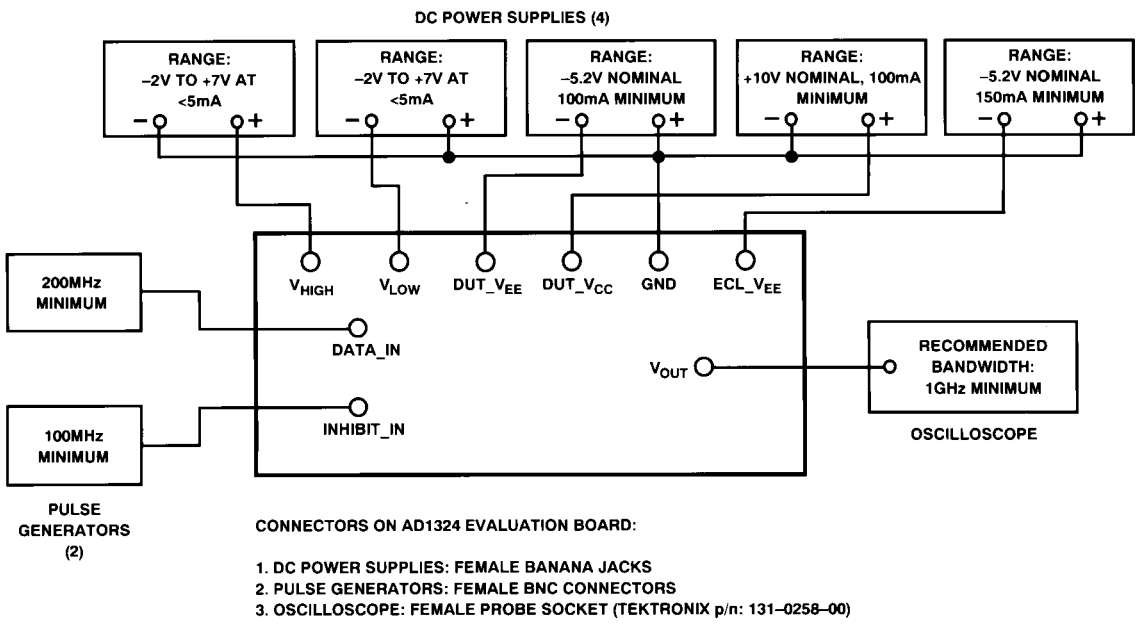


Figure 19. AD1324EB Evaluation Board Connections