

ADVANCED CUSTOMIZED ECL (ACE)

ACE600 & ACE900

MASTER SLICE LOGIC ARRAYS

FEATURES

- 3-micron geometry (first metal)
- Internal gate delays as low as 300 picoseconds (average gate delay of 450 picoseconds)
- Expandable 80-cell MACRO library
- Mask-selectable rise/fall times for I/O interface cells
- Bidirectional and TTL interfaces
- 10K/100K ECL compatibility
- Computer aided design (CAD) for layout, simulation, and testing
- Mature process (SUBILO P)
- Pin grid array packages for easy socket insertion
- 25 and 50 ohm drive capability

PRODUCT DESCRIPTION

The Signetics Advanced Customized ECL (ACE) family of products provides the user with a cost-effective technology, futuristic speeds, and other high-performance alternatives for the design of LSI-based systems. Basic cell designs are implemented with Emitter Coupled and Common Mode Logic (ECL/CML) to guarantee the very best compromise between speed, power, and interface capabilities—see Figure 1 and TECHNICAL SUMMARY that follows.

At present, the ACE product line is available with gate complements of 600, 900, 1320, 1400, and 2200; the 1320 array

actually contains 1000 gates with an on-board 320-bit RAM. The 600/900-gate arrays, described in this data sheet, are well-suited for low-cost applications and for use in systems that do not require 25-ohm terminations. To meet the flexibility requirements, the rise-and-fall times for I/O cells of these arrays are mask-selectable and bidirectional and TTL interfaces are standard.

All ACE arrays are I/O compatible with the 10K/100K ECL logic family and all are fabricated with a very mature process; thus, even with 3-micron first-metal geometry, first pass success is a virtual certainty. The speed-power product for devices in the ACE family is in the neighborhood of 1 to 3 picojoules, permitting heat-sink cooling at ambient air temperatures. The ACE family and MACRO library is alternately sourced by a major supplier of semicustom devices.

To summarize, the designer, using ACE, is limited only by innovation and imagination:

- ECL/CML Technology for SPEED and EFFICIENCY
- Mature process for PRODUCT CERTAINTY
- Computer aided design for QUICK DELIVERY
- Pin grid packages (socket insertion) for RELIABILITY
- Signetics for QUALITY

ORDERING INFORMATION

Contact Local Sales Representative

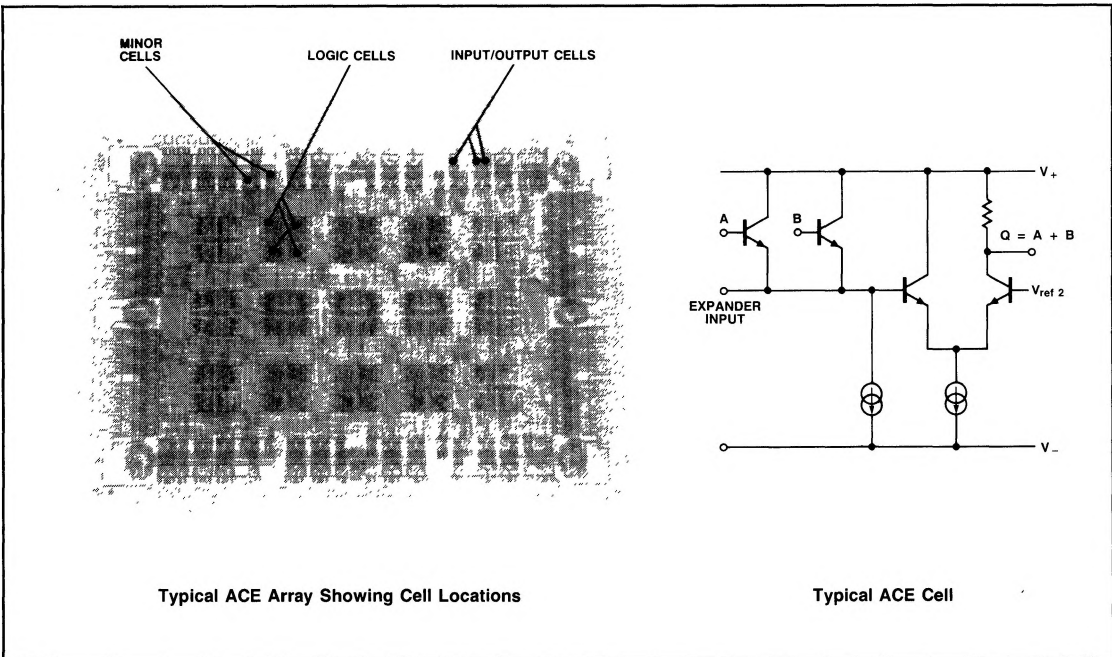


Figure 1. Chip Architecture and Typical Circuit

ADVANCED CUSTOMIZED ECL (ACE)**ACE600 & ACE900****MASTER SLICE LOGIC ARRAYS****TECHNICAL SUMMARY OF ACE FAMILY**

PARAMETER	ACE 600	ACE 900	ACE 1320	ACE 1400	ACE 2200
Major cells	24	36	48	60	100
Input/output cells	28	28	96	96	128
Input cells	30	42	—	—	—
Worst case noise margin	24 - 45 mV		24 - 45 mV		
Junction temperature range	30 - 125°C		30 - 125°C		
Average prop delay (internal gate)	0.3 - 0.5 ns		0.3 - 0.5 ns		
	10K LEVEL	100K LEVEL	10K LEVEL	100K LEVEL	
Power supply	-5.25V ± 5%	-4.5V ± 5%	-5.25V ± 5%	-4.5V ± 5%	
Power consumption	2.1 - 2.7 mW	1.8 - 2.3 mW	4.6 - 6.3 mW	4 - 5.5 mW	
ACE PACKAGE TYPE AND THERMAL RESISTIVITY SELECTION					
	PACKAGE	THERMAL RESISTIVITY (°C/W)			
		HEAT SINK	NO AIR FLOW	5 m/s AIR FLOW	
ACE 600 & ACE 900	64 Pin	Yes	25	13	
		No	50	25	
ACE 1320, ACE 1400 & ACE 2200	144 Pin	Yes	12	6	
		No	24	12	