96LS32

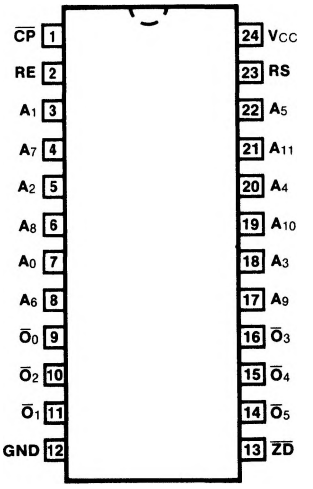
ADDRESS MULTIPLEXER/REFRESH COUNTER

(For 4K Dynamic RAMs)

DESCRIPTION — The 96LS32 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to six input addresses (or 4K bits for 64 x 64 organization). It multiplexes 12 bits of system applied address to six output address pins. The device also contains a 6-bit refresh counter which is externally clocked so that either distributed or burst refresh may be used. The high performance of the 96LS32 makes it especially suitable for use with high speed n-channel RAMs like the M4027. The 96LS32 operates from a single +5.0 V power supply and is specified for operation over a 0°C to +75°C ambient temperature range.

- **SIMPLIFIES SYSTEM DESIGN**
- **REDUCES PACKAGE COUNT**
- **DRIVES HIGH CAPACITANCE LOADS**
- **USE FOR DISTRIBUTED OR BURST REFRESH**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

CONNECTION DIAGRAM
PINOUT A



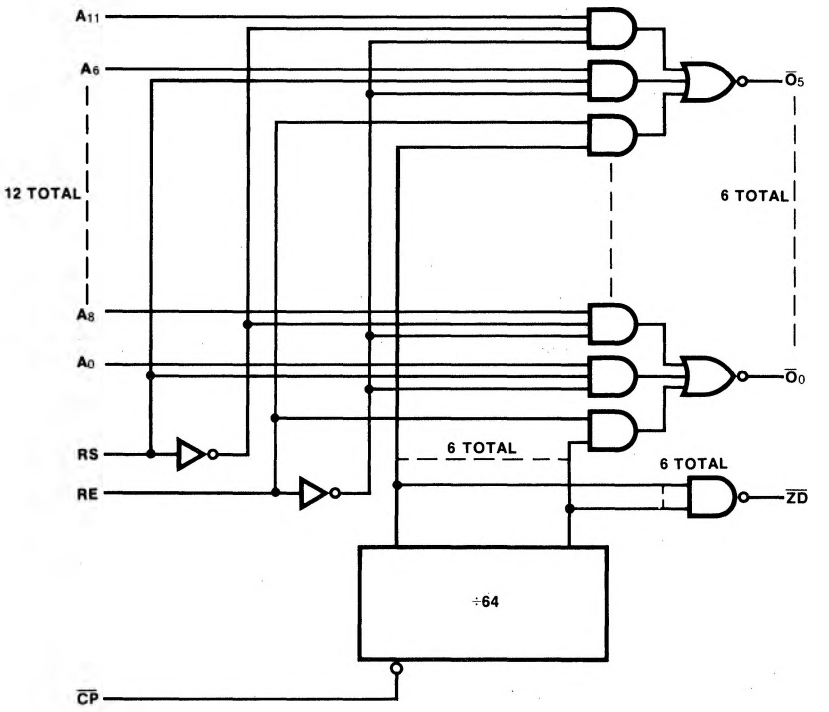
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	96LS32PC		9N
Ceramic DIP (D)	A	96LS32DC	96LS32DM	6N
Flatpak (F)	A	96LS32FC	96LS32FM	4M

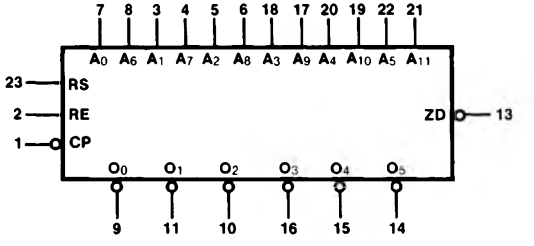
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
$A_0 - A_5$	Row Address Inputs	0.5/0.13
$A_6 - A_{11}$	Column Address Inputs	0.5/0.13
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.13
RE	Refresh Enable Input (Active HIGH)	0.5/0.13
RS	Row Select Input (Active HIGH)	0.5/0.13
$\overline{ZD}$	Refresh Counter Zero Detect Output (Active LOW)	25/3.1
$\overline{O}_0 - \overline{O}_5$	Address Outputs	25/3.1

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

FUNCTIONAL DESCRIPTION — The 96LS32 address multiplexer/refresh counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh

These functions are controlled by two signals, Refresh Enable and Row Select, both of which are active HIGH TTL inputs. the Function Table shows the levels required to multiplex to the output:

1. Refresh address (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

BURST REFRESH MODE — When refresh is requested the Refresh Enable input is HIGH. This input is ANDed with the six outputs of the internal 6-bit counter. At each $\overline{CP}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0 - \overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeroes, the Zero Detect output goes LOW signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after t_{cz} following the LOW going edge of $\overline{CP}$.

DISTRIBUTED REFRESH MODE — In the distributed refresh mode, one row is selected for refresh each ($t_{refresh/n}$) time where n = number of rows in the device and refresh is the specified refresh rate for the device. For the M4027, $t_{refresh}$ = 2.0 ms and n = 64, therefore one row is refreshed each 31 μs. Following the refresh cycle at row n, the $\overline{CP}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n + 1. The $\overline{CP}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

ROW AND COLUMN ADDRESS — All twelve system address lines are applied to the inputs of the 96LS32. When Refresh Enable is LOW and Row Select is HIGH, the input addresses $A_0 - A_5$ are gated to the outputs and applied to the driven memories. Conversely, when Row Select is LOW (with Refresh Enable still LOW), input addresses $A_6 - A_{11}$ are gated to the outputs and applied to the driven memories. When memory devices are driven directly by the 96LS32, the address applied to the memory devices is the inverse of the address at the inputs due to the inverted outputs of the 96LS32. This should be remembered when checking out the memory system.

FUNCTION TABLE

Refresh Enable	Row Select	Outputs
H	X	Refresh Address (from internal counter)
L	H	Row Address (complement of $A_0 - A_5$)
L	L	Column Address (complement of $A_6 - A_{11}$)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial